



# STH180N10F3-2 STP180N10F3

N-channel 100 V, 3.2 mΩ, 180 A STripFET™ Power MOSFET  
H<sup>2</sup>PAK, TO-220

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH180N10F3-2	100 V	4 mΩ	180 A
STP180N10F3	100 V	4.8 mΩ	120 A

- Ultra low on-resistance
- 100% avalanche tested

## Application

- High current switching applications

## Description

These devices are the latest refinement of STMicroelectronics unique “single feature size” strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

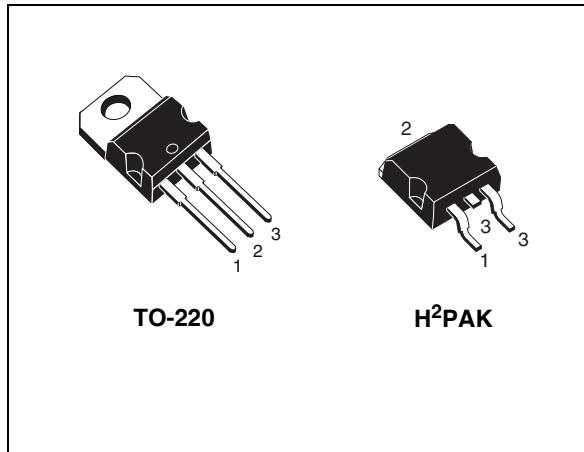
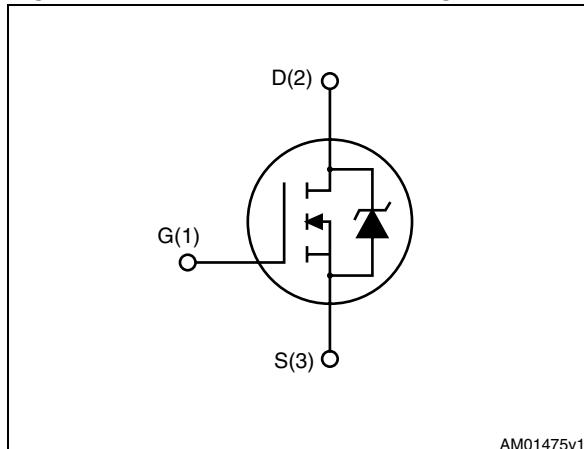


Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STH180N10F3-2	180N10F3	H <sup>2</sup> PAK	Tape and reel
STP180N10F3	180N10F3	TO-220	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	H <sup>2</sup> PAK	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> =0)	100		V
V <sub>GS</sub>	Gate-source voltage	± 20		V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25°C	120	180	A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> =100°C	110	120	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	480	720	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	315		W
	Derating factor	2.1		W/°C
dv/dt	Peak diode recovery voltage slope	TBD		V/ns
E <sub>AS</sub> <sup>(3)</sup>	Single pulse avalanche energy	TBD		mJ
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature storage temperature	- 55 to 175		°C

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 60 A, V<sub>DD</sub> = 40 V

**Table 3. Thermal data**

Symbol	Parameter	TO-220	H <sup>2</sup> PAK	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	0.48		°C/W
R <sub>thj-a</sub>	Thermal resistance junction-ambient max	62.5		°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-ambient max		35	°C/W
T <sub>I</sub>	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on FR-4 board, on 1inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_{CASE}=25^\circ\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ , $V_{DS} = \text{max rating, } @125^\circ\text{C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 200$	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$ H <sup>2</sup> PAK TO-220		3.2 3.84	4 4.8	$\text{m}\Omega$ $\text{m}\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance			6446		pF
$C_{oss}$	Output capacitance		-	710	-	pF
$C_{rss}$	Reverse transfer capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$ , $V_{GS} = 0$		51.2		pF
$Q_g$	Total gate charge			100		nC
$Q_{gs}$	Gate-source charge	$V_{DD} = 44 \text{ V}, I_D = 120 \text{ A}$ ,	-	TBD	-	nC
$Q_{gd}$	Gate-drain charge	$V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 3</a> )		TBD		nC

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time			TBD		ns
$t_r$	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 27.5 \text{ V}, I_D = 60 \text{ A}$	-	TBD	-	ns
$t_f$	Fall time	$R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 2</a> , <a href="#">Figure 7</a> )		TBD		ns

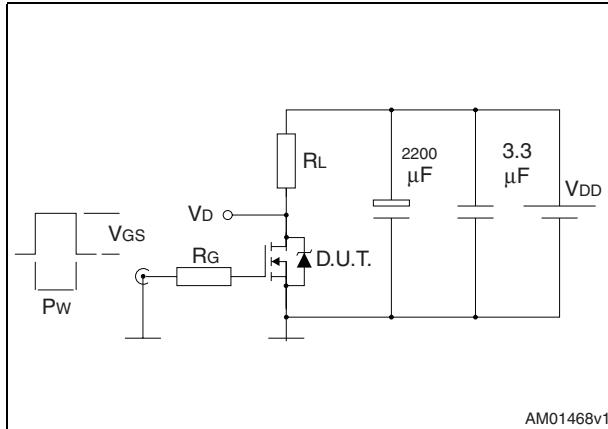
**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120\text{ A}, V_{GS}=0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=120\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD}=30\text{ V}, T_j=150^\circ\text{C}$	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current (see <i>Figure 4</i> )			TBD		A

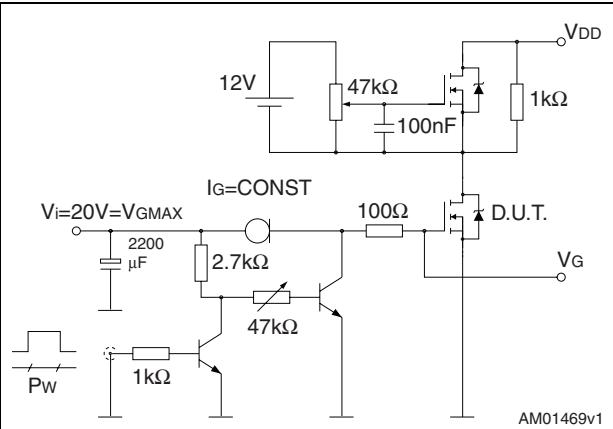
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuits

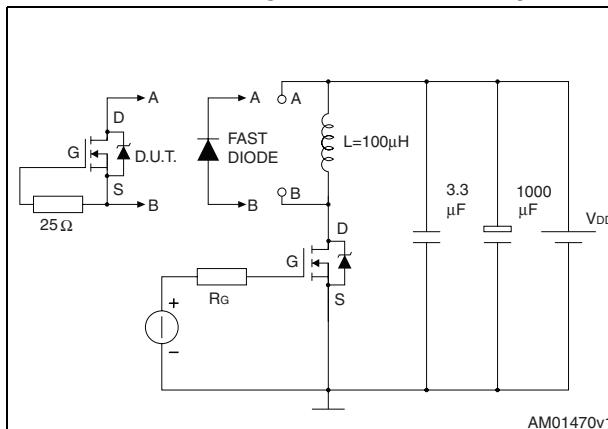
**Figure 2. Switching times test circuit for resistive load**



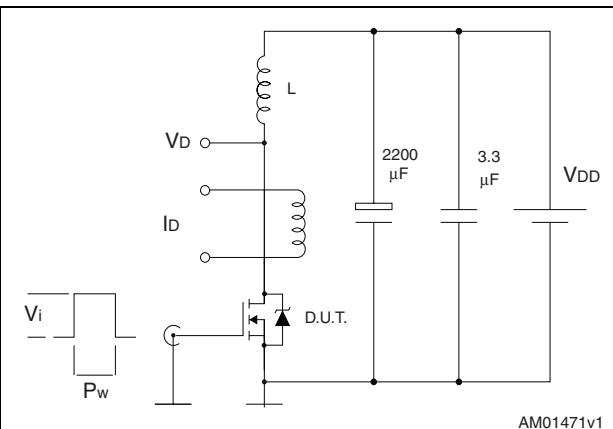
**Figure 3. Gate charge test circuit**



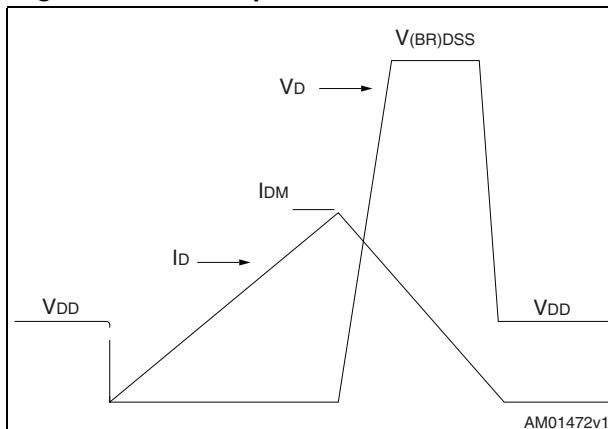
**Figure 4. Test circuit for inductive load switching and diode recovery times**



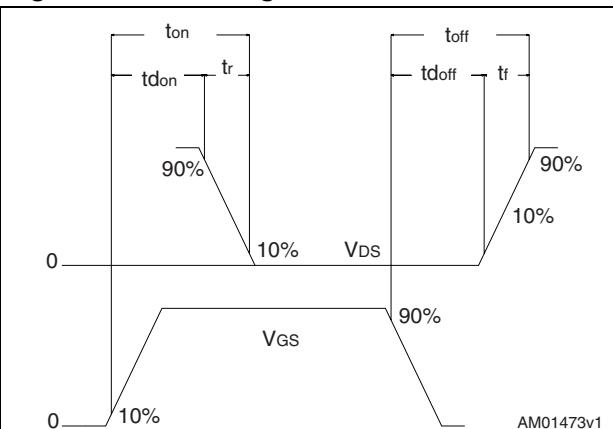
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**

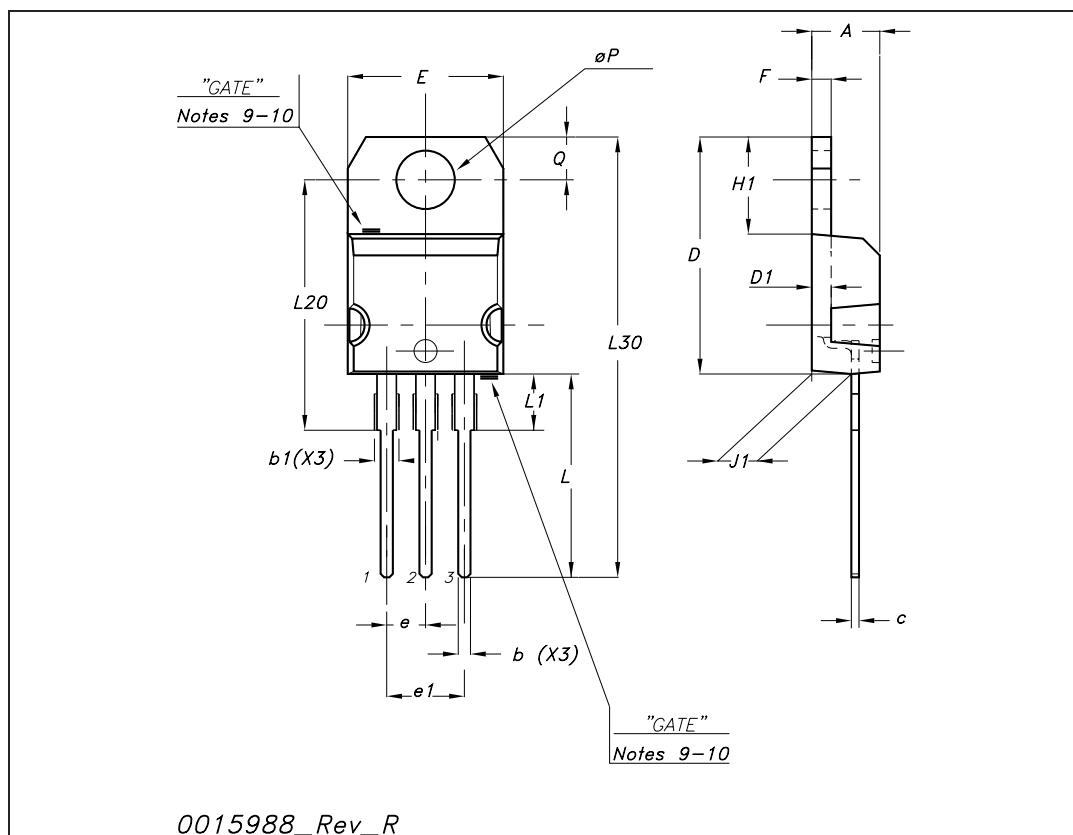


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## TO-220 mechanical data

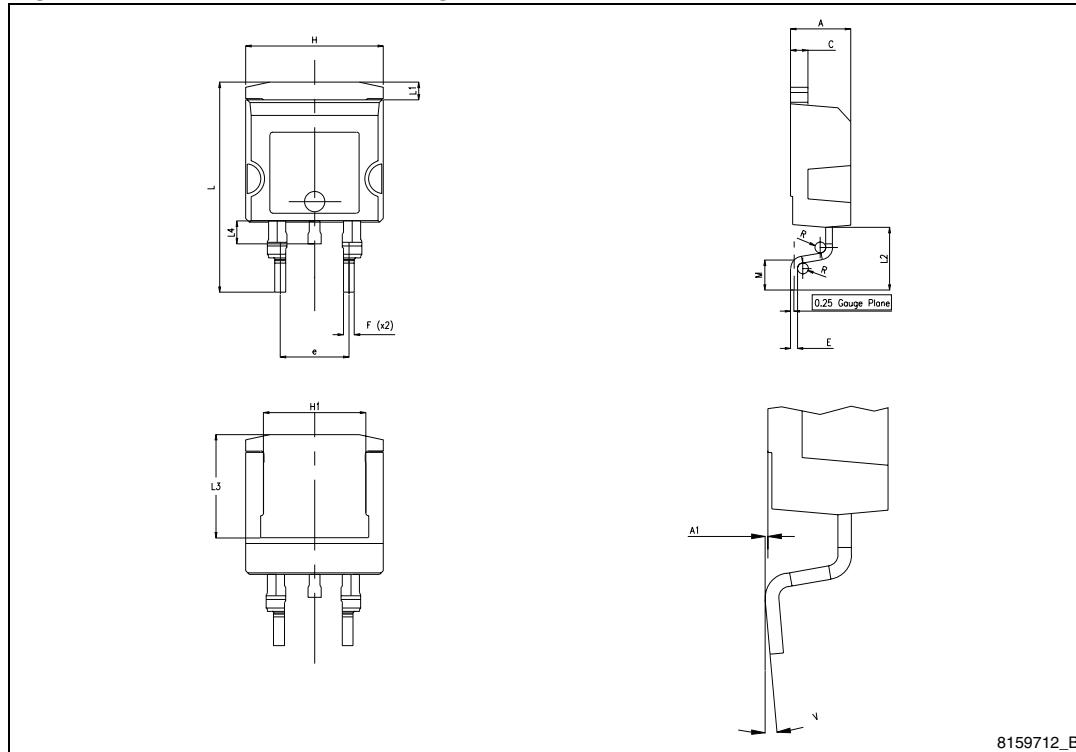
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\emptyset P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

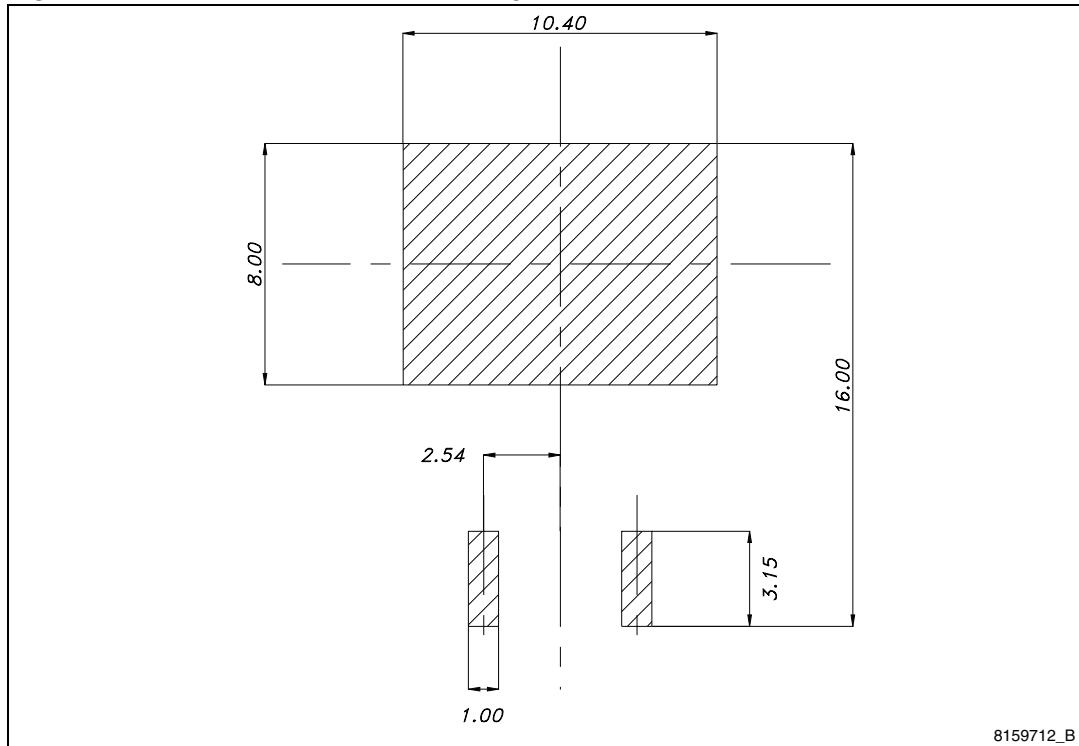


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**Table 8. H<sup>2</sup>PAK 2 leads mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

**Figure 8. H<sup>2</sup>PAK 2 leads drawing**

**Figure 9.** H<sup>2</sup>PAK 2 recommended footprint

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
01-Aug-2008	1	First version
03-jun-2010	2	<ul style="list-style-type: none"><li>– Removed package, mechanical data: D<sup>2</sup>PAK</li><li>– Added new package mechanical data: H<sup>2</sup>PAK</li></ul>

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