



Integrated Device Technology, Inc.

**128K x 8
64K x 8
CMOS DUAL-PORT
STATIC RAM MODULE**

**ADVANCE
INFORMATION
IDT7MP1021
IDT7MP1023**

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times:
– 25, 30, 35, 40, 50, 65ns
- Fully asynchronous read/write operation from either port
- On-board semaphore ($\overline{\text{SEM}}$) controls
- Surface mounted plastic components on a 64-pin FR-4 SIMM (Single In-line Memory Module)
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Single 5V ($\pm 10\%$) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION

VCC	1	2	GND
$\overline{\text{L}}_{\text{OE}}$	3	4	$\overline{\text{R}}_{\text{OE}}$
$\overline{\text{L}}_{\text{R/W}}$	5	6	$\overline{\text{R}}_{\text{R/W}}$
$\overline{\text{L}}_{\text{SEM}}$	7	8	$\overline{\text{R}}_{\text{SEM}}$
$\overline{\text{L}}_{\text{CS}}$	9	10	$\overline{\text{R}}_{\text{CS}}$
$\overline{\text{L}}_{\text{I/O}}(0)$	11	12	$\overline{\text{R}}_{\text{I/O}}(0)$
$\overline{\text{L}}_{\text{I/O}}(1)$	13	14	$\overline{\text{R}}_{\text{I/O}}(1)$
GND	15	16	$\overline{\text{R}}_{\text{I/O}}(2)$
$\overline{\text{L}}_{\text{I/O}}(2)$	17	18	$\overline{\text{R}}_{\text{I/O}}(3)$
$\overline{\text{L}}_{\text{I/O}}(3)$	19	20	$\overline{\text{R}}_{\text{I/O}}(4)$
$\overline{\text{L}}_{\text{I/O}}(4)$	21	22	$\overline{\text{R}}_{\text{I/O}}(5)$
$\overline{\text{L}}_{\text{I/O}}(5)$	23	24	$\overline{\text{R}}_{\text{I/O}}(6)$
$\overline{\text{L}}_{\text{I/O}}(6)$	25	26	$\overline{\text{R}}_{\text{I/O}}(7)$
$\overline{\text{L}}_{\text{I/O}}(7)$	27	28	$\overline{\text{R}}_{\text{A}}(0)$
$\overline{\text{L}}_{\text{A}}(0)$	29	30	$\overline{\text{R}}_{\text{A}}(1)$
$\overline{\text{L}}_{\text{A}}(1)$	31	32	$\overline{\text{R}}_{\text{A}}(2)$
$\overline{\text{L}}_{\text{A}}(2)$	33	34	$\overline{\text{R}}_{\text{A}}(3)$
$\overline{\text{L}}_{\text{A}}(3)$	35	36	$\overline{\text{R}}_{\text{A}}(4)$
$\overline{\text{L}}_{\text{A}}(4)$	37	38	$\overline{\text{R}}_{\text{A}}(5)$
$\overline{\text{L}}_{\text{A}}(5)$	39	40	$\overline{\text{R}}_{\text{A}}(6)$
$\overline{\text{L}}_{\text{A}}(6)$	41	42	$\overline{\text{R}}_{\text{A}}(7)$
$\overline{\text{L}}_{\text{A}}(7)$	43	44	$\overline{\text{R}}_{\text{A}}(8)$
$\overline{\text{L}}_{\text{A}}(8)$	45	46	GND
$\overline{\text{L}}_{\text{A}}(9)$	47	48	$\overline{\text{R}}_{\text{A}}(9)$
$\overline{\text{L}}_{\text{A}}(10)$	49	50	$\overline{\text{R}}_{\text{A}}(10)$
$\overline{\text{L}}_{\text{A}}(11)$	51	52	$\overline{\text{R}}_{\text{A}}(11)$
$\overline{\text{L}}_{\text{A}}(12)$	53	54	$\overline{\text{R}}_{\text{A}}(12)$
$\overline{\text{L}}_{\text{A}}(13)$	55	56	$\overline{\text{R}}_{\text{A}}(13)$
$\overline{\text{L}}_{\text{A}}(14)$	57	58	$\overline{\text{R}}_{\text{A}}(14)$
$\overline{\text{L}}_{\text{A}}(15)$	59	60	$\overline{\text{R}}_{\text{A}}(15)$
$\overline{\text{L}}_{\text{A}}(16)$	61	62	$\overline{\text{R}}_{\text{A}}(16)$
GND	63	64	VCC

**SIMM
TOP VIEW**

DESCRIPTION:

The IDT7MP1021/IDT7MP1023 is a 128Kx8/64Kx8 high-speed CMOS dual-port static RAM module constructed on a multilayer glass epoxy laminate (FR-4) substrate using eight IDT7006 (16K x 8) dual-port RAMs and two IDT 74FCT138 decoders. This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. The $\overline{\text{SEM}}$ controls can be used to facilitate port-to-port communication via "handshake" signaling. The $\overline{\text{SEM}}$ controls are logic latches which are part of the IDT7006 but independent of the dual-port RAM memory array. This control allows the signalling of information to easily pass through the dual-port module.

The IDT7MP1021/1023 module is packaged on a multi-layer glass epoxy laminate (FR-4) 64-pin SIMM (Single In-line Memory Module) with dimensions of only 3.85" x 0.305" x 1.12". Maximum access times as fast as 25ns over the commercial temperature range are available.

All inputs and outputs of the IDT7MP1021/1023 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

PIN NAMES

Left Port	Right Port	Description
$\overline{\text{L}}_{\text{A}}(0-16)$	$\overline{\text{R}}_{\text{A}}(0-16)$	Address Inputs
$\overline{\text{L}}_{\text{I/O}}(0-7)$	$\overline{\text{R}}_{\text{I/O}}(0-7)$	Data Inputs/Outputs
$\overline{\text{L}}_{\text{R/W}}$	$\overline{\text{R}}_{\text{R/W}}$	Read/Write Enables
$\overline{\text{L}}_{\text{CS}}$	$\overline{\text{R}}_{\text{CS}}$	Chip Select
$\overline{\text{L}}_{\text{OE}}$	$\overline{\text{R}}_{\text{OE}}$	Output Enable
$\overline{\text{L}}_{\text{SEM}}$	$\overline{\text{R}}_{\text{SEM}}$	Semaphore Control
VCC		Power
GND		Ground

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COMMERCIAL TEMPERATURE RANGE

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