

## Description

The μPD424190A/L and μPD42S4190A/L are fast-page dynamic RAMs organized as 262,144 words by 18 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424190A	+5 V
424190L	+3.3 V
42S4190A	+5 V; self-refresh mode
42S4190L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

Word writing (I/O<sub>1</sub> - I/O<sub>18</sub>), upper byte writing (I/O<sub>10</sub> - I/O<sub>18</sub>), and lower byte writing (I/O<sub>1</sub> - I/O<sub>9</sub>) are all possible using  $\overline{UWE}$  and  $\overline{LWE}$ . If  $\overline{UWE}$  or  $\overline{LWE}$  goes low during an early write cycle, all data outputs remain in high impedance. Either going low causes a byte write cycle, while bringing both low at the same time results in a word write cycle.  $\overline{UWE}$  and  $\overline{LWE}$  cannot be staggered within the same write cycle.

Refreshing may be accomplished by a  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle (CBR) that internally generates the refresh address.  $\overline{RAS}$ -only refresh cycles will also refresh all memory locations.

The self-refresh mode is entered by holding  $\overline{RAS}$  low for longer than 100 μs during a CBR cycle. Detection of this long  $\overline{RAS}$  time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

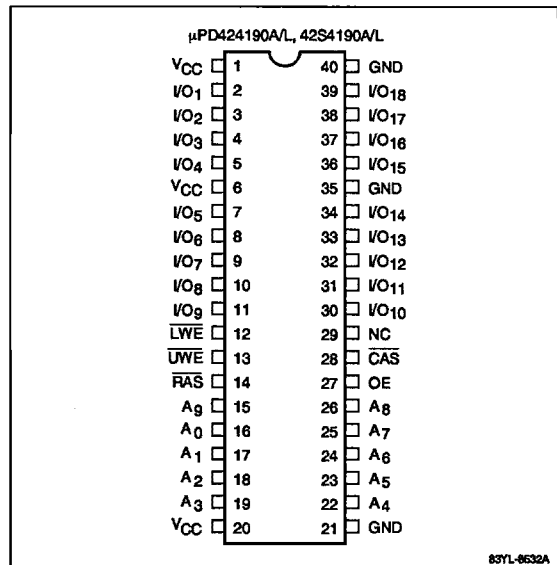
## Features

- 262,144 by 18-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option

- Byte write control with  $\overline{UWE}$  and  $\overline{LWE}$
- Low power dissipation
- $\overline{CAS}$  before  $\overline{RAS}$  refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 1024 refresh cycles every 16 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

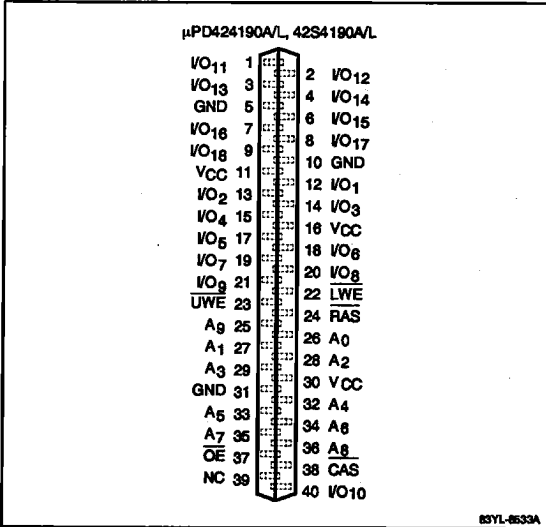
## Pin Configurations

### 40-Pin Plastic SOJ

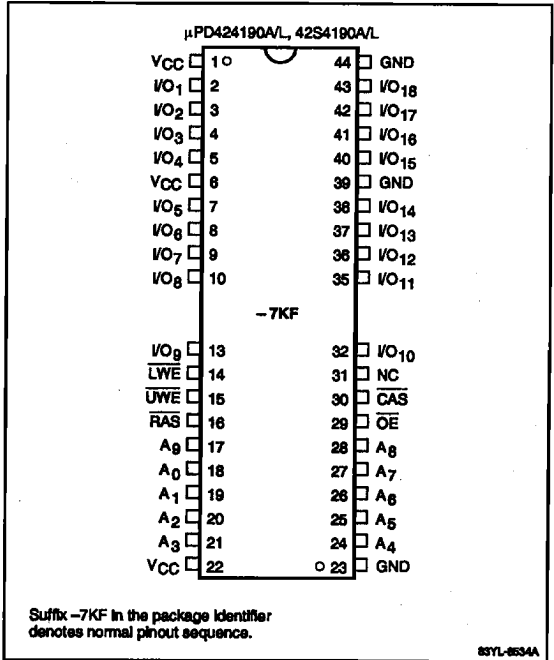


Pin Configurations (cont)

40-Pin Plastic ZIP

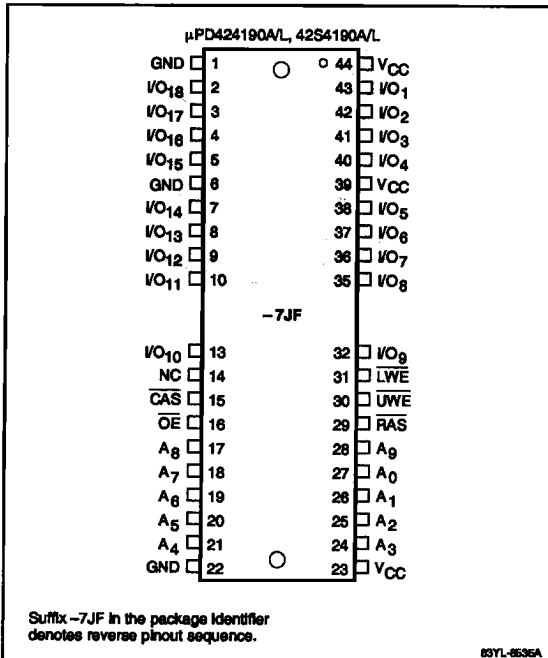


44/40-Pin Plastic TSOP (Normal Pinouts)



Suffix -7KF in the package identifier denotes normal pinout sequence.

44/40-Pin Plastic TSOP (Reverse Pinouts)



Suffix -7JF in the package identifier denotes reverse pinout sequence.

Pin Identification

Name	Function
A <sub>0</sub> - A <sub>9</sub>	Address inputs
CAS	Column address strobe
IO <sub>1</sub> - IO <sub>18</sub>	Data inputs and outputs
OE	Output enable
RAS	Row address strobe
UWE and LWE	Byte write enable
GND	Ground
V <sub>CC</sub>	+5-volt or +3.3-volt power supply
NC	No connection

### Ordering Information, μPD424190A (+ 5-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424190ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424190AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424190AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424190AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

### Ordering Information, μPD424190L (+ 3.3-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424190LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424190LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424190LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424190LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

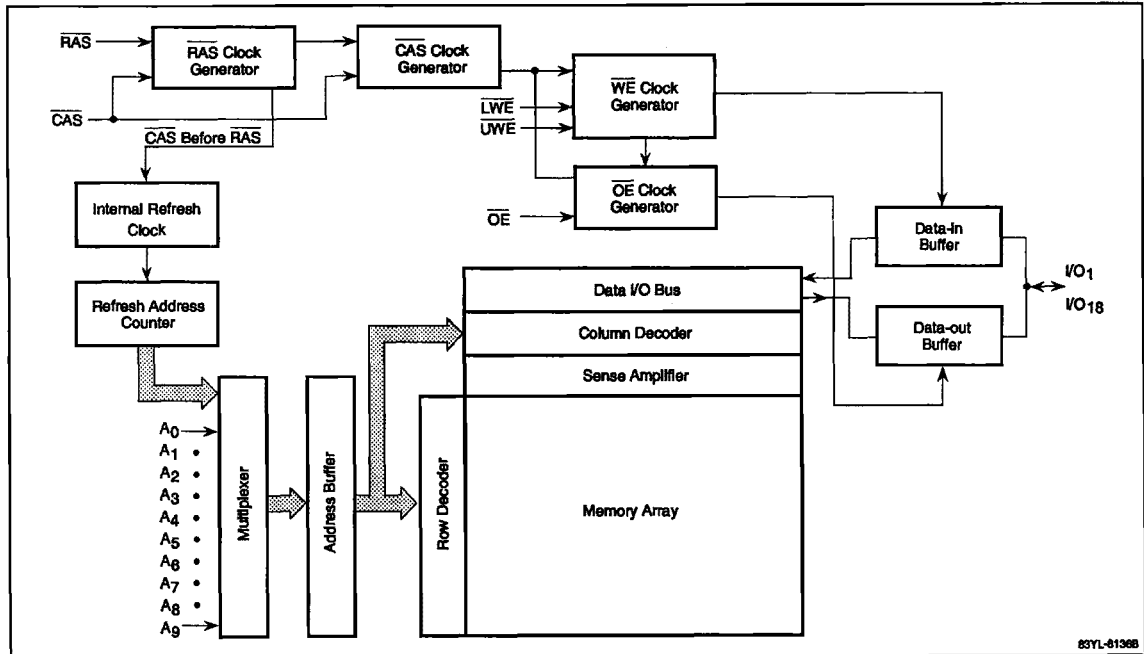
**Ordering Information, μPD42S4190A (+ 5-volt power; self-refresh mode)**

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4190ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4190AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4190AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4190AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

**Ordering Information, μPD42S4190L (+ 3.3-volt power; self-refresh mode)**

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4190LLE-A60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4190LV-A60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4190LG5-A60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4190LG5M-A60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

### Block Diagram



83YL-61368

### Truth Table

Function	RAS	LWL	UWL	CAS	OE	I/O <sub>1</sub> - I/O <sub>9</sub>	I/O <sub>10</sub> - I/O <sub>18</sub>
Standby	V <sub>IH</sub>	X	X	X	X	High-Z	High-Z
Refresh cycle	V <sub>IL</sub>	X	X	V <sub>IH</sub>	X	High-Z	High-Z
Byte write cycle	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Data input	High-Z
	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	High-Z	Data input
Word read cycle	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Data output	Data output
Word write cycle	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Data input	Data input
—	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	High-Z	High-Z

X = don't care.

**Absolute Maximum Ratings**

Voltage on any pin relative to GND	
5-volt devices	-1.0 to +7.0 V
3.3-volt devices	-0.5 to +4.6 V
Operating temperature, T <sub>OPR</sub>	0 to +70°C
Storage temperature, T <sub>STG</sub>	-55 to +125°C
Short-circuit output current, I <sub>OS</sub>	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P <sub>D</sub>	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Capacitance**

T<sub>A</sub> = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C <sub>I1</sub>	5	pF	Addresses
	C <sub>I2</sub>	7	pF	$\overline{LWE}$ , $\overline{UWE}$ , $\overline{OE}$ , RAS
Input/output capacitance	C <sub>O</sub>	7	pF	I/O <sub>1</sub> - I/O <sub>18</sub>

**Recommended Operating Conditions**

Parameter	Symbol	5-Volt Devices			3.3-Volt Devices			Unit
		Min	Typ	Max	Min	Typ	Max	
Input voltage, high	V <sub>IH</sub>	2.4		V <sub>CC</sub> + 1.0	2.0		V <sub>CC</sub> + 0.3	V
Input voltage, low	V <sub>IL</sub>	-1.0		0.8	-0.5		0.8	V
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T <sub>A</sub>	0		+70	0		+70	°C

**Self-Refresh Current**

T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = +5 V ±10% (42S4190A) or +3.3 V ±0.3 V (42S4190L)

Symbol	42S4190A	42S4190L	Conditions
I <sub>CC7</sub>	300 μA max	100 μA max	I/O pins: V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V; V <sub>IL</sub> ≤ 0.2 V or open. Other input pins: V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V; V <sub>IL</sub> ≤ 0.2 V or open. t <sub>RAS</sub> ≥ 100 μs

**DC Characteristics; 5-Volt Devices**

T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I <sub>CC2</sub>			2.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}(\text{min}); I_O = 0 \text{ mA}$
				300	μA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2 \text{ V}; I_O = 0 \text{ mA}$
Input leakage current	I <sub>I(L)</sub>	-10		10	μA	V <sub>IN</sub> = 0 V to V <sub>CC</sub> ; all other pins not under test = 0 V
Output leakage current	I <sub>O(L)</sub>	-10		10	μA	D <sub>OUT</sub> disabled; V <sub>OUT</sub> = 0 V to V <sub>CC</sub>
Output voltage, low	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4.2 mA
Output voltage, high	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -5 mA

### DC Characteristics; 3.3-Volt Devices

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +3.3\text{ V} \pm 0.3\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	$I_{CC2}$			500	$\mu\text{A}$	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{IH}(\text{min}); I_O = 0\text{ mA}$
				100	$\mu\text{A}$	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}; I_O = 0\text{ mA}$
Input leakage current	$I_{I(L)}$	-5		5	$\mu\text{A}$	$V_{IN} = 0\text{ V to } V_{CC}$ ; all other pins not under test = $0\text{ V}$
Output leakage current	$I_{O(L)}$	-5		5	$\mu\text{A}$	$D_{OUT}$ disabled; $V_{OUT} = 0\text{ V to } V_{CC}$
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = -2.0\text{ mA}$
Output voltage, high	$V_{OH}$	2.4			V	$I_{OH} = -2.0\text{ mA}$

### AC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$

μPD424190A, 42S4190A:  $V_{CC} = +5.0\text{ V} \pm 10\%$

μPD424190L, 42S4190L:  $V_{CC} = +3.3\text{ V} \pm 0.3\text{ V}$

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Operating current, average	$I_{CC1} (+5)$		130		120		110	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling; $t_{RC} = t_{RC} \text{ min (Note 5)}$
	$I_{CC1} (+3.3)$		120		110		100		
Operating current, $\overline{\text{RAS}}$ -only refresh cycle, average	$I_{CC3} (+5)$		130		120		110	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} \geq V_{IH} \text{ min}; t_{RC} = t_{RC} \text{ min (Note 5)}$
	$I_{CC3} (+3.3)$		120		110		100		
Operating current, fast-page cycle, average	$I_{CC4} (+5)$		110		100		90	mA	$\overline{\text{RAS}} \leq V_{IL}$ ; $\overline{\text{CAS}}$ cycling; $t_{PC} = t_{PC} \text{ min (Note 5)}$
	$I_{CC4} (+3.3)$		110		100		90		
Operating current, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, average	$I_{CC5} (+5)$		140		130		120	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} \leq V_{IL} \text{ max}; t_{RC} = t_{RC} \text{ min (Note 5)}$
	$I_{CC5} (+3.3)$		130		120		110		
Access time from column address	$t_{AA}$		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{\text{CAS}}$ precharge (rising edge)	$t_{ACP}$		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	$t_{ASC}$	0		0		0		ns	
Row address setup time	$t_{ASR}$	0		0		0		ns	
Column address to $\overline{\text{WE}}$ delay time	$t_{AWD}$	50		55		70		ns	(Note 14)
Access time from $\overline{\text{CAS}}$ (falling edge)	$t_{CAC}$		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	$t_{CAH}$	15		15		15		ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	20	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing	$t_{CHR}$	15		15		15		ns	(Note 15)
$\overline{\text{CAS}}$ hold time (CBR self-refresh mode)	$t_{CHS}$	-35		-40		-50		ns	For 42S4190A/L only

**AC Characteristics (cont)**

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
CAS to output in low-Z	t <sub>CLZ</sub>	0		0		0		ns	(Notes 4, 7)
Fast-page CAS precharge time	t <sub>CP</sub>	10		10		10		ns	
CAS precharge time	t <sub>CPN</sub>	10		10		10		ns	
Fast-page CAS precharge to WE delay time	t <sub>CPWD</sub>	55		60		75		ns	(Note 14)
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10		ns	(Note 10)
CAS hold time	t <sub>CSH</sub>	60		70		80		ns	
CAS setup time for CAS before RAS refresh cycle	t <sub>CSR</sub>	5		5		5		ns	(Note 15)
CAS to WE delay	t <sub>CWD</sub>	40		40		50		ns	(Note 14)
Write command referenced to CAS lead time	t <sub>CWL</sub>	15		15		15		ns	
Data-in hold time	t <sub>DH</sub>	15		15		15		ns	(Notes 13, 16)
Data-in setup time	t <sub>DS</sub>	0		0		0		ns	(Notes 13, 16)
Masked write hold time referenced to CAS	t <sub>MCH</sub>	0		0		0		ns	
Masked write setup time	t <sub>MCS</sub>	0		0		0		ns	
Masked write hold time referenced to RAS	t <sub>MRH</sub>	0		0		0		ns	
Access time from OE	t <sub>OEA</sub>		20		20		20	ns	(Notes 3, 4, 7, 8)
OE data delay time	t <sub>OED</sub>	15		15		15		ns	
OE command hold time	t <sub>OEH</sub>	0		0		0		ns	
OE to RAS inactive setup time	t <sub>OES</sub>	0		0		0		ns	
Output turnoff delay from OE	t <sub>OEZ</sub>	0	15	0	15	0	15	ns	(Note 9)
Output disable from CAS high	t <sub>OFF</sub>	0	15	0	15	0	20	ns	(Note 9)
OE to output in low-Z	t <sub>OLZ</sub>	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t <sub>PC</sub>	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with extended data output	t <sub>PRWC</sub>	85		90		100		ns	(Note 6)



### AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{\text{RAS}}$ to column address delay time	$t_{\text{RAD}}$	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	$t_{\text{RAH}}$	10		10		10		ns	
Column address lead time referenced to $\overline{\text{RAS}}$ (rising edge)	$t_{\text{RAL}}$	30		35		40		ns	
$\overline{\text{RAS}}$ pulse width	$t_{\text{RAS}}$	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{\text{RAS}}$ pulse width	$t_{\text{RASp}}$	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{RAS}}$ pulse width (CBR self-refresh mode)	$t_{\text{RASS}}$	100		100		100		μs	For 42S4190A/L
Random read or write cycle time	$t_{\text{RC}}$	120		130		150		ns	(Note 6)
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{\text{RCD}}$	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0		0		0		ns	(Note 11)
Read command setup time	$t_{\text{RCS}}$	0		0		0		ns	
Refresh period	$t_{\text{REF}}$		16		16		16	ms	Addresses $A_0 - A_9$
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{CAS}}$ precharge	$t_{\text{RHCP}}$	35		40		45		ns	
$\overline{\text{RAS}}$ precharge time	$t_{\text{RP}}$	50		50		60		ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	$t_{\text{RPC}}$	0		0		0		ns	
$\overline{\text{RAS}}$ precharge time (CBR self-refresh mode)	$t_{\text{RPS}}$	120		130		150		ns	For 42S4190A/L
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0		0		0		ns	(Note 11)
$\overline{\text{RAS}}$ hold time	$t_{\text{RSH}}$	20		20		25		ns	
Read-modify-write cycle time	$t_{\text{RWC}}$	165		175		200		ns	(Note 6)
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	$t_{\text{RWD}}$	80		90		105		ns	(Note 14)
Write command referenced to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	20		20		20		ns	
Rise and fall times	$t_{\text{r}}$	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	$t_{\text{WCH}}$	15		15		15		ns	(Note 12)

## AC Characteristics (cont)

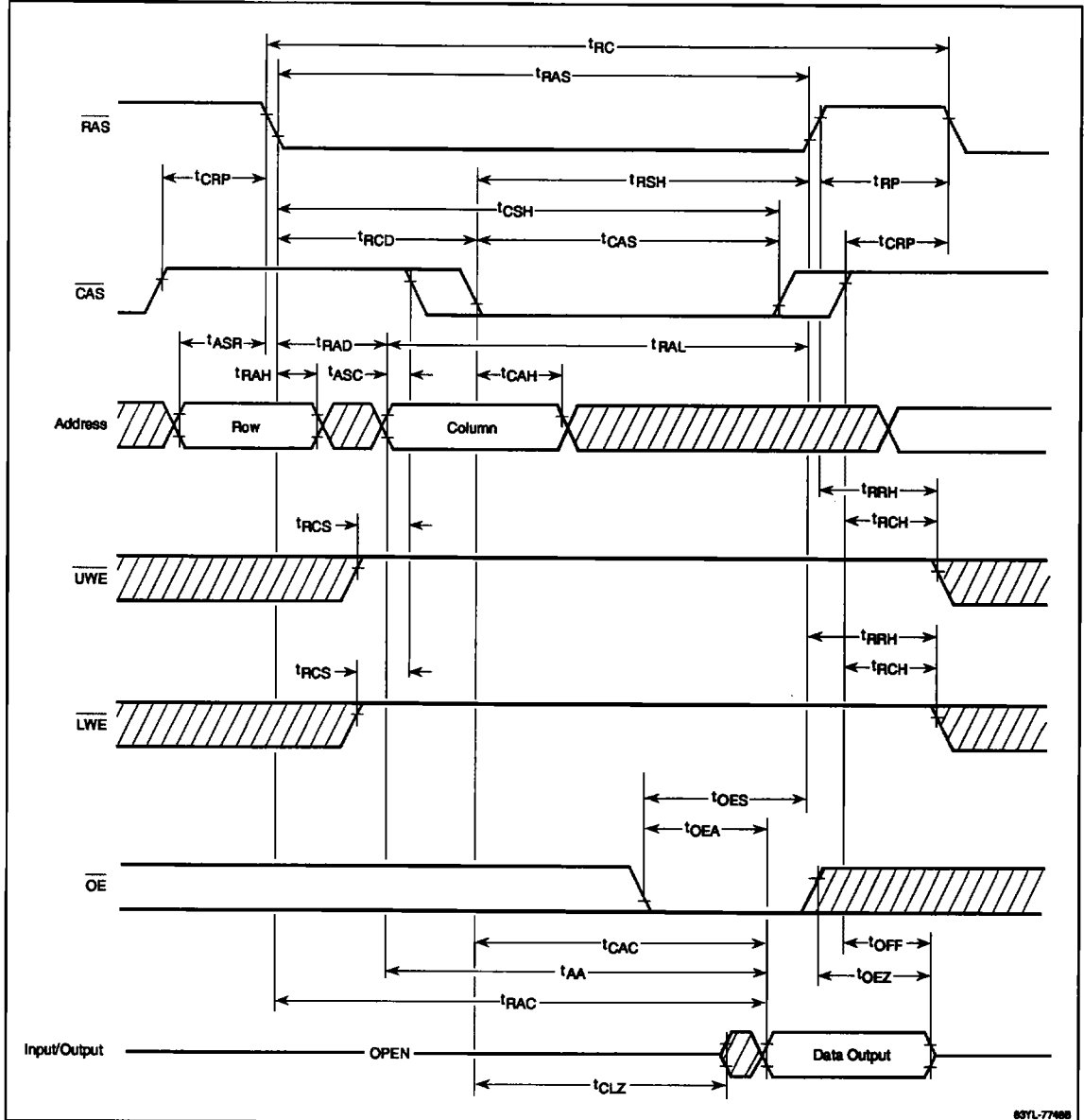
Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Write command setup time	$t_{WCS}$	0		0		0		ns	(Note 14)
Write command pulse width	$t_{WP}$	15		15		15		ns	(Note 12)

## Notes:

- (1) All voltages are referenced to GND.
- (2) An initial pause of 100  $\mu$ s is required after power-up, followed by any eight RAS cycles, before proper device operation is achieved.
- (3) Ac measurements assume  $t_T = 5$  ns.
- (4)  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring the timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- (5)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC5}$  depend on output loading and cycle rates. Specified values are obtained with the output open.  $I_{CC3}$  is measured assuming that all column address inputs are held at either a high level or a low level during  $\overline{RAS}$ -only refresh cycles.  $I_{CC4}$  is measured assuming that all column address inputs are switched only once during each fast-page cycle.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ( $T_A = 0$  to  $+70^\circ\text{C}$ ) is assured.
- (7) Load = 2 TTL ( $-1$  mA,  $+4$  mA) loads and 100 pF. For 3.3-volt devices,  $V_{OH} = 2.0$  V and  $V_{OL} = 0.8$  V (ac reference levels).
- (8) If  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ , access time is defined by  $t_{RAC}(\text{max})$ .  
If  $t_{RCD} \geq t_{RCD}(\text{max})$ , access time is defined by  $t_{CAD}(\text{max})$ .  
If  $t_{RAD} \geq t_{RAD}(\text{max})$ , access time is defined by  $t_{AAD}(\text{max})$ .
- (9)  $t_{OFF}(\text{max})$  and  $t_{OEZ}(\text{max})$  define the time at which the outputs become open-circuit and are not referenced to  $V_{OH}$  or  $V_{OL}$ .
- (10) The  $t_{CRP}$  requirement should be applicable for  $\overline{RAS}/\overline{CAS}$  cycles preceded by any cycle.
- (11) Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- (12) Parameter  $t_{WP}$  is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both  $t_{WCS}$  and  $t_{WCH}$  must be met.
- (13) These parameters are referenced to the falling edge of  $\overline{CAS}$  for early write cycles and to the falling edge of  $\overline{WE}$  for delayed write or read-modify-write cycles.
- (14)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{CPWD}$  and  $t_{AWD}$  are restrictive operating parameters in read-write/read-modify-write cycles only. If  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{RWD} \geq t_{RWD}(\text{min})$ , and  $t_{AWD} \geq t_{AWD}(\text{min})$ , then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until  $\overline{CAS}$  returns to  $V_{IH}$ ) is indeterminate.
- (15) Holding  $\overline{CAS}$  low prior to  $\overline{RAS}$  going negative will initiate a  $\overline{CAS}$  before RAS refresh cycle ( $t_{CSR}$  and  $t_{CHR}$  must be satisfied).
- (16) The first  $\overline{WE}$  falling edge is used as a reference for the setup and hold requirements of  $t_{DS}$  and  $t_{DH}$  (late write cycle).

## Timing Waveforms

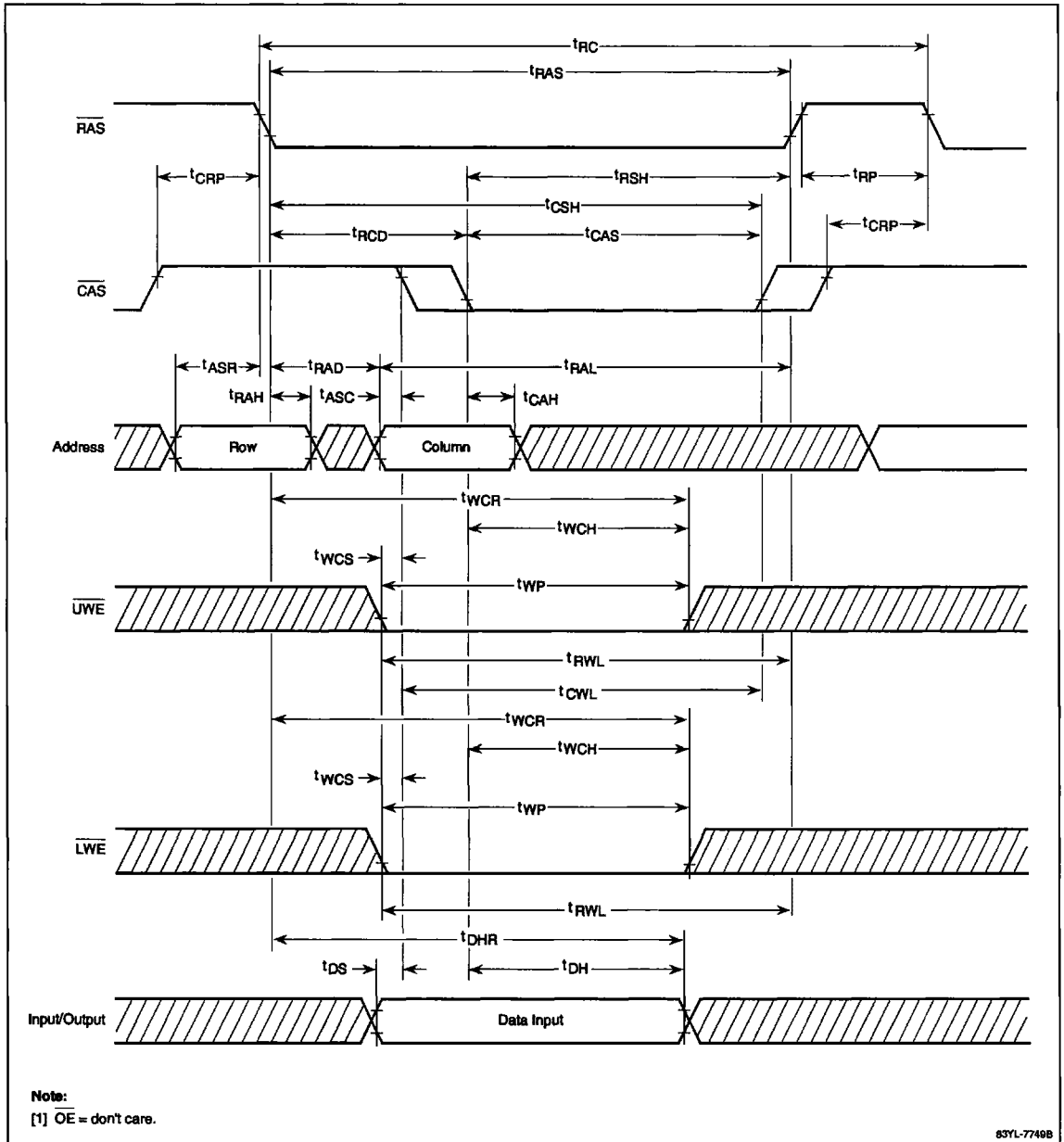
### Word Read Cycle



7b

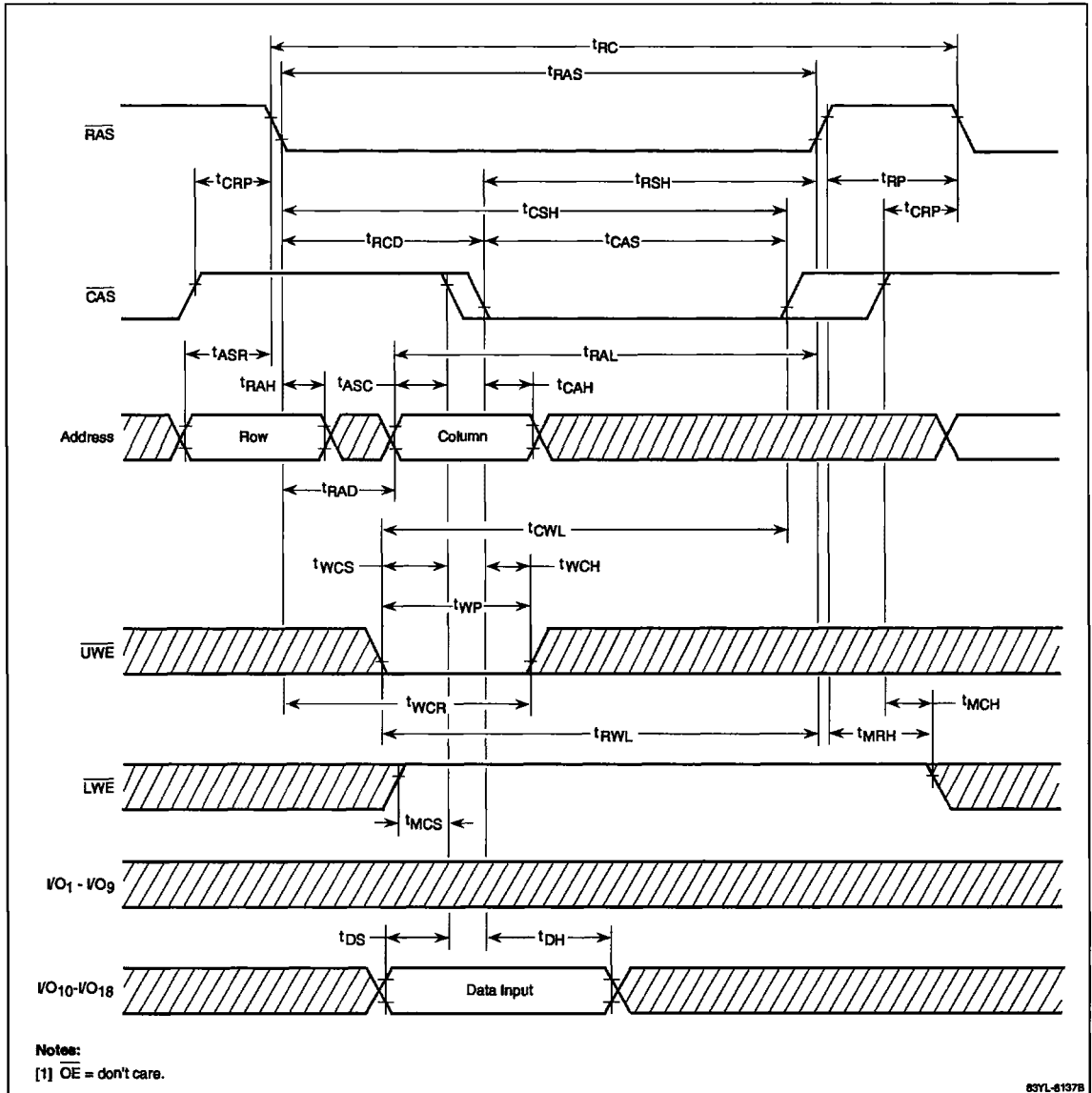
Timing Waveforms (cont)

**Word Early-Write Cycle**



## Timing Waveforms (cont)

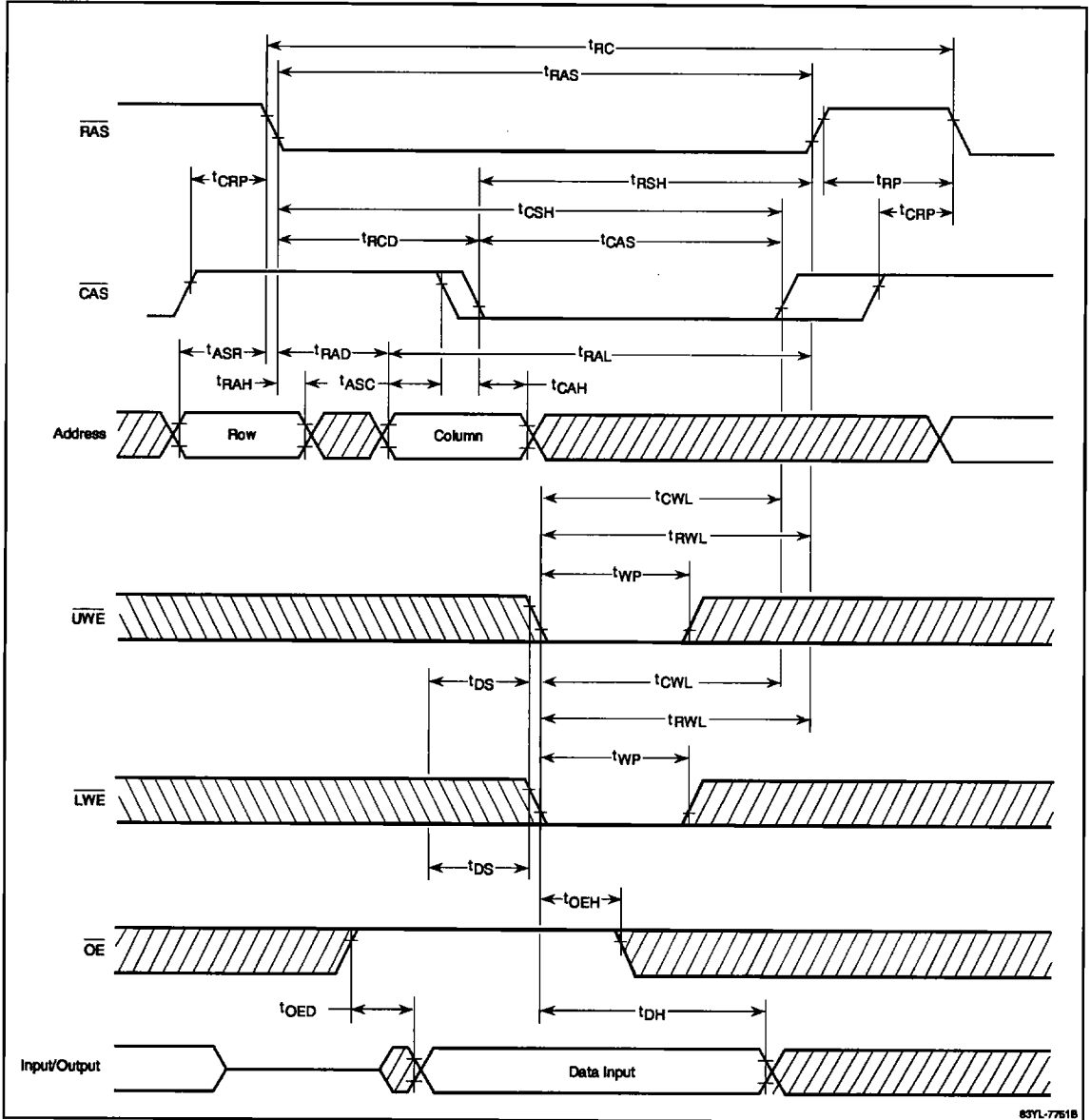
### Byte Early-Write Cycle



7b

Timing Waveforms (cont)

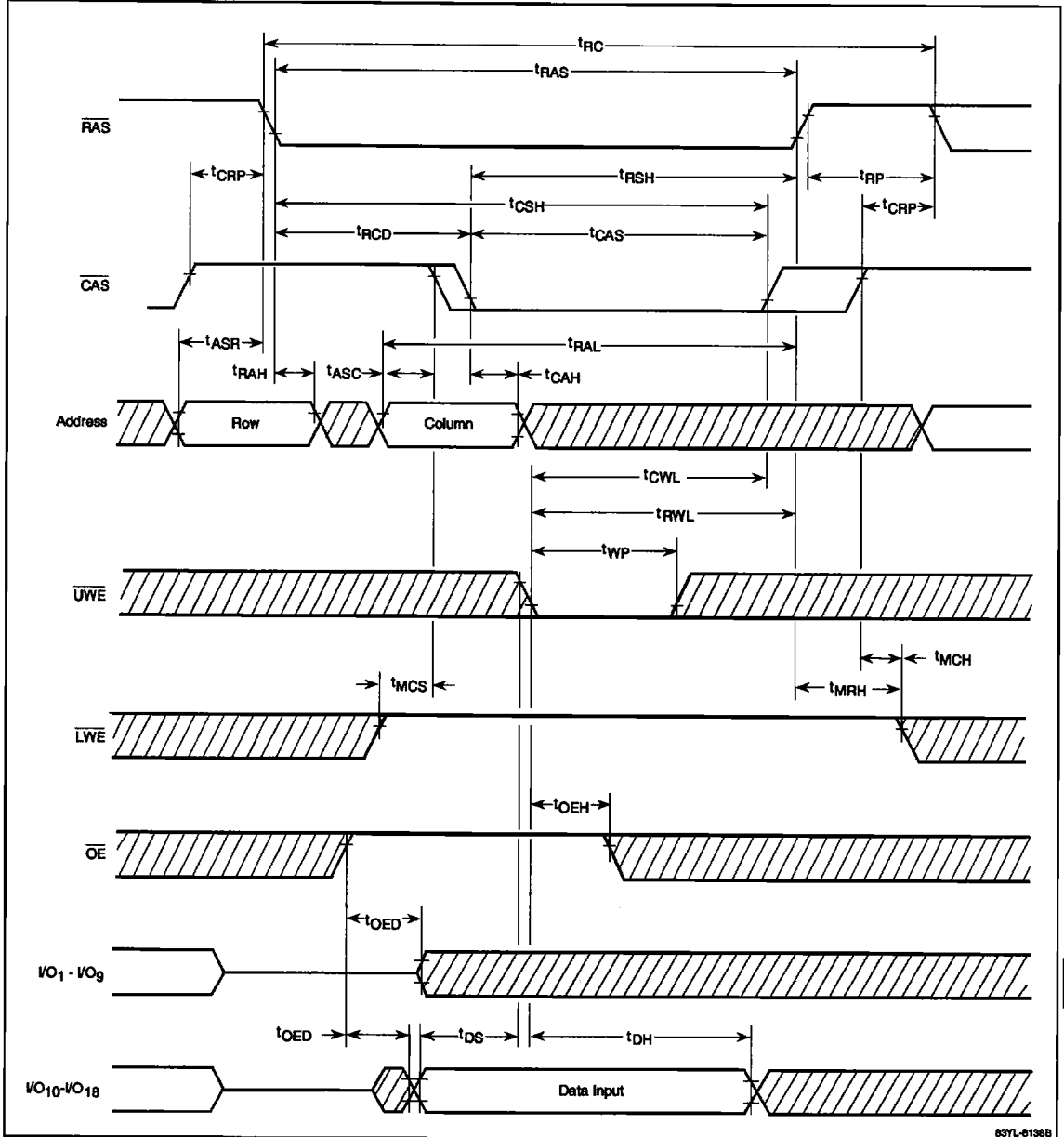
**Word Late-Write Cycle**



83YL-7751B

## Timing Waveforms (cont)

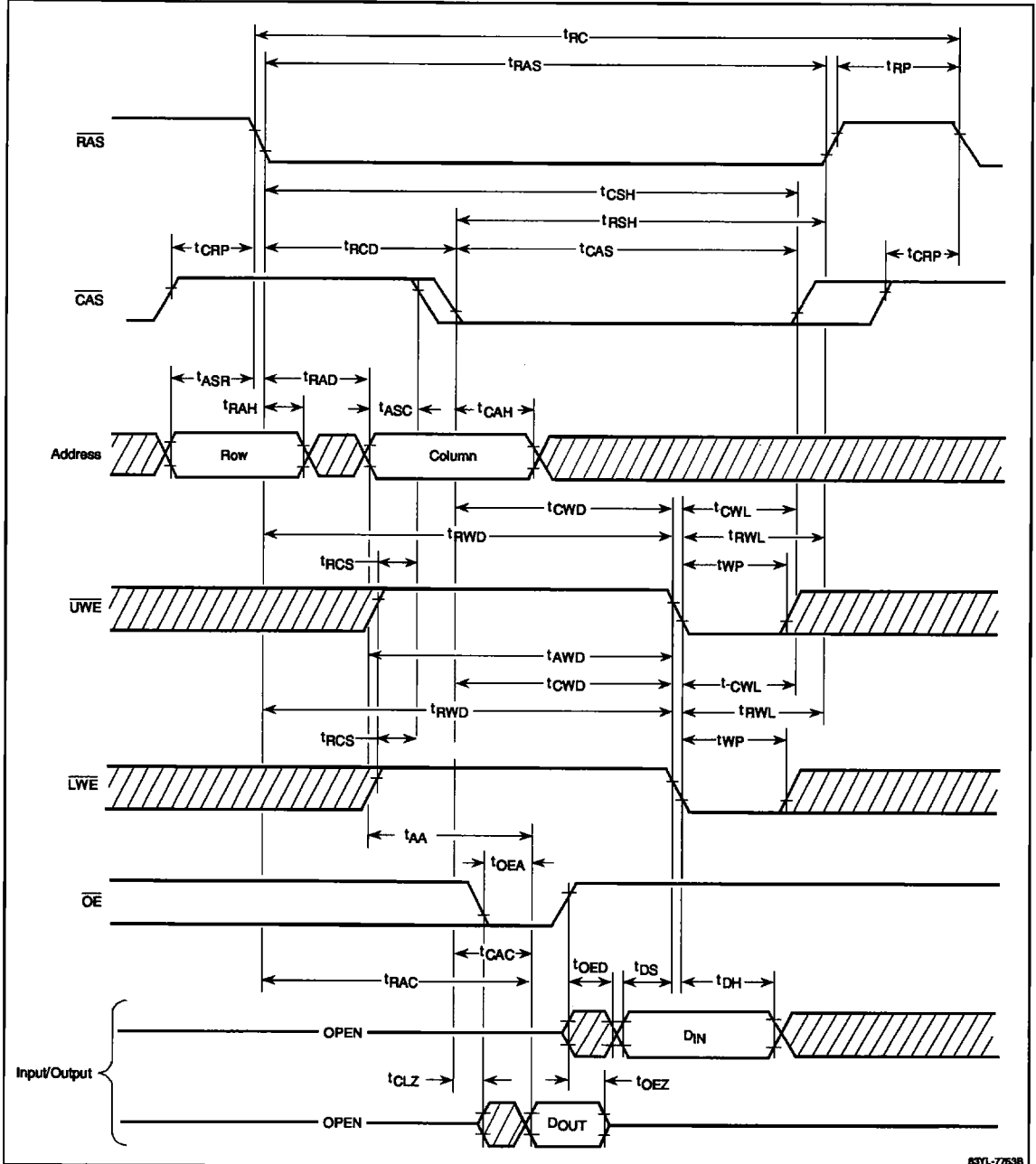
### Byte Late-Write Cycle



7b

Timing Waveforms (cont)

Word Read-Modify-Write Cycle

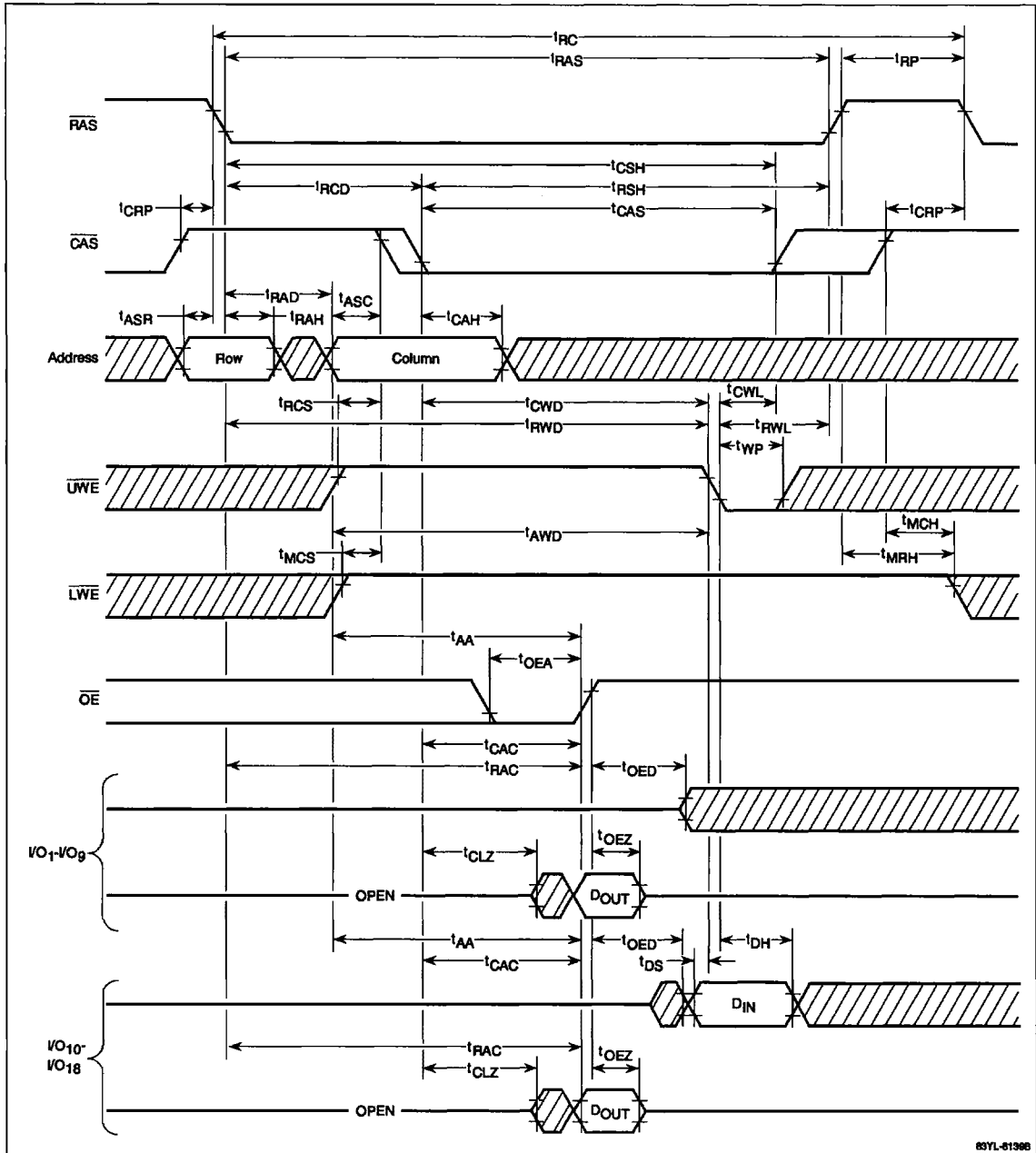


83YL-7763B



### Timing Waveforms (cont)

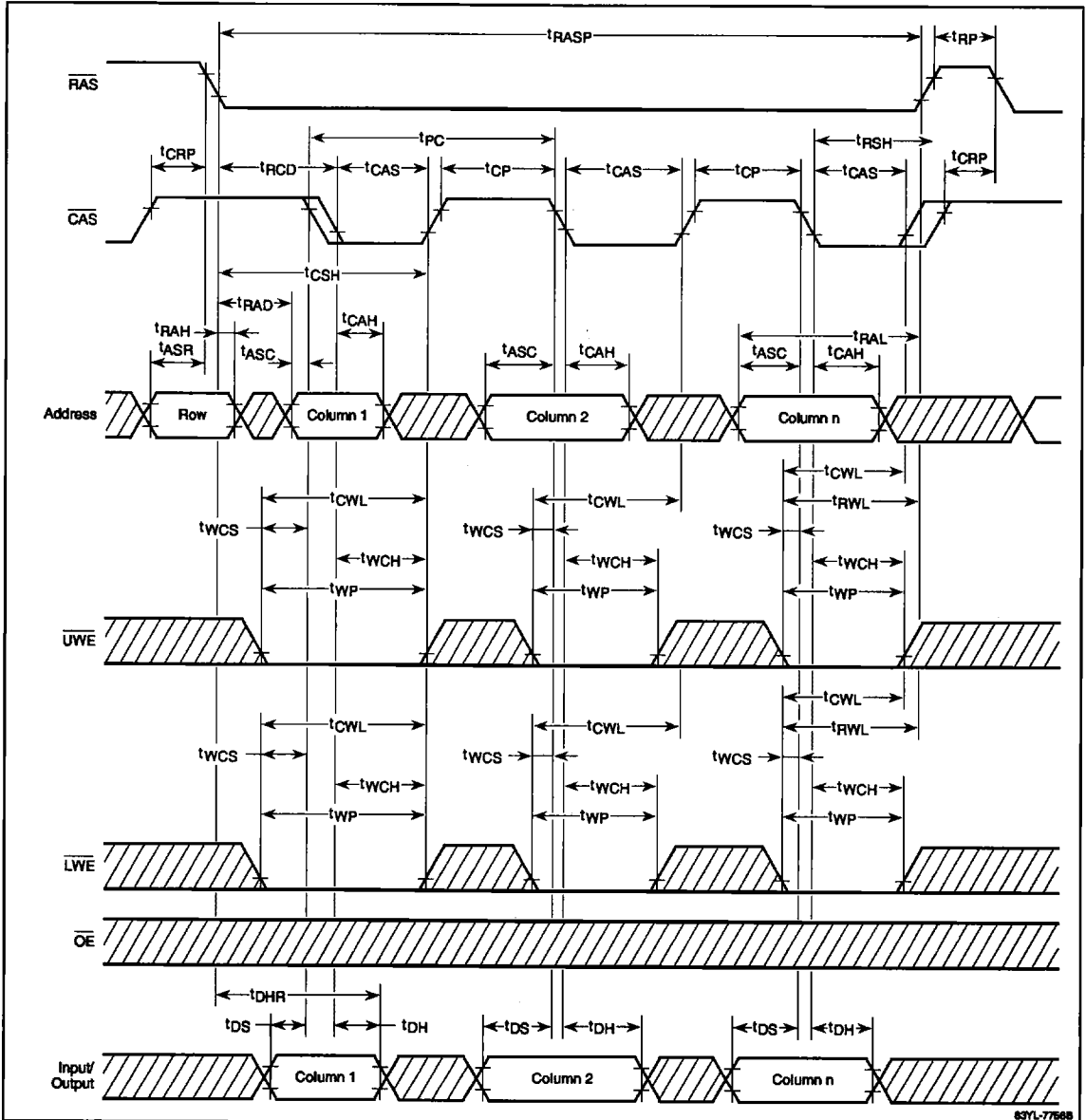
#### Byte Read-Modify-Write Cycle





## Timing Waveforms (cont)

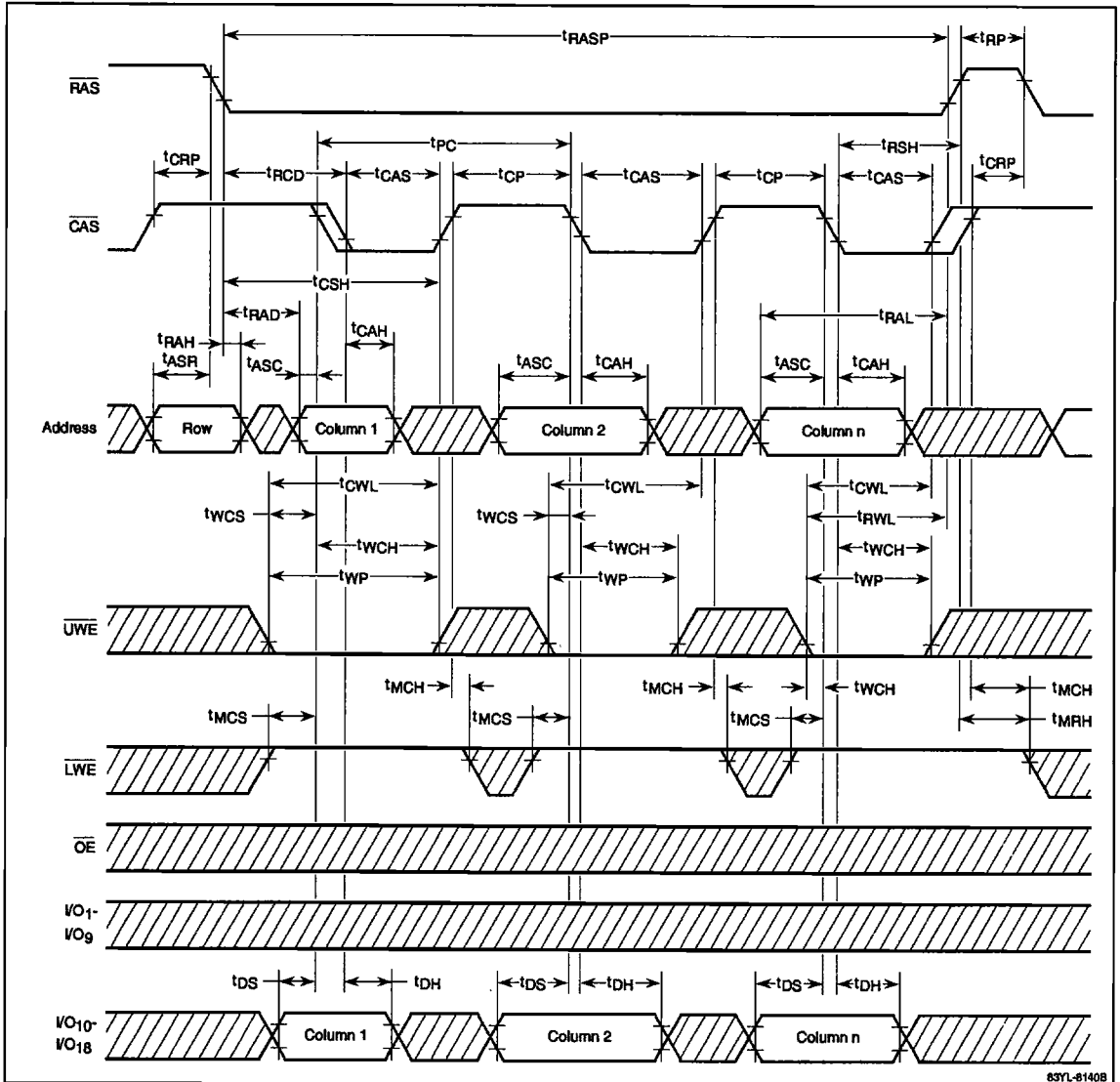
### Word Fast-Page-Write Cycle



7b

Timing Waveforms (cont)

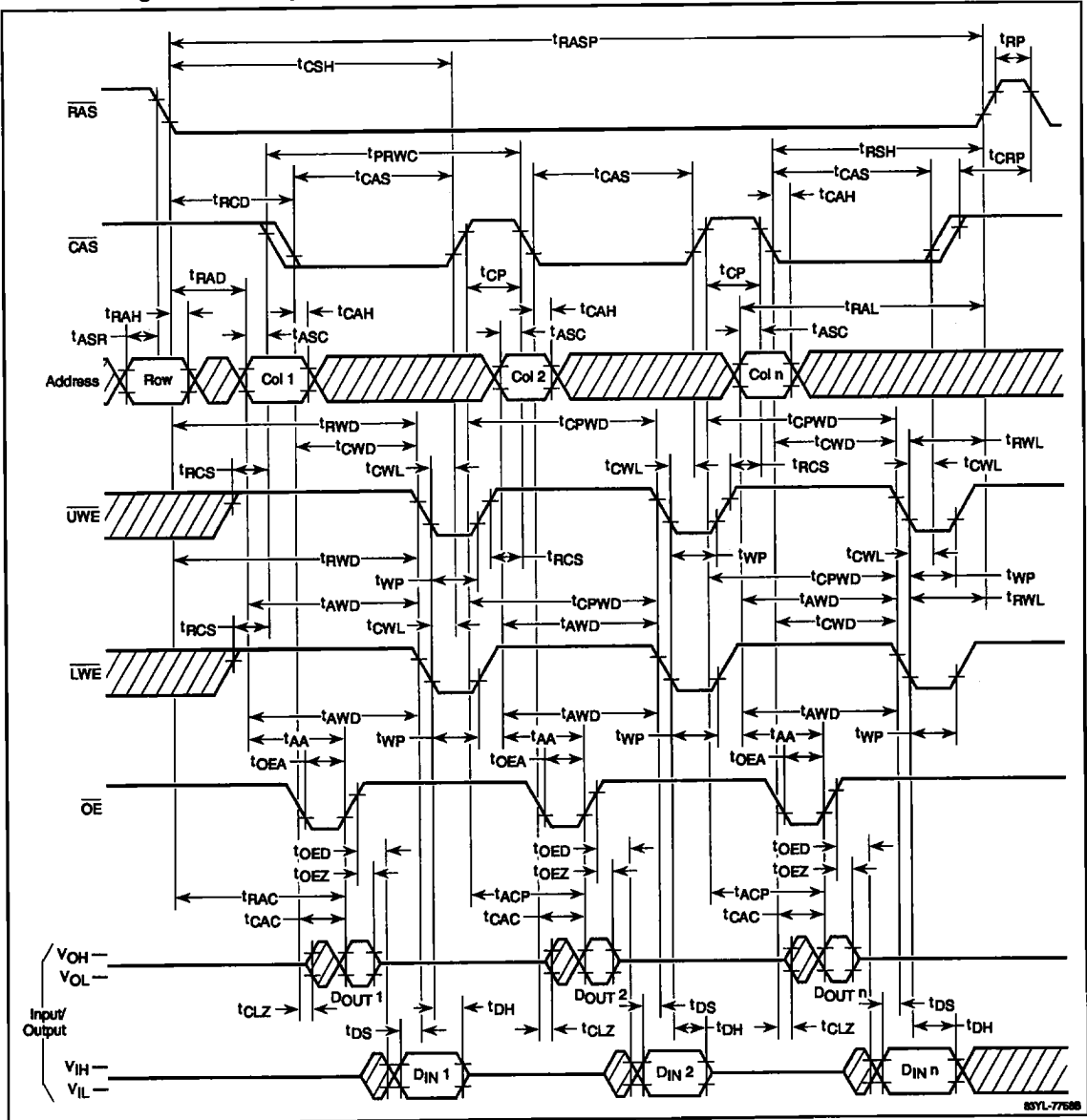
**Byte Fast-Page Write Cycle**



83YL-8140B

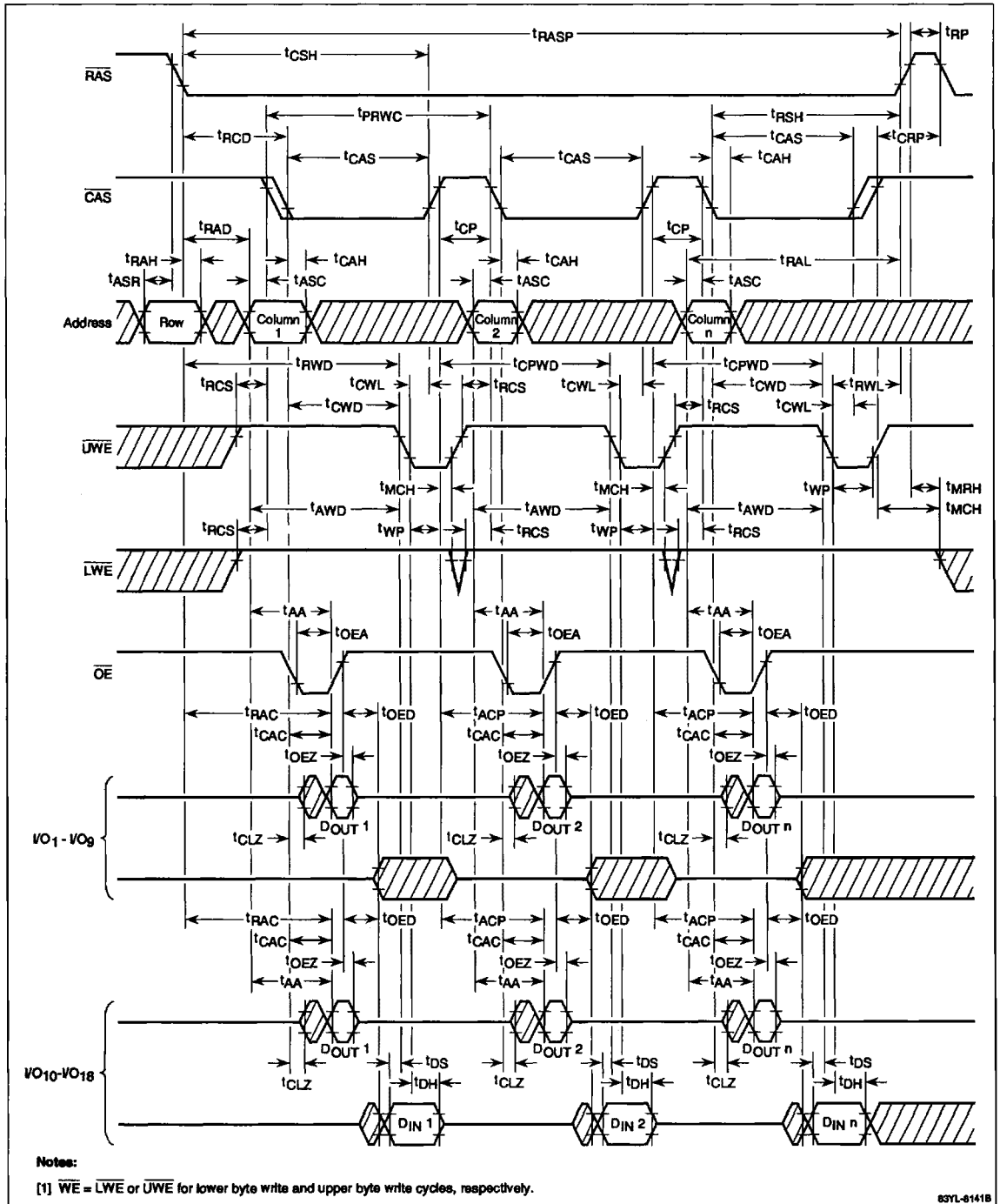
## Timing Waveforms (cont)

### Word Fast-Page Read-Modify-Write Cycle



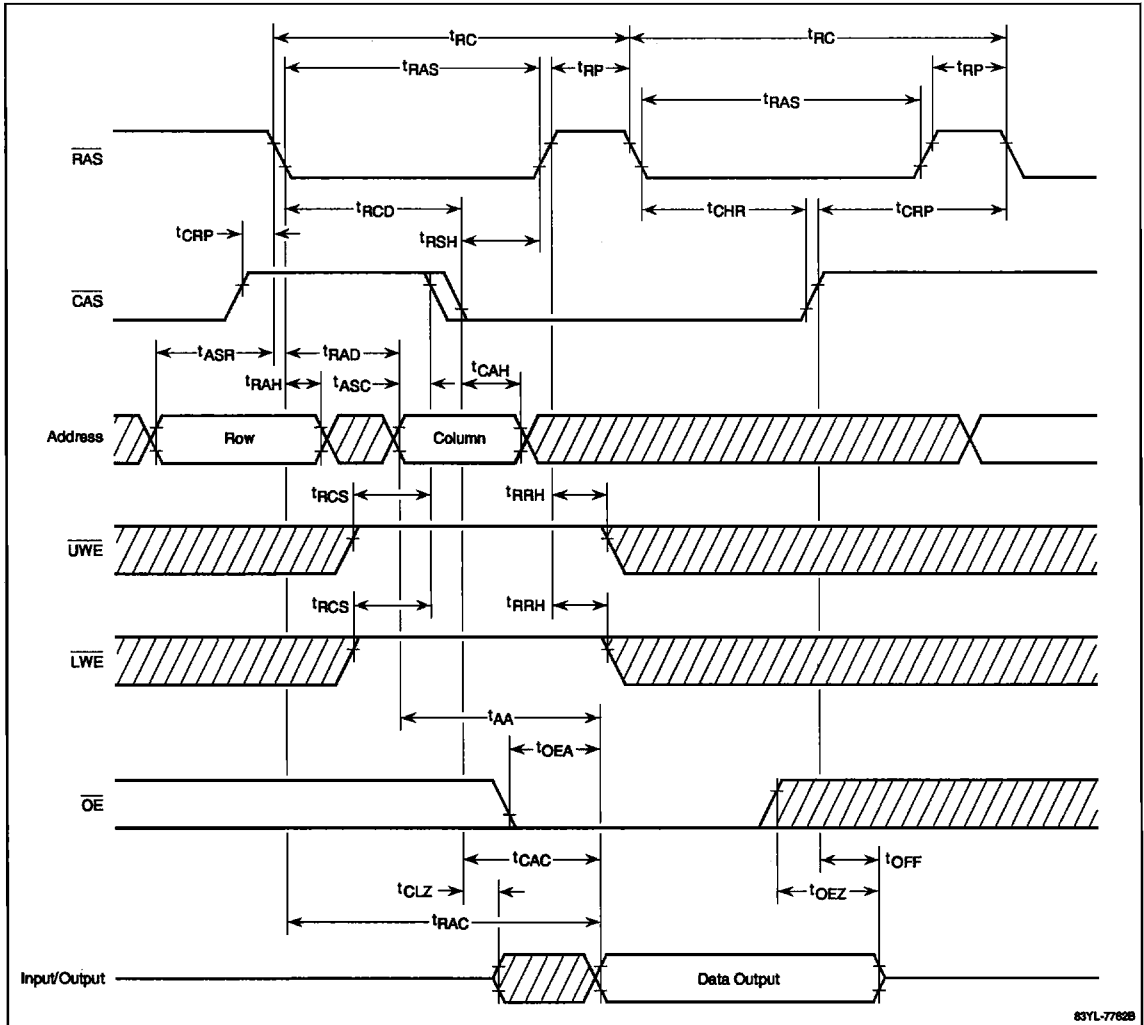
7b

Byte Fast-Page Read-Modify-Write Cycle



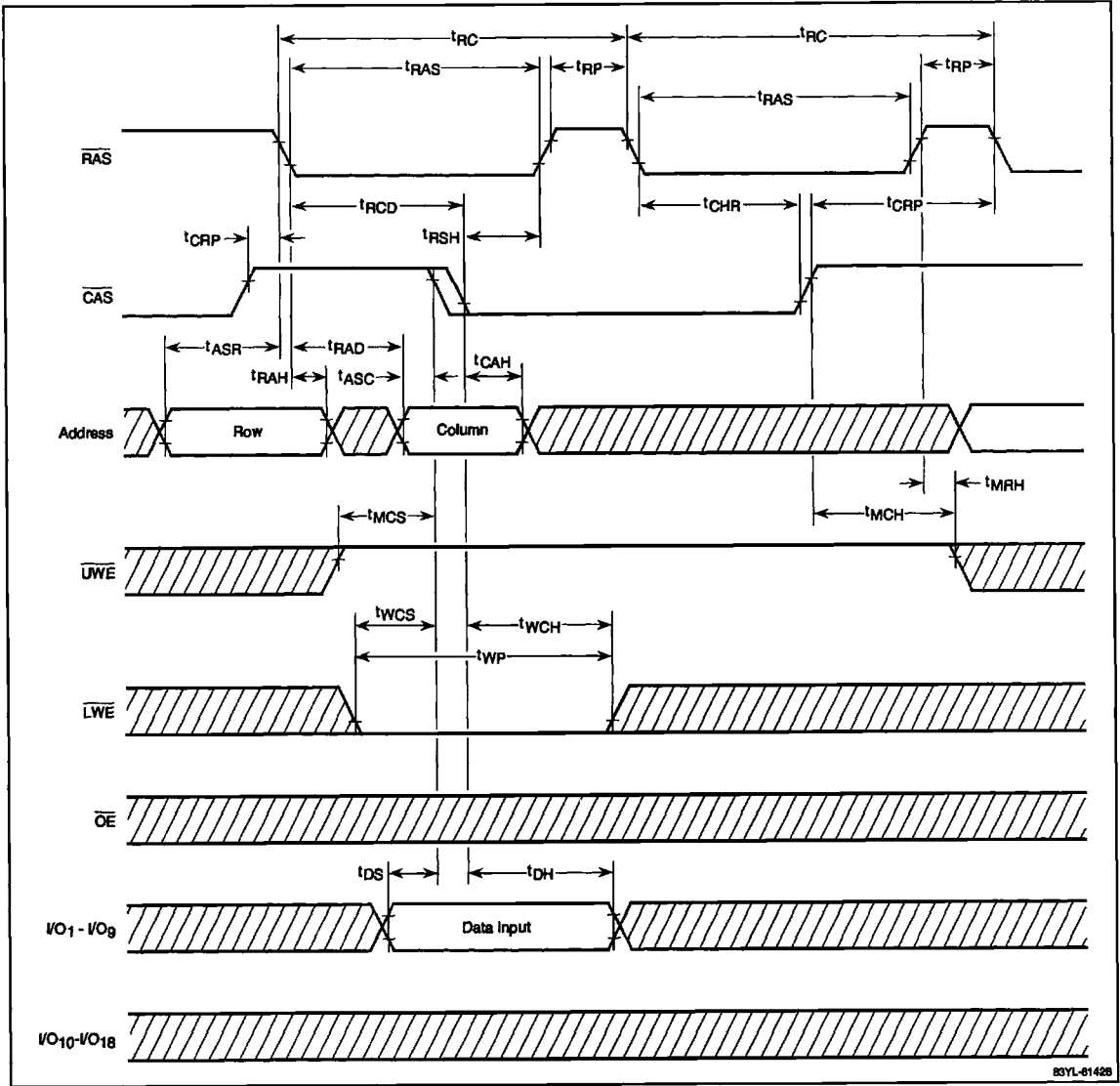
### Timing Waveforms (cont)

#### Hidden Refresh Cycle (Read Cycle)



Timing Waveforms (cont)

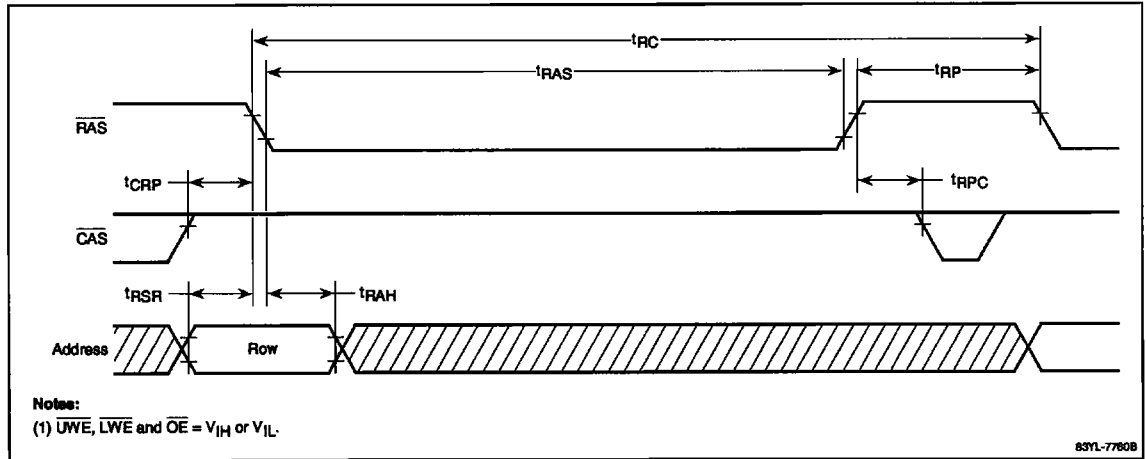
Byte Hidden-Refresh Cycle (Write)



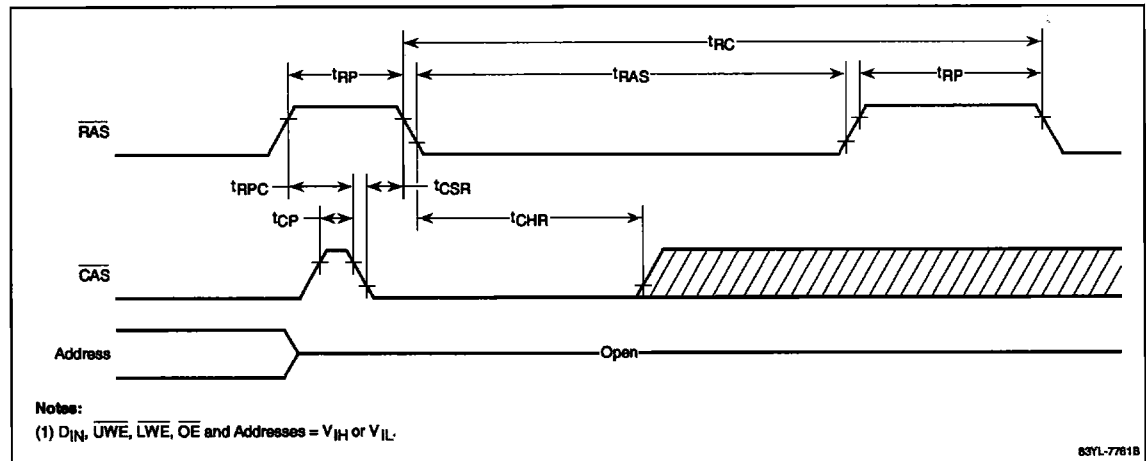


### Timing Waveforms (cont)

#### RAS Refresh Cycle



#### CAS Before RAS Refresh Cycle



Timing Waveforms (cont)

**CBR Self-Refresh Cycle**

