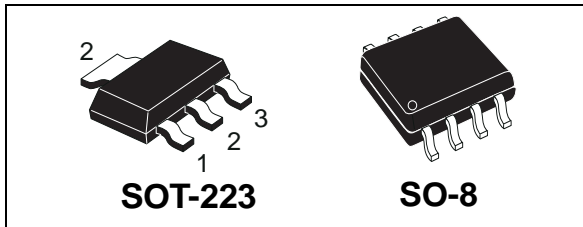


## OMNIFET III

### fully protected low-side driver

Datasheet - production data



## Description

The VNL5090N3-E and VNL5090S5-E are monolithic devices made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit.

Output current limitation protects the devices in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

## Features

Type	V <sub>clamp</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
VNL5090N3-E	41 V	90 mΩ	13 A
VNL5090S5-E			

- Automotive qualified
- Drain current: 13 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Open drain status output (Root part number 2 only)
- Specially intended for 2 x R10W or 4 x R5W automotive signal lamps

Table 1. Devices summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	VNL5090N3-E	VNL5090N3TR-E
SO-8	VNL5090S5-E	VNL5090S5TR-E

# Contents

- 1      Block diagrams and pins configurations ..... 5**
- 2      Electrical specifications ..... 8**
  - 2.1 Absolute maximum ratings ..... 8
  - 2.2 Thermal data ..... 8
  - 2.3 Electrical characteristics ..... 9
- 3      Application information ..... 13**
  - 3.1 MCU I/O protection ..... 14
- 4      Package and PC board thermal data ..... 16**
  - 4.1 SOT-223 thermal data ..... 16
  - 4.2 SO-8 thermal data ..... 19
- 5      Package and packing information ..... 22**
  - 5.1 ECOPACK® ..... 22
  - 5.2 SOT-223 mechanical data ..... 22
  - 5.3 SO-8 mechanical data ..... 23
  - 5.4 SOT-223 packing information ..... 25
  - 5.5 SO-8 packing information ..... 26
- 6      Revision history ..... 27**



## List of tables

Table 1.	Devices summary . . . . .	1
Table 2.	Pin function . . . . .	6
Table 3.	Suggested connections for unused and N.C. pins . . . . .	7
Table 4.	Absolute maximum ratings . . . . .	8
Table 5.	Thermal data . . . . .	8
Table 6.	PowerMOS section . . . . .	9
Table 7.	Source drain diode . . . . .	9
Table 8.	Input section . . . . .	9
Table 9.	Status pin . . . . .	9
Table 10.	Logic input . . . . .	10
Table 11.	Openload detection . . . . .	10
Table 12.	Supply section . . . . .	10
Table 13.	Switching characteristics . . . . .	11
Table 14.	Protection and diagnostics . . . . .	11
Table 15.	Truth table. . . . .	12
Table 16.	SOT-223 thermal parameters . . . . .	18
Table 17.	SO-8 thermal parameters . . . . .	21
Table 18.	SOT-223 mechanical data . . . . .	23
Table 19.	SO-8 mechanical data . . . . .	24
Table 20.	Document revision history . . . . .	27

## List of figures

Figure 1.	VNL5090N3-E block diagram . . . . .	5
Figure 2.	VNL5090S5-E block diagram . . . . .	5
Figure 3.	VNL5090N3-E current and voltage conventions. . . . .	6
Figure 4.	VNL5090S5-E current and voltage conventions . . . . .	6
Figure 5.	Configuration diagrams (top view) . . . . .	7
Figure 6.	Switching characteristics . . . . .	12
Figure 7.	VNL5090N3-E application schematic . . . . .	13
Figure 8.	VNL5090S5-E application schematic . . . . .	13
Figure 9.	Maximum demagnetization energy ( $V_{CC} = 16\text{ V}$ ) . . . . .	15
Figure 10.	SOT-223 PC board . . . . .	16
Figure 11.	SOT-223 Rthj-amb vs PCB copper area in open box free air condition . . . . .	16
Figure 12.	SOT-223 thermal impedance junction ambient single pulse. . . . .	17
Figure 13.	Thermal fitting model of a LSD in SOT-223 . . . . .	17
Figure 14.	SO-8 PC board . . . . .	19
Figure 15.	SO-8 Rthj-amb vs PCB copper area in open box free air condition . . . . .	19
Figure 16.	SO-8 thermal impedance junction ambient single pulse. . . . .	20
Figure 17.	Thermal fitting model of a LSD in SO-8 . . . . .	20
Figure 18.	SOT-223 package dimensions . . . . .	22
Figure 19.	SO-8 package dimensions . . . . .	23
Figure 20.	SOT-223 tape and reel shipment (suffix "TR") . . . . .	25
Figure 21.	SO-8 tube shipment (no suffix) . . . . .	26
Figure 22.	SO-8 tape and reel shipment (suffix "TR") . . . . .	26

# 1 Block diagrams and pins configurations

Figure 1. VNL5090N3-E block diagram

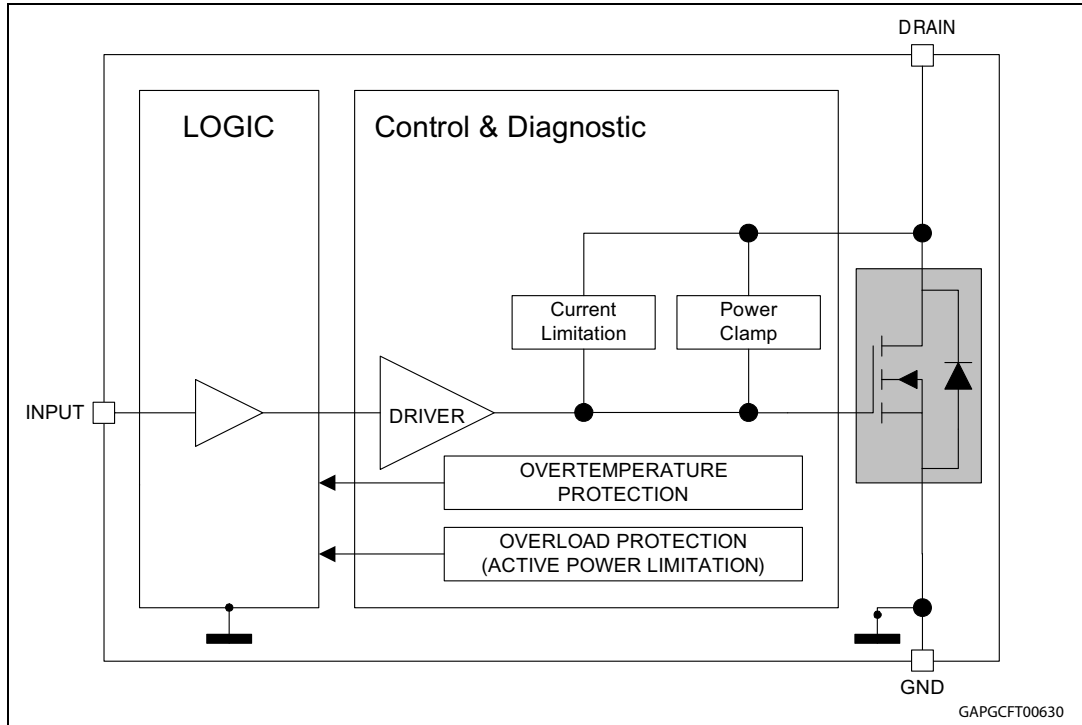


Figure 2. VNL5090S5-E block diagram

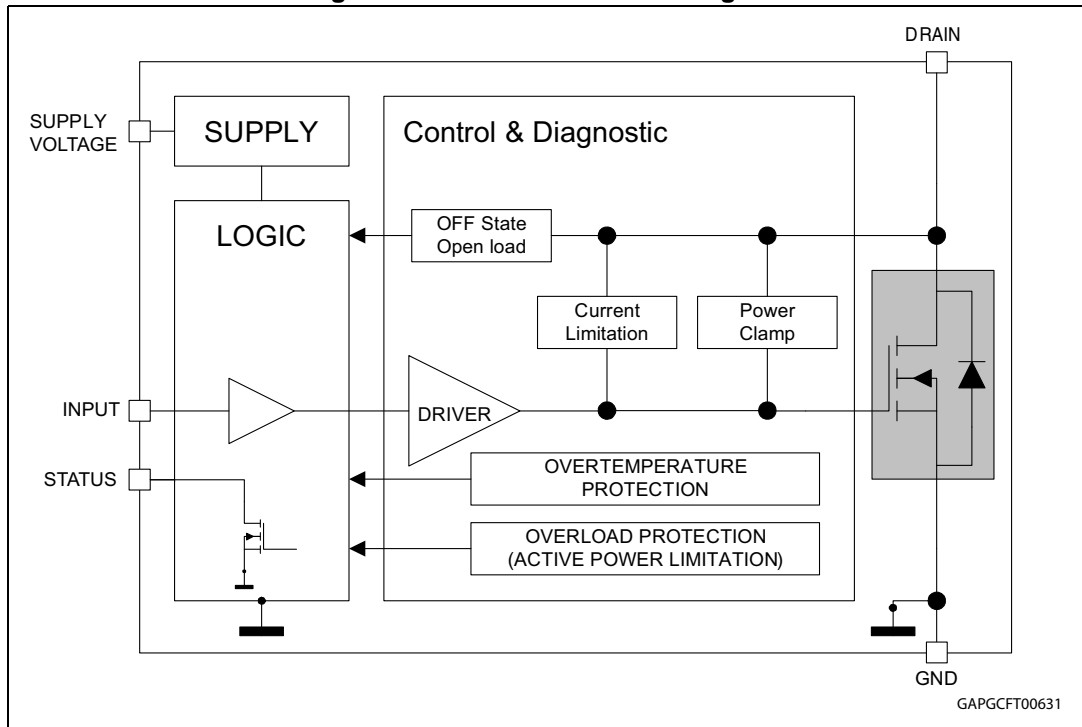


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible; It controls output switch state <sup>(1)</sup>
DRAIN	PowerMOS drain
SOURCE	PowerMOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5 V)
STATUS	Open drain digital diagnostic pin <sup>(2)</sup>

1. Internally connected to  $V_{supply}$  in the VNL5090N3-E
2. Valid for VNL5090S5-E only.

Figure 3. VNL5090N3-E current and voltage conventions

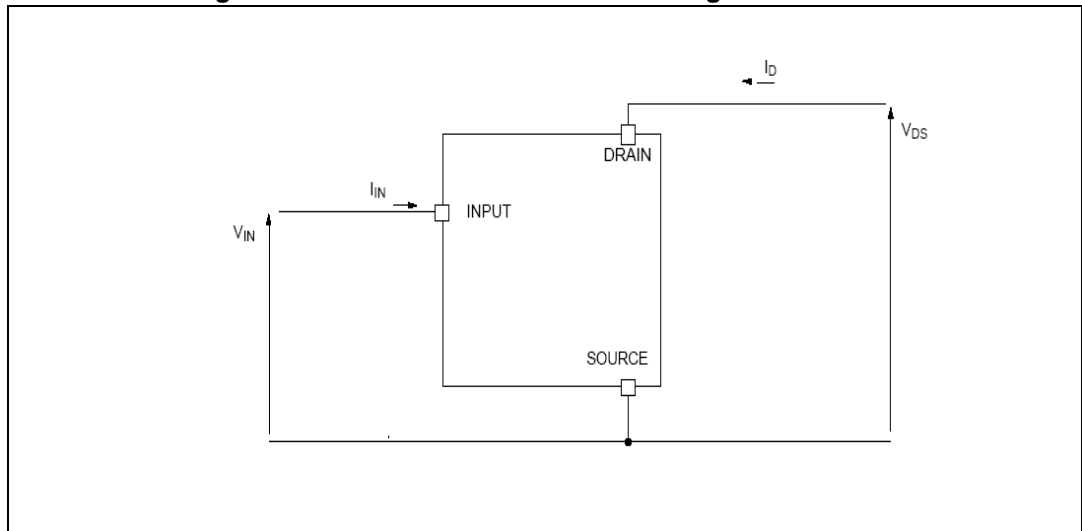


Figure 4. VNL5090S5-E current and voltage conventions

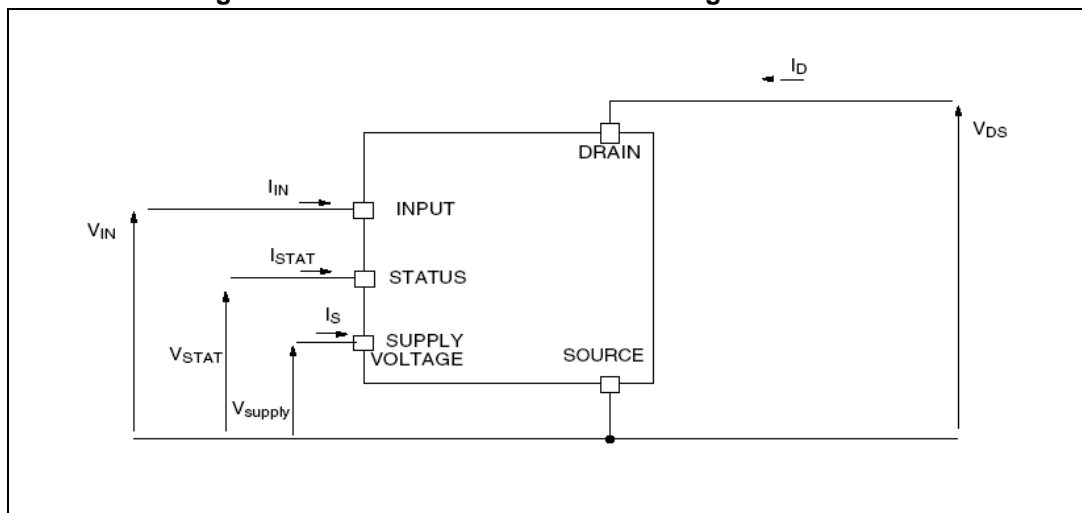


Figure 5. Configuration diagrams (top view)

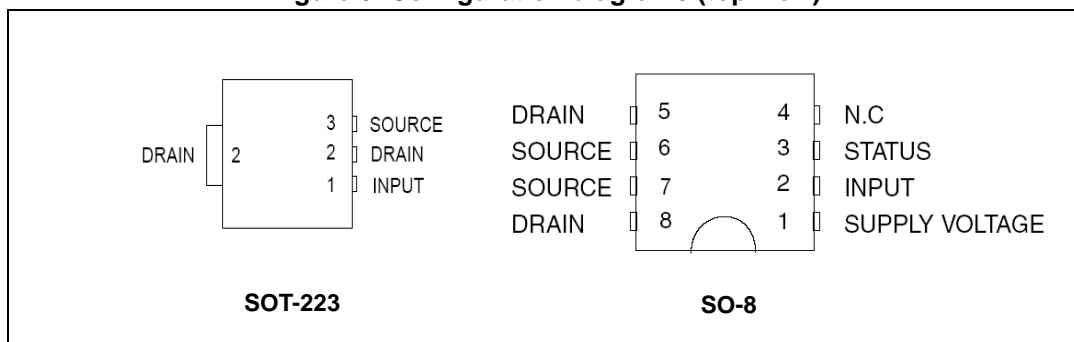


Table 3. Suggested connections for unused and N.C. pins

Connection / pin	Status	N.C.	Input
Floating	X <sup>(1)</sup>	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

1. X: do not care.

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
$V_{DS}$	Drain-source voltage ( $V_{IN} = 0\text{ V}$ )	Internally clamped		V
$I_D$	DC drain current	Internally limited		A
$-I_D$	Reverse DC drain current	12.5		A
$I_S$	DC supply current	—	-1 to 10	mA
$I_{IN}$	DC input current	-1 to 10		mA
$I_{STAT}$	DC status current	—	-1 to 10	mA
$V_{ESD1}$	Electrostatic discharge ( $R = 1.5\text{ k}\Omega$ ; $C = 100\text{ pF}$ )			
	–D RAIN	5000		V
	– SUPPLY, INPUT, STATUS	4000		V
$V_{ESD2}$	Electrostatic discharge on output pin only ( $R = 330\ \Omega$ , $C = 150\text{ pF}$ )	2000		V
$T_j$	Junction operating temperature	-40 to 150		°C
$T_{stg}$	Storage temperature	-55 to 150		°C
$E_{AS}$	Single pulse avalanche energy ( $L = 1.1\text{ mH}$ , $T_j = 150^\circ\text{C}$ , $R_L = 0$ , $I_{OUT} = I_{limL}$ )	50		mJ

### 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Maximum value		Unit
		SOT-223	SO-8	
$R_{thj-amb}$	Thermal resistance junction-ambient	147 <sup>(1)</sup>	102	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm<sup>2</sup> of Cu (at least 35  $\mu\text{m}$  thick) connected to all DRAIN pins



## 2.3 Electrical characteristics

Values specified in this section are for  $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise stated.

**Table 6. PowerMOS section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{supply}}$	Operating supply voltage		3.5	5	5.5	V
$R_{\text{ON}}$	ON-state resistance	$I_D = 1.6 \text{ A}; T_j = 25^\circ\text{C}; V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$			90	m $\Omega$
		$I_D = 1.6 \text{ A}; T_j = 150^\circ\text{C}; V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$			180	
		$I_D = 1.6 \text{ A}; T_j = 150^\circ\text{C}; V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}^{(1)}$			190	
$V_{\text{CLAMP}}$	Drain-source clamp voltage	$V_{\text{IN}} = 0 \text{ V}; I_D = 1.6 \text{ A}$	414	65	2	V
$V_{\text{CLTH}}$	Drain-source clamp threshold voltage	$V_{\text{IN}} = 0 \text{ V}; I_D = 2 \text{ mA}$	36			V
$I_{\text{DSS}}$	OFF-state output current	$V_{\text{IN}} = 0 \text{ V}; V_{\text{DS}} = 13 \text{ V}; T_j = 25^\circ\text{C}$	03			$\mu\text{A}$
		$V_{\text{IN}} = 0 \text{ V}; V_{\text{DS}} = 13 \text{ V}; T_j = 125^\circ\text{C}$	05			

1. Valid only for VNL5090N3-E.

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{SD}}$	Forward on voltage	$I_D = 1.6 \text{ A}; V_{\text{IN}} = 0 \text{ V}$	—	0.8	—	V

**Table 8. Input section<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{\text{ISS}}$	Supply current from input pin	ON-state: $V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}; V_{\text{DS}} = 0 \text{ V}$		30	65	$\mu\text{A}$
$V_{\text{ICL}}$	Input clamp voltage	$I_S = 1 \text{ mA}$	5.5		7	V
		$I_S = -1 \text{ mA}$		-0.7		
$V_{\text{INTH}}$	Input threshold voltage	$V_{\text{DS}} = V_{\text{IN}}; I_D = 1 \text{ mA}$	1		3.5	V

1. Valid for VNL5090N3-E option (input and supply pins connected together)

**Table 9. Status pin<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{STAT}}$	Status low output voltage	$I_{\text{STAT}} = 1 \text{ mA}$			0.5	V
$I_{\text{LSTAT}}$	Status leakage current	Normal operation, $V_{\text{STAT}} = 5 \text{ V}$			10	$\mu\text{A}$

Table 9. Status pin<sup>(1)</sup> (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>STAT</sub>	Status pin input capacitance	Normal operation, V <sub>STAT</sub> = 5 V			100	pF
V <sub>STCL</sub>	Status clamp voltage	I <sub>STAT</sub> = 1 mA	5.5		7	V
		I <sub>STAT</sub> = -1 mA		-0.7		

1. Valid for VNL5090S5-E option

Table 10. Logic input<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Low-level input voltage				0.9	V
I <sub>IL</sub>	Low-level input current	V <sub>IN</sub> = 0.9 V	1			μA
V <sub>IH</sub>	High-level input voltage		2.1			V
I <sub>IH</sub>	High-level input current	V <sub>IN</sub> = 2.1 V			10	μA
V <sub>I(hyst)</sub>	Input hysteresis voltage		0.13			V
V <sub>ICL</sub>	Input clamp voltage	I <sub>IN</sub> = 1 mA	5.5		7	V
		I <sub>IN</sub> = -1 mA		-0.7		

1. Valid for VNL5090S5-E option

Table 11. Openload detection<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>OI</sub>	Openload OFF-state voltage detection threshold	V <sub>IN</sub> = 0 V	0.6	1.2	1.7	V
t <sub>d(oloff)</sub>	Delay between INPUT falling edge and STATUS falling edge in openload condition	I <sub>OUT</sub> = 0 A	45	425	1100	μs

1. Valid for VNL5090S5-E option

Table 12. Supply section<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Supply current	OFF-state; T <sub>j</sub> = 25°C; V <sub>IN</sub> = V <sub>DRAIN</sub> = 0 V;		10	25	μA
		ON-state; V <sub>IN</sub> = 5 V; V <sub>DS</sub> = 0 V		25	65	
V <sub>SCL</sub>	Supply clamp voltage	I <sub>SCL</sub> = 1 mA	5.5		7	V
		I <sub>SCL</sub> = -1 mA		-0.7		

1. Valid for VNL5090S5-E option

Table 13. Switching characteristics<sup>(1)</sup>

Symbol	Parameter	Test conditions	SOT-223 <sup>(2)</sup>			SO-8			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on delay time	$R_L = 8.2 \Omega$ , $V_{CC} = 13 V^{(3)}$	—8	—	—	—	8	—	$\mu s$
$t_{d(OFF)}$	Turn-off delay time	$R_L = 8.2 \Omega$ , $V_{CC} = 13 V^{(3)}$	—3	.4	—	—	18	—	$\mu s$
$t_r$	Rise time	$R_L = 8.2 \Omega$ , $V_{CC} = 13 V^{(3)}$	—1	0	—	—	10	—	$\mu s$
$t_f$	Fall time	$R_L = 8.2 \Omega$ , $V_{CC} = 13 V^{(3)}$	—2	.7	—	—	10	—	$\mu s$
$W_{ON}$	Switching energy losses at turn-on	$R_L = 8.2 \Omega$ , $V_{CC} = 13 V^{(3)}$	—5	7	—	—	57	—	$\mu J$
$W_{OFF}$	Switching energy losses at turn-off	$R_L = 8.2 \Omega$ , $V_{CC} = 13 V^{(3)}$	—1	4	—	—	55	—	$\mu J$

1. See [Figure 7: VNL5090N3-E application schematic](#) and [Figure 8: VNL5090S5-E application schematic](#)
2.  $3.5 V \leq V_{supply} = V_{IN} \leq 5.5 V$
3. See [Figure 6: Switching characteristics](#)

Table 14. Protection and diagnostics

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$I_{limH}$	DC short-circuit current	$V_{DS} = 13 V$ ; $V_{supply} = V_{IN} = 5 V$	13	18	25	A
$I_{limL}$	Short-circuit current during thermal cycling	$V_{DS} = 13 V$ ; $T_R < T_j < T_{TSD}$ ; $V_{supply} = V_{IN} = 5 V$		8A		
$t_{dimL}$	Step response current limit	$V_{DS} = 13 V$ ; $V_{input} = 5 V$		44		$\mu s$
$T_{TSD}$	Shutdown temperature		150	175	200	$^{\circ}C$
$T_R^{(2)}$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
$T_{RS}^{(3)}$	Thermal reset of STATUS		135			$^{\circ}C$
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			$7^{\circ}$		C

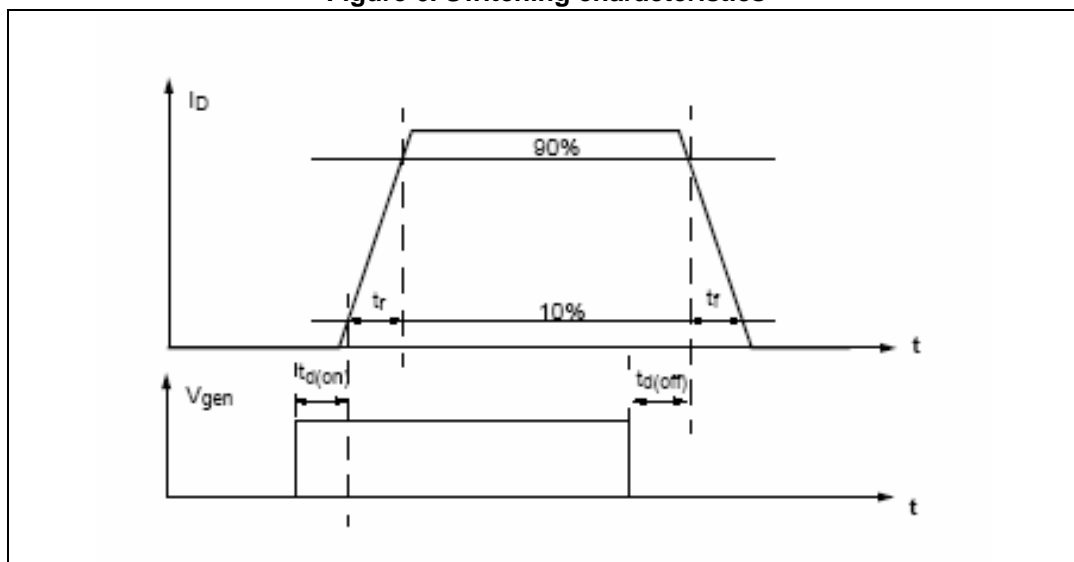
1.  $V_{supply} = V_{input}$  in VNL5090N3-E version.
2. Valid for VNL5090S5-E option.

Table 15. Truth table<sup>(1)</sup>

Conditions	INPUT	DRAIN	STATUS
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Overtemperature	L	H	H
	H	H	L
Undervoltage	L	H	X
	H	H	X
Output voltage < $V_{OL}$	L	L	L
	H	L	H

1. Valid for VNL5090S5-E option

Figure 6. Switching characteristics



### 3 Ap plication information

Figure 7. VNL5090N3-E application schematic

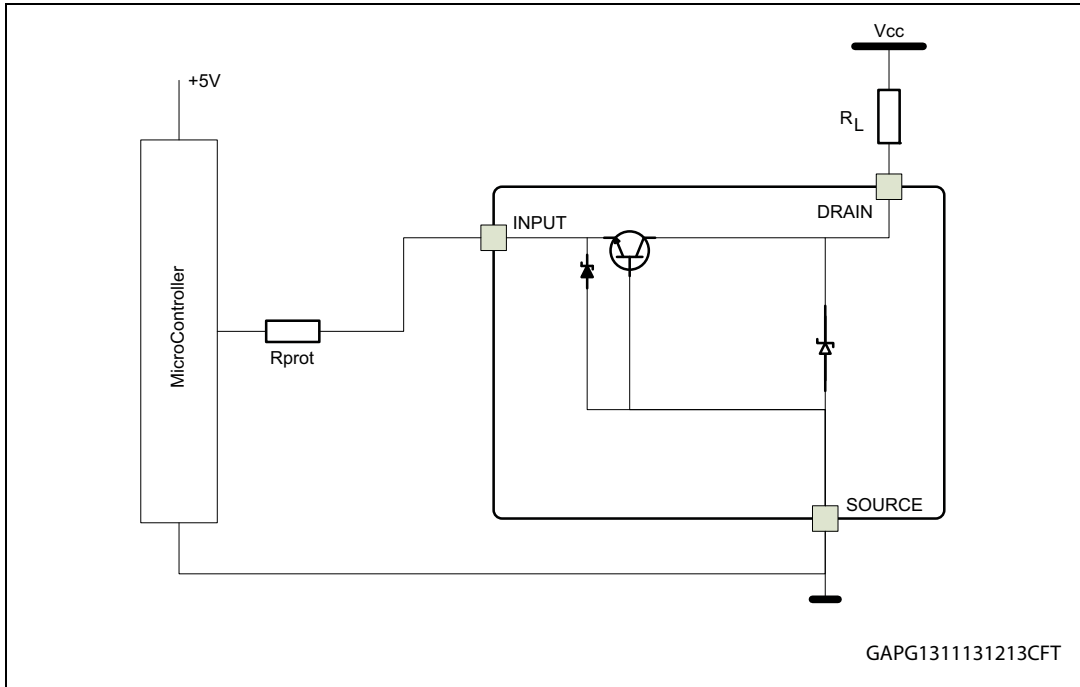
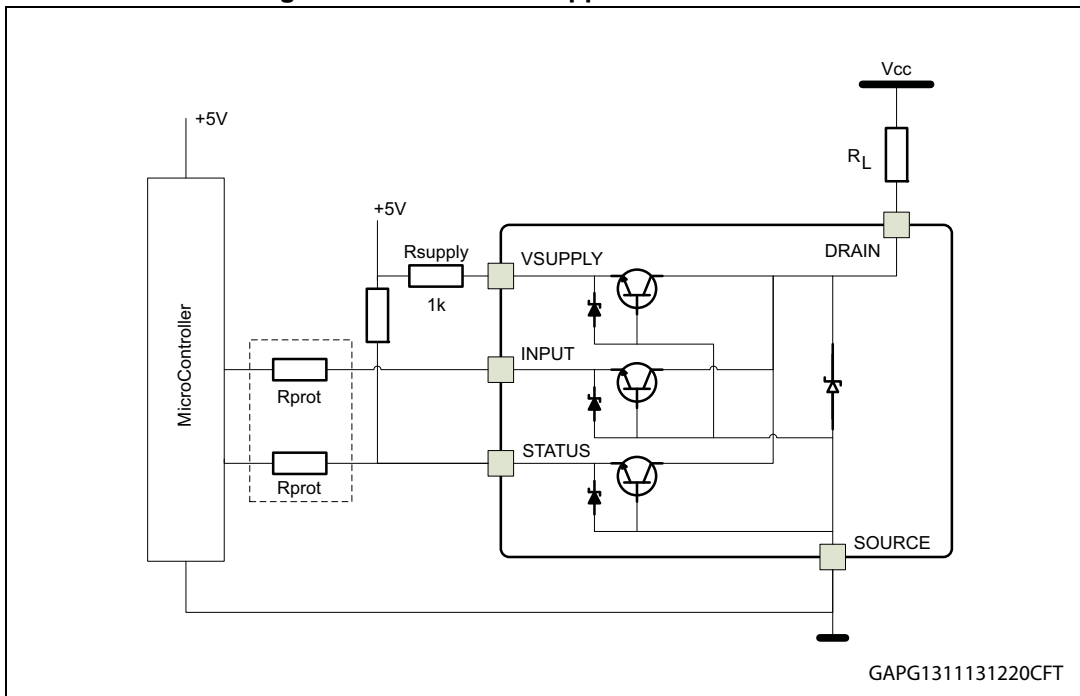


Figure 8. VNL5090S5-E application schematic



### 3.1 MCU I/O protection

ST suggests to insert a resistor ( $R_{\text{prot}}$ ) in line to prevent the microcontroller I/O pins from latching up<sup>(a)</sup>. The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

#### Equation 1

$$\frac{0.7}{I_{\text{latchup}}} \leq R_{\text{prot}} \leq \frac{(V_{\text{OH}\mu\text{C}} - V_{\text{IH}})}{I_{\text{IH max}}}$$

Let:

- $I_{\text{latchup}} \geq 20 \text{ mA}$
- $V_{\text{OH}\mu\text{C}} \geq 4.5 \text{ V}$
- $35 \Omega \leq R_{\text{prot}} \leq 100 \text{ K}\Omega$

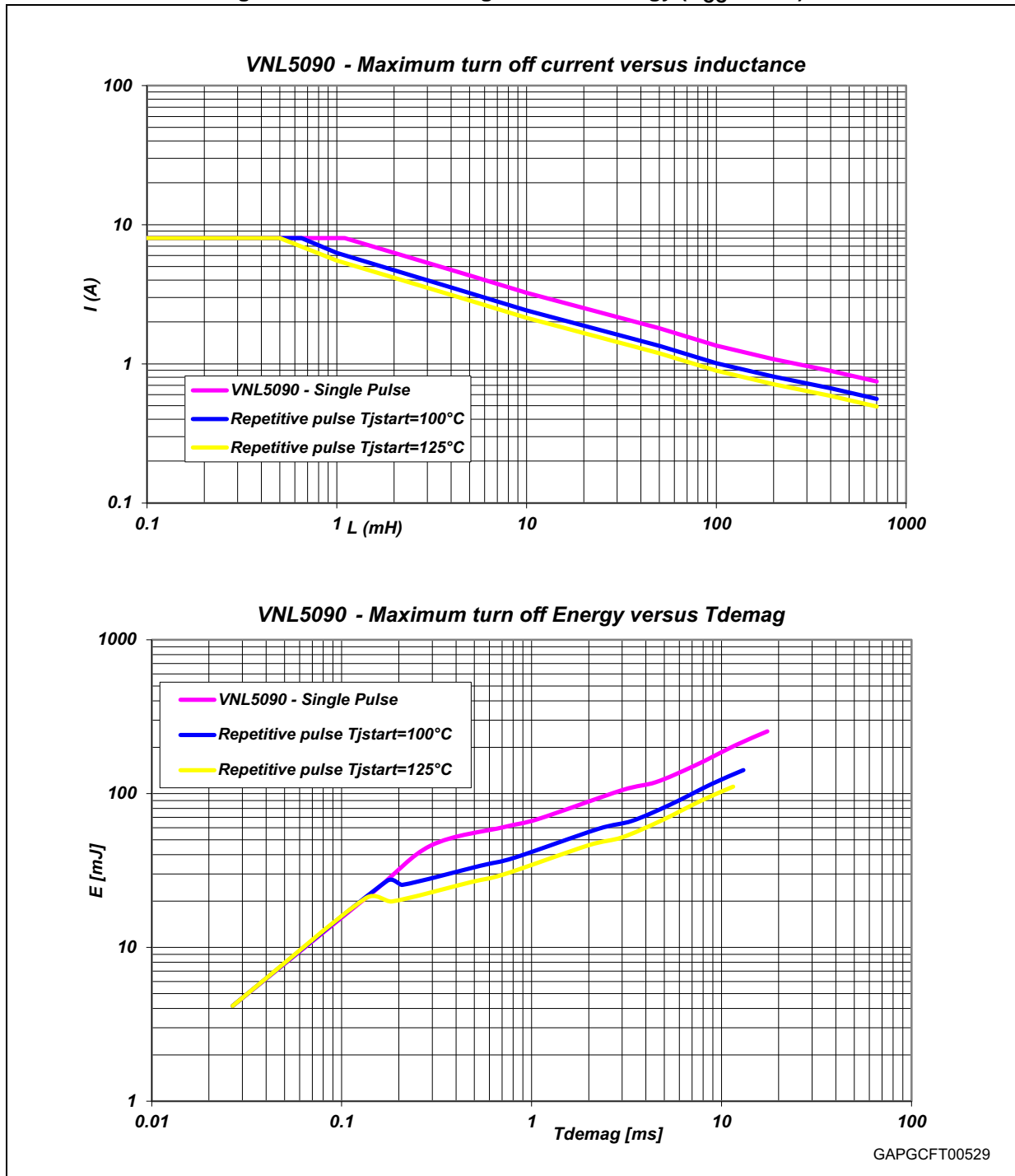
Then, the recommended value is  $R_{\text{prot}} = 1 \text{ K}\Omega$

[Figure 9](#) shows the turn-off current drawn during the demagnetization.

---

a. In case of negative transient on the drain pin.

Figure 9. Maximum demagnetization energy ( $V_{CC} = 16\text{ V}$ )

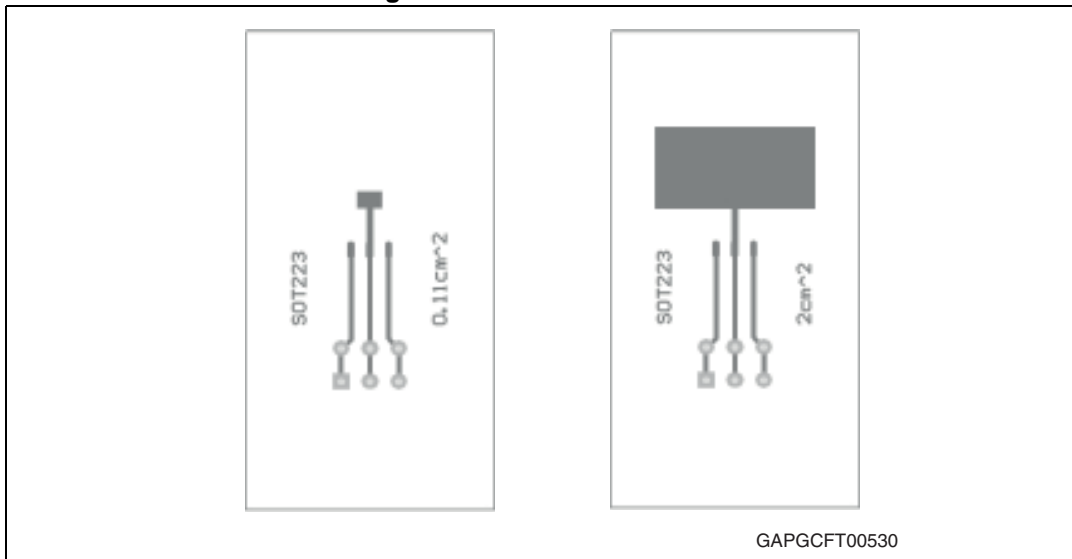


1. The voltage supply is  $V_{CC} = 13.5\text{ V}$ .

## 4 Package and PC board thermal data

### 4.1 SOT-223 thermal data

Figure 10. SOT-223 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 30 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35  $\mu$ m, copper areas: from minimum pad lay-out to 0.8 cm<sup>2</sup>).

Figure 11. SOT-223  $R_{thj-amb}$  vs PCB copper area in open box free air condition

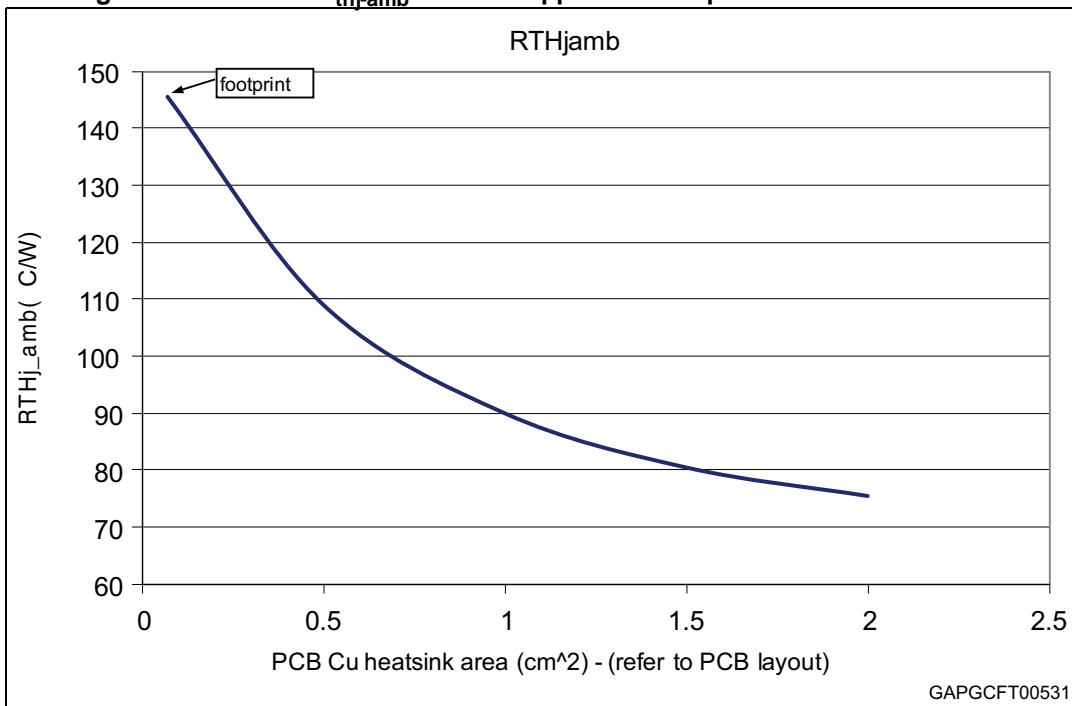
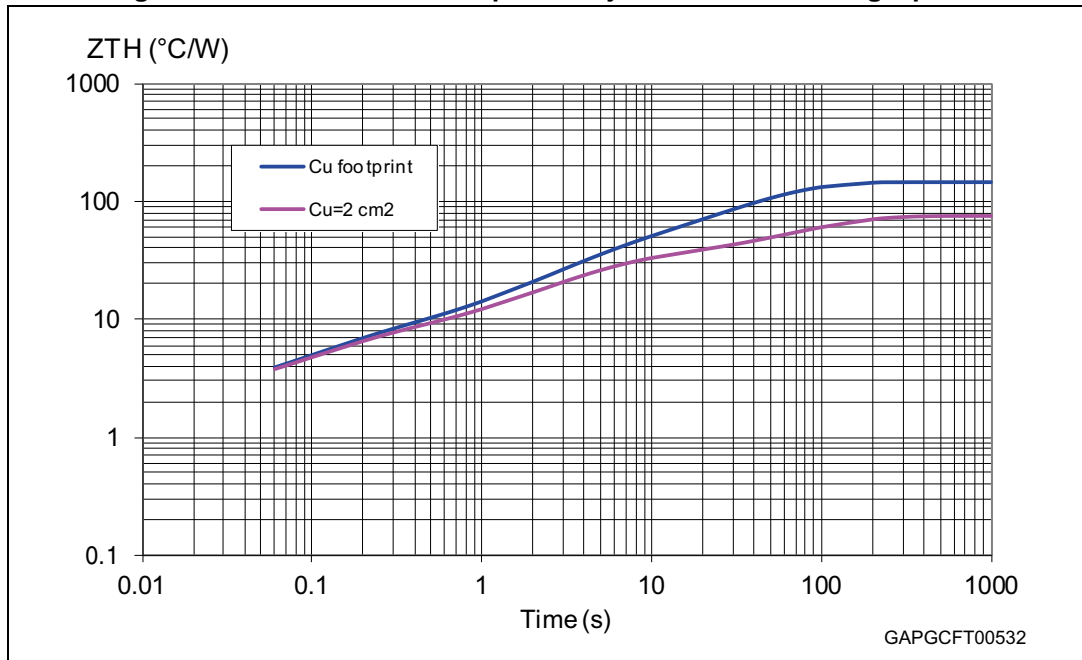




Figure 12. SOT-223 thermal impedance junction ambient single pulse

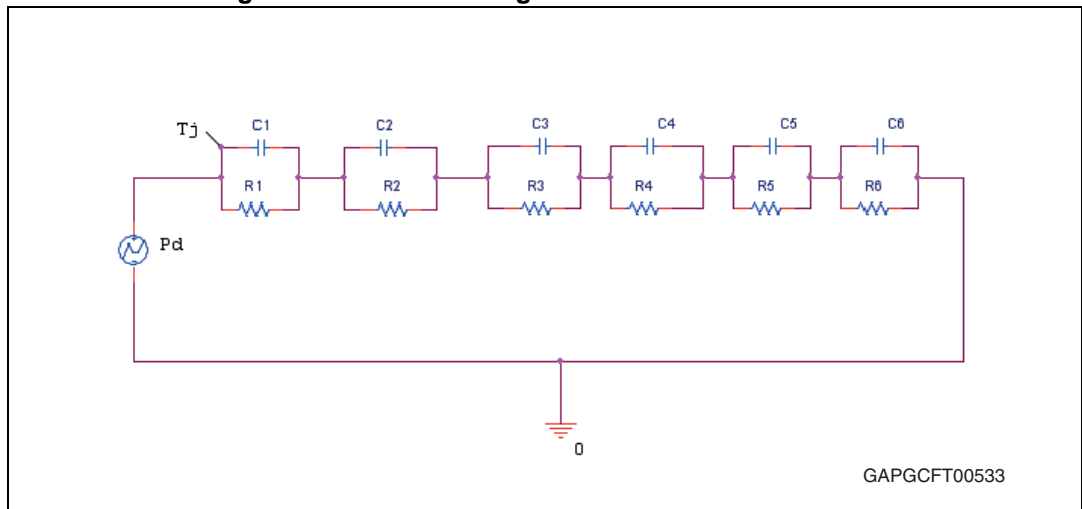


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 13. Thermal fitting model of a LSD in SOT-223



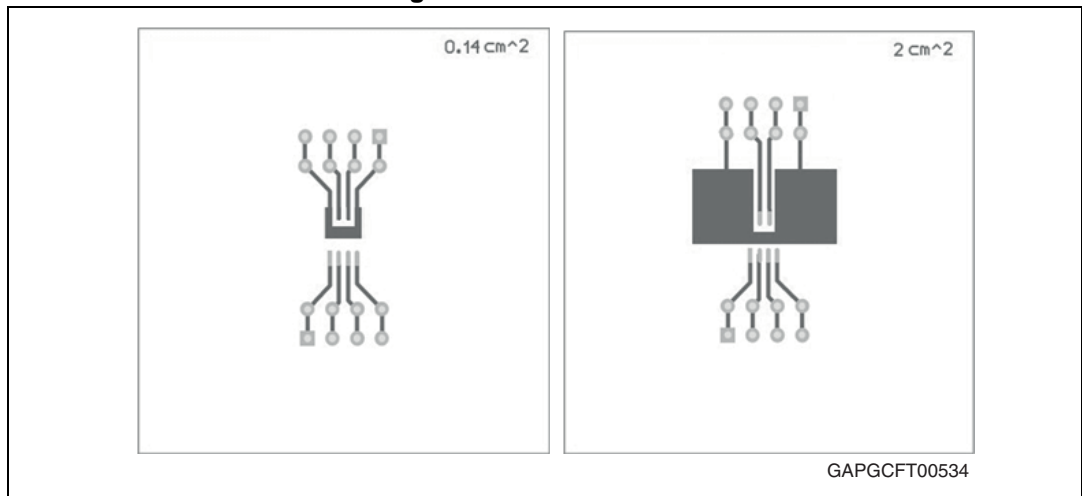
Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SOT-223 thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	0.8	
R2 (°C/W)	1	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	115	45
C1 (W.s/°C)	0.00004	
C2 (W.s/°C)	0.0003	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.16	
C5 (W.s/°C)	1000	
C6 (W.s/°C)	0.4	2

### 4.2 SO-8 thermal data

Figure 14. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 2 cm<sup>2</sup>).

Figure 15. SO-8  $R_{thj-amb}$  vs PCB copper area in open box free air condition

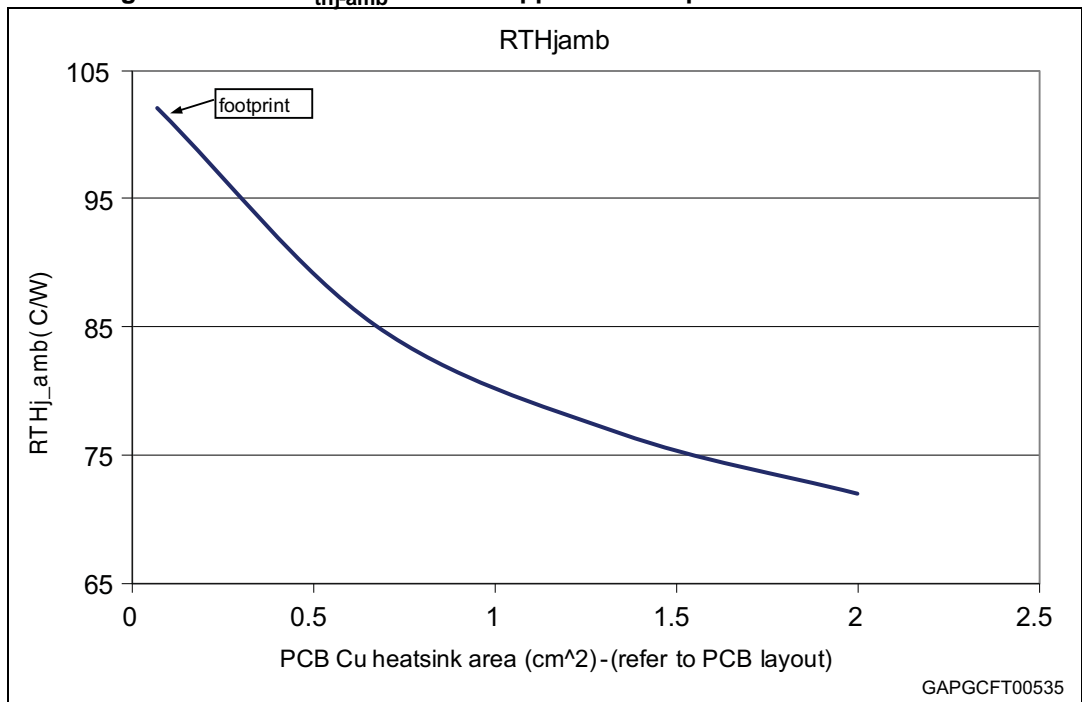
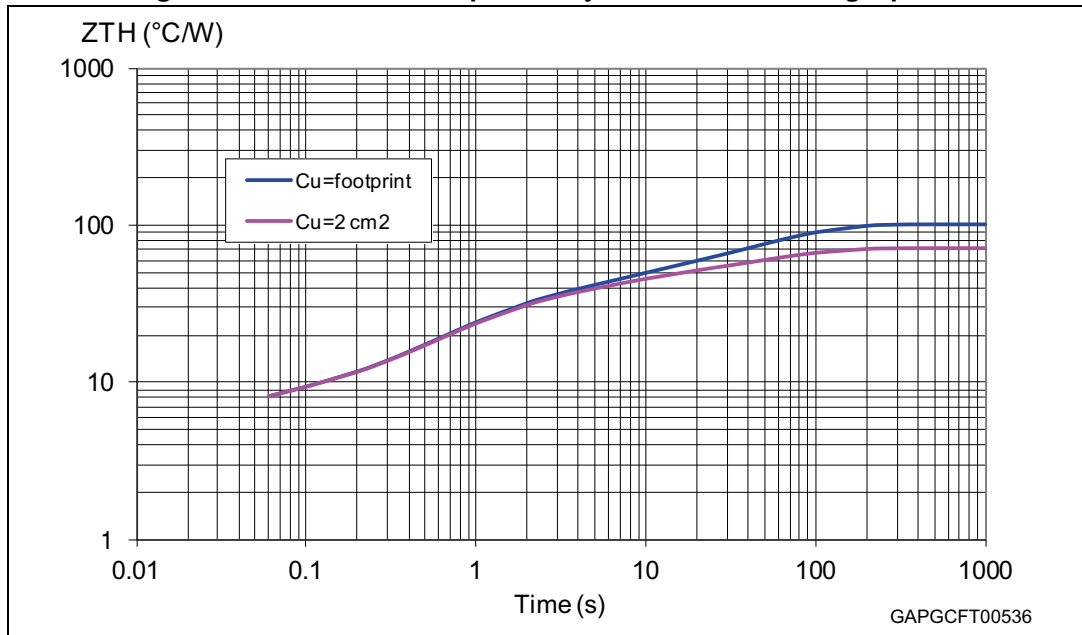


Figure 16. SO-8 thermal impedance junction ambient single pulse

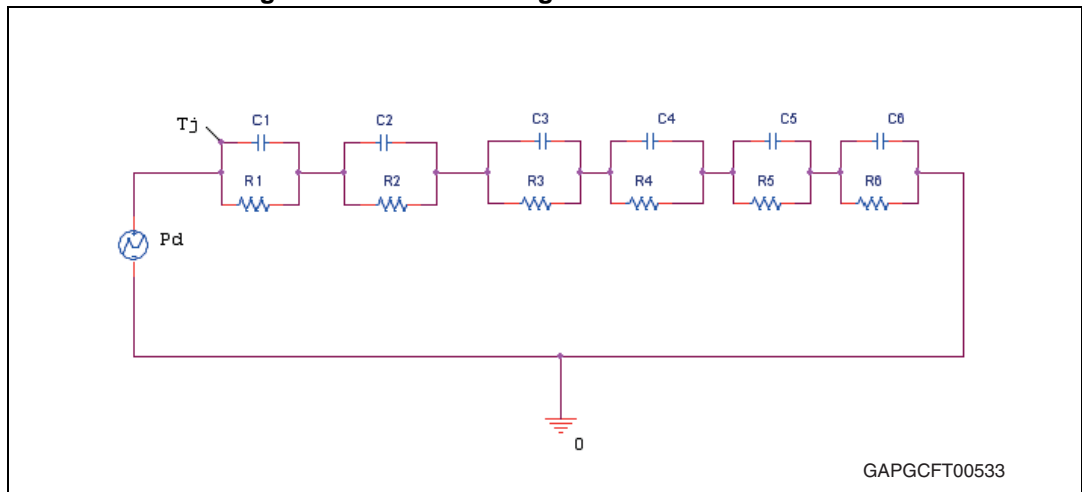


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 17. Thermal fitting model of a LSD in SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. SO-8 thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	0.8	
R2 (°C/W)	2.7	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00005	
C2 (W.s/°C)	0.001	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> ACK<sup>®</sup>

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 5.2 SOT -223 mechanical data

Figure 18. SOT-223 package dimensions

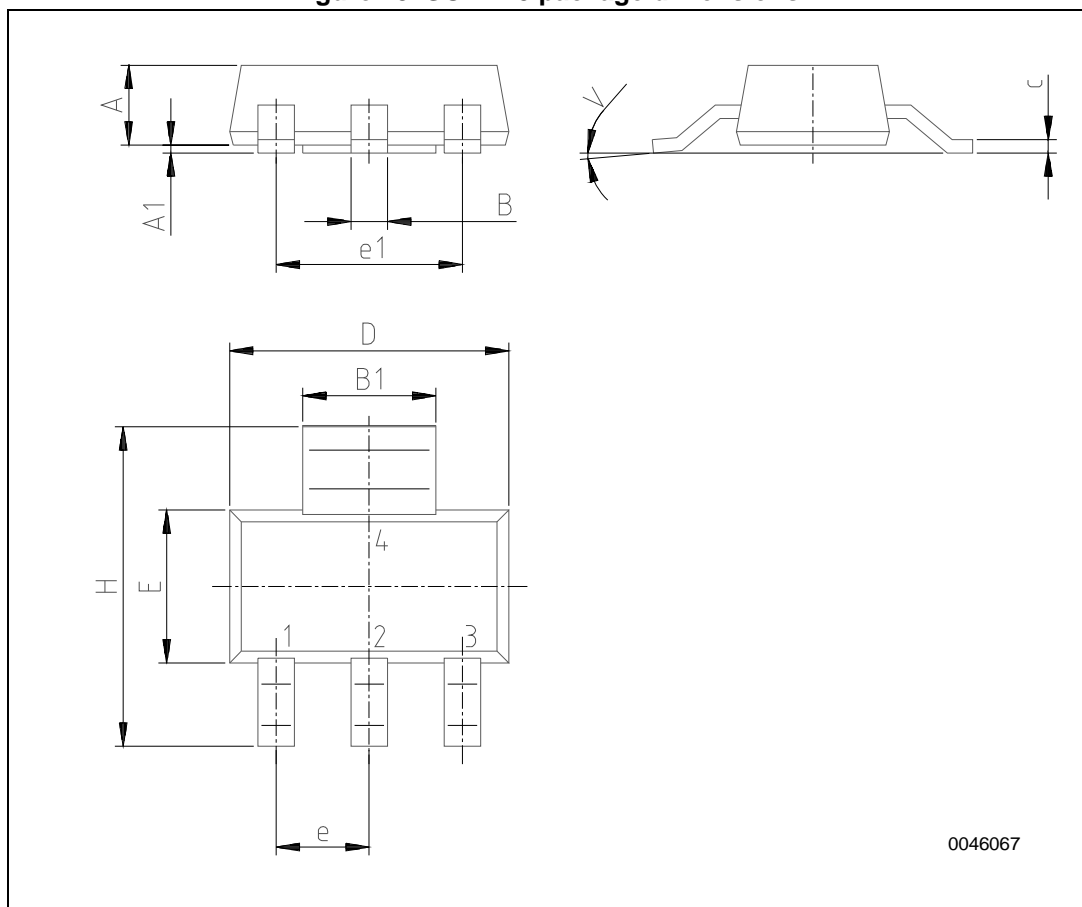


Table 18. SOT-223 mechanical data

DIM.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1			.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e2		.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10 (max)					
A1	0.02		0.1	0.0008		0.004

5.3 SO-8 mechanical data

Figure 19. SO-8 package dimensions

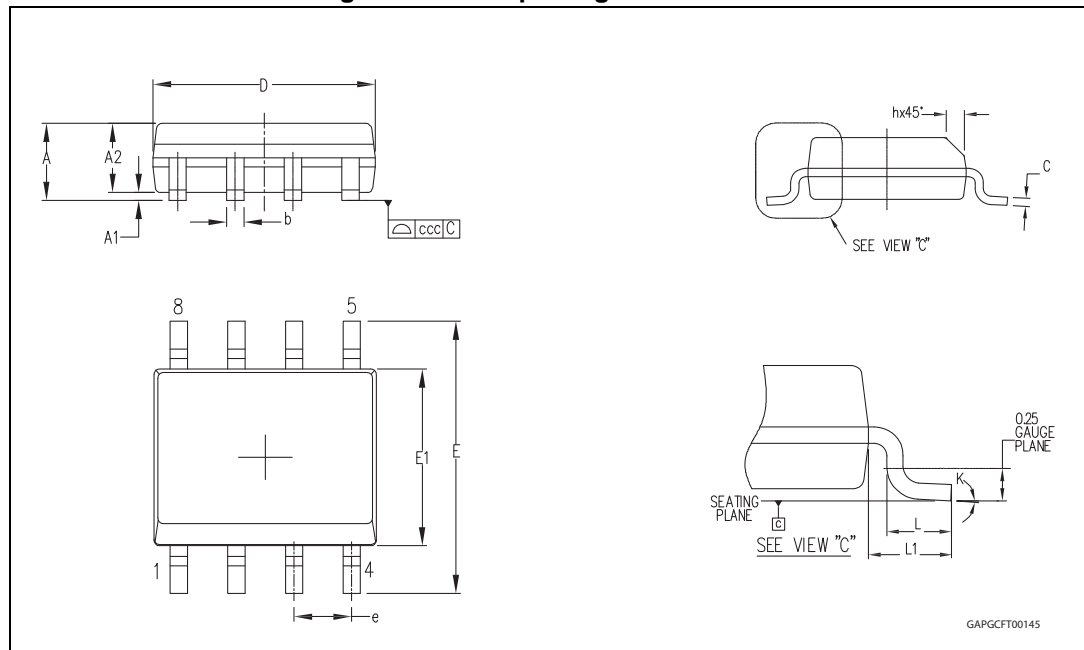


Table 19. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b0	.28		0.48
c0	.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e1		.27	
h0	.25		0.50
L0	.40		1.27
L1		1.04	
k0	°		8°
ccc			0.10

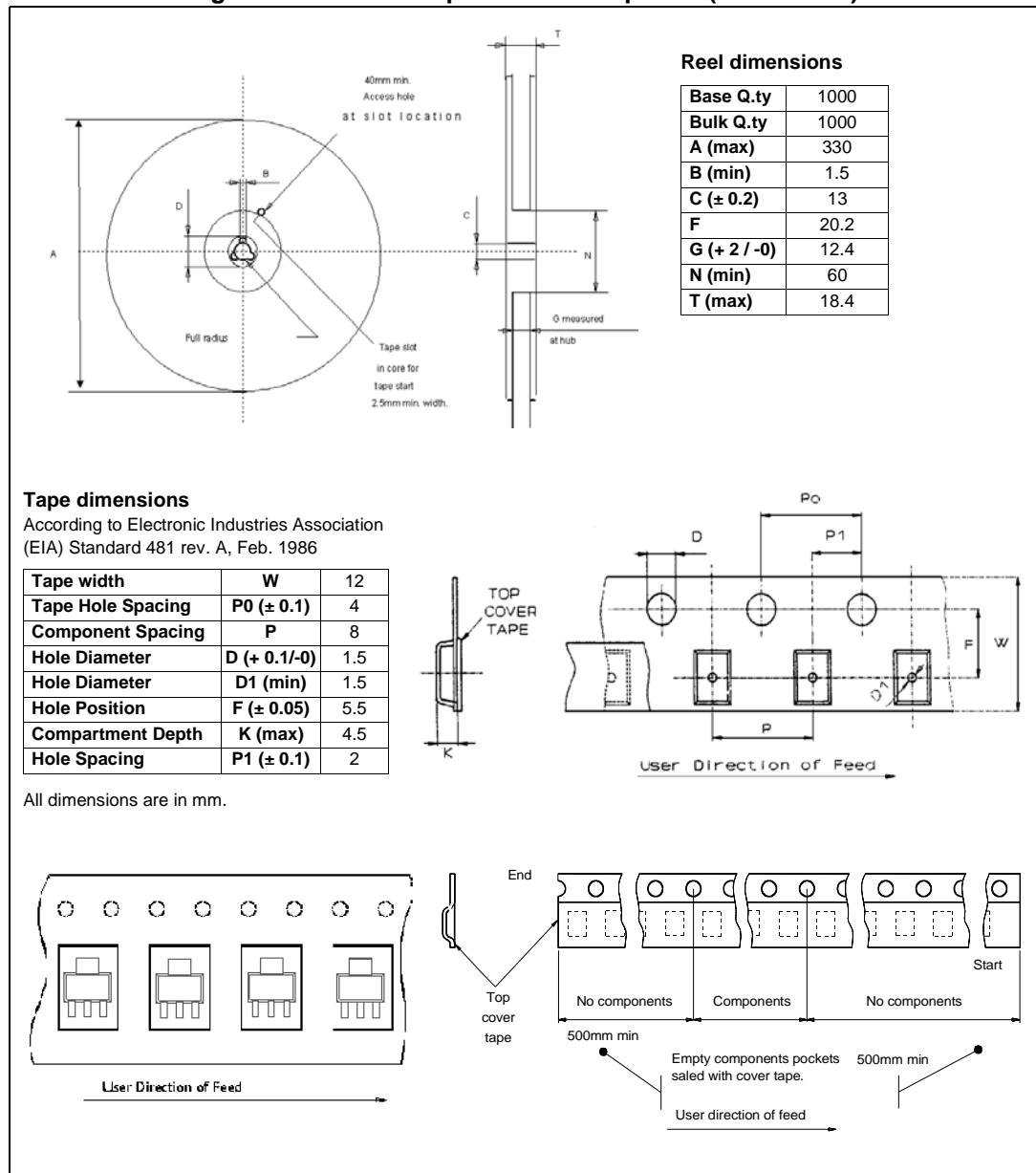
1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.



### 5.4 SOT-223 packing information

The devices can be packed in tube or tape and reel shipments (see the [Table 1: Devices summary on page 1](#)).

Figure 20. SOT-223 tape and reel shipment (suffix "TR")



### 5.5 SO-8 packing information

Figure 21. SO-8 tube shipment (no suffix)

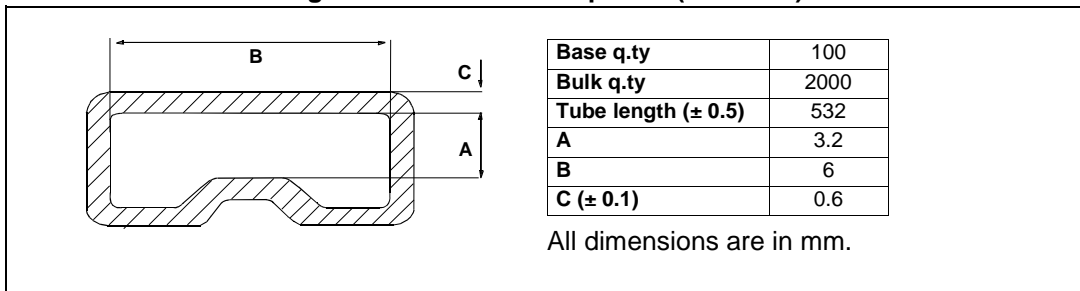
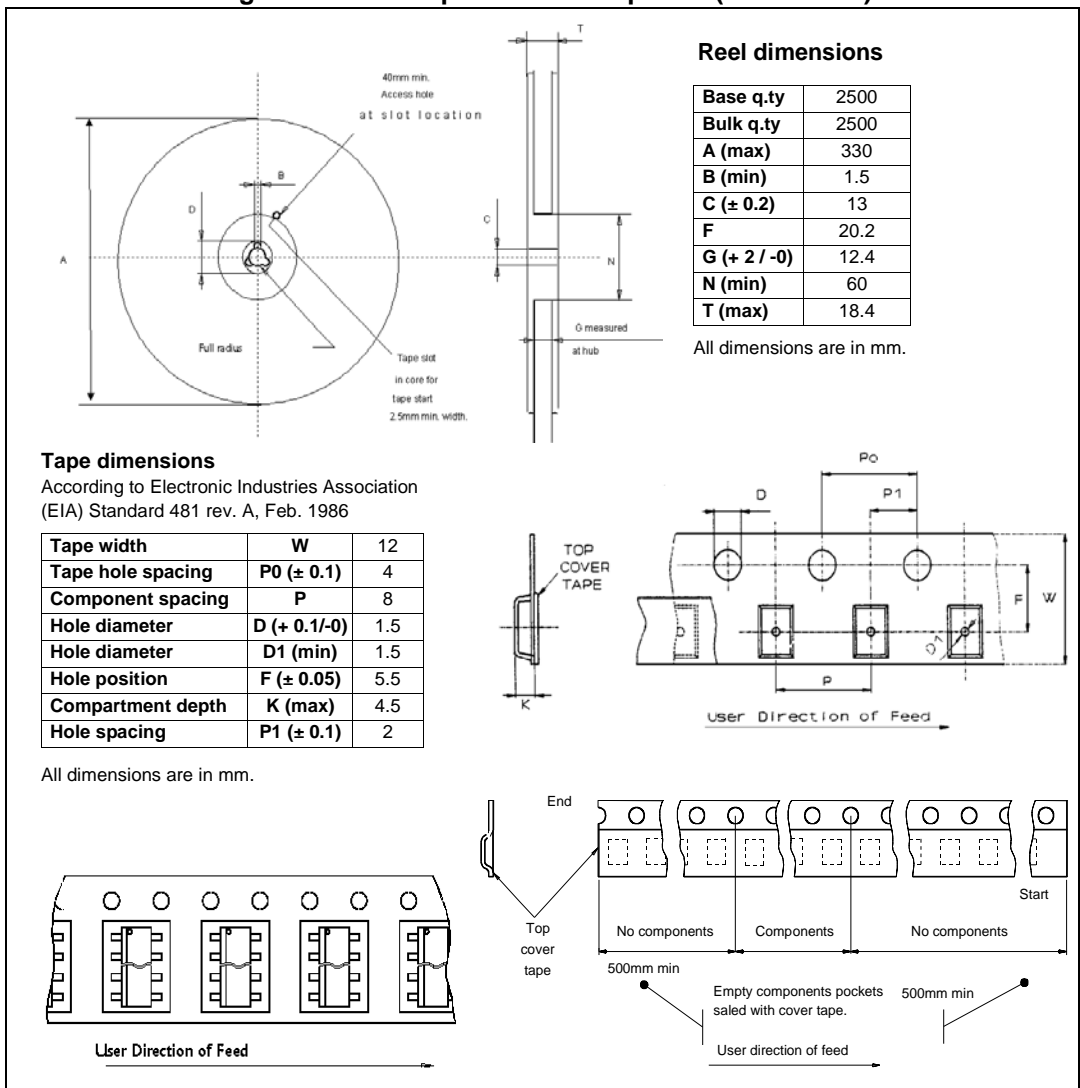


Figure 22. SO-8 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 20. Document revision history**

Date	Revision	Changes
15-Dec-2011	1	Initial release.
20-Jan-2012	2	<i>Table 4: Absolute maximum ratings:</i> -- I <sub>D</sub> : updated value
18-Apr-2012	3	Updated <i>Features</i> list
10-Aug-2012	4	Updated <i>Table 13: Switching characteristics</i>
18-Sep-2013	5	Updated disclaimer.
13-Nov-2013	6	Updated <i>Features</i> list <i>Table 8: Input section:</i> -I <sub>ISS</sub> : updated maximum value <i>Table 12: Supply section:</i> -I <sub>IS</sub> : updated maximum value Updated <i>Figure 7: VNL5090N3-E application schematic</i> and <i>Figure 8: VNL5090S5-E application schematic</i> Updated <i>Section 3.1: MCU I/O protection</i>

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)