TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73S8023C
Demo Board User Manual

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Table of Contents

Figures

Tables

1 Introduction

The 73S8023C Demo Board is a platform for evaluating the Teridian 73S8023C Smart Card Interface device. The board incorporates the 73S8023C integrated circuit and has been designed to operate either as a standalone platform (to be used in conjunction with an external microcontroller) or as a daughter card to be used in conjunction with the 73S1121F evaluation platform.

The board has been designed to comply with the EMV 2000 Specification, Version 4.0. 73S8023C Demo Boards can easily be modified to comply with NDS specifications by replacing a few external components that are highlighted in this document.

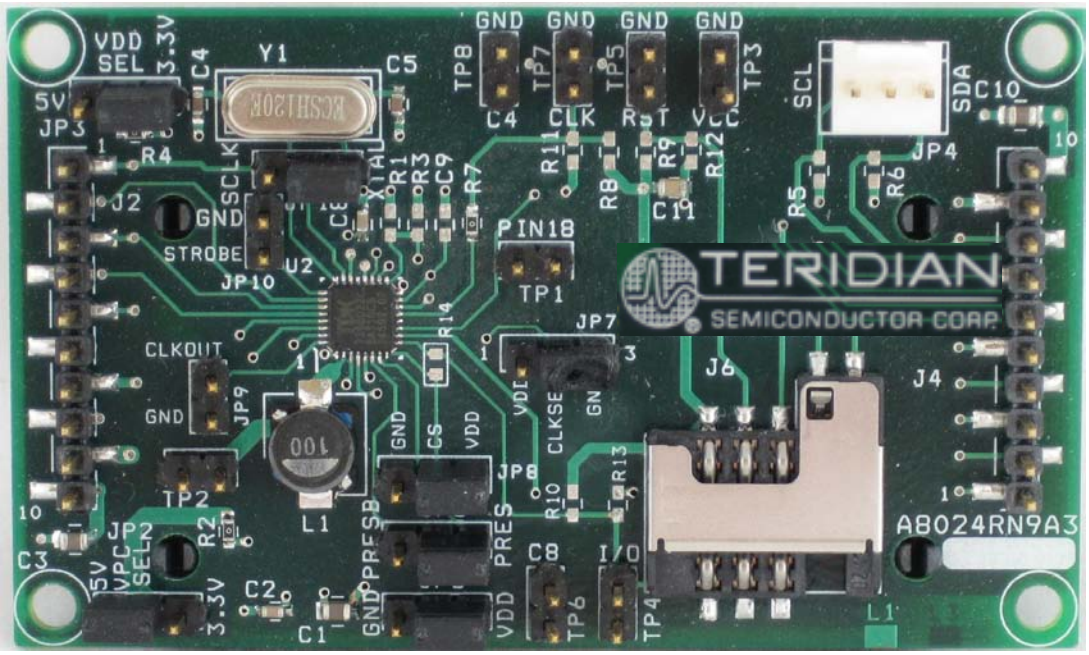

Figure 1: 73S8023C Demo Board

1.1 Package Contents

The 73S8023C Demo Board Kit includes:

- A 73S8023C Demo Board
- The following documents on CD:
  - *73S8023C Data Sheet*
  - *73S8023C Demo Board User Manual* (this document)
  - *Application Note*

1.2 Safety and ESD Notes

Connecting live voltages to the 73S8023C Demo Board system will result in potentially hazardous voltages on the boards.

Extreme caution should be taken when handling the 73S8023C Demo Board after connection to live voltages!

The 73S8023C Demo Board is ESD sensitive! ESD precautions should be taken when handling this board!

2 Basic Connections

The basic connections to the demo board are described below and shown in Figure 2.

1. Connect power supply: Apply 3.3 V to pin 10 of J4.
2. Control signals to the device can be connected through J2 and J4 (see Figure 2 and the Electrical Schematic, Figure 5).
3. To set the clock frequency with an external clock source:
   - Set JP1 to the SCLK setting.
   - Apply clock source to pin 1 of J2.
   - Apply 3.3V (1) or GND (0) to CLKDIV1 and CLKDIV2 pins to set the desired clock rate as follows:
     - CLKDIV1 = CLKDIV2 = 0 clock frequency = SCLK/8
     - CLKDIV1 = 0, CLKDIV2 =1 clock frequency = SCLK/4
     - CLKDIV1 = 1, CLKDIV2 =0 clock frequency = SCLK
     - CLKDIV1 = CLKDIV2 = 1 clock frequency = SCLK/2
4. To set the clock frequency using crystal Y1:
   - The crystal included on the demo board is 12 MHz.
   - Set JP1 to XTAL position.
   - Apply 3.3V (1) or GND (0) to CLKDIV1 and CLKDIV2 pins to set the desired clock rate as follows:
     - CLKDIV1 = CLKDIV2 = 0 clock frequency = 1.5 MHz
     - CLKDIV1 = 0, CLKDIV2 =1 clock frequency = 3 MHz
     - CLKDIV1 = 1, CLKDIV2 =0 clock frequency = 12 MHz
     - CLKDIV1 = CLKDIV2 = 1 clock frequency = 6 MHz

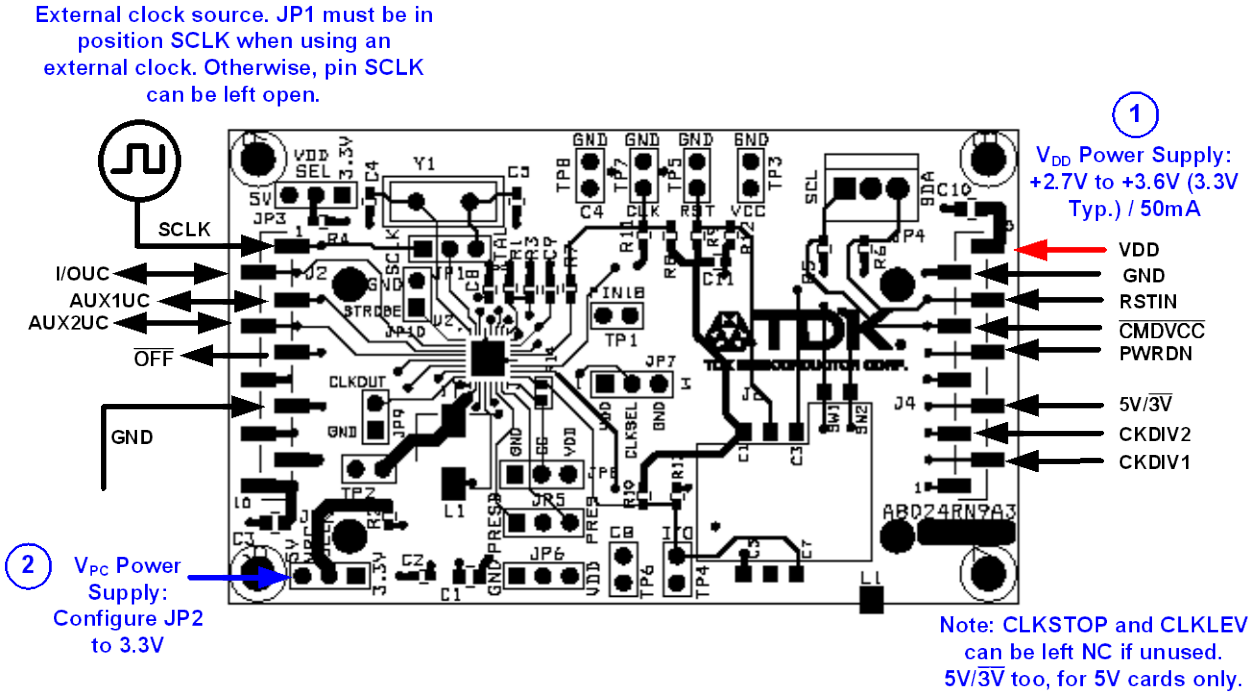

Figure 2: 73S8023C Demo Board Basic Connections

3 Hardware Description

3.1 Demo Board Connectors, Jumpers and Test Points

Table 1 describes the 73S8023C Demo Board connectors, jumpers and test points. The Item # in Table 1 refers to Figure 3.

Table 1: 73S8023C Demo Board Connector, Jumper and Test Points

Item #	Schematic/ Silkscreen Reference	Name	Function
Connectors:			
1	J2	Auxiliary Interface / 5V Board Power	73S8023C auxiliary interface (I/OUC, AUX1UC, AUX2UC), external clock (SCLK) and interrupt ($\overline{OFF}$) pins. The external clock (SCLK) can be left open when JP1 is in position XTAL. The 5V power supply is unused and must be left open and JP2 must be inserted in position 3.3V.
9	J4	3.3V Board Power / Digital Control Signals	3.3V board power supply and the 73S8023C host control signals RSTIN, $\overline{CMDVCC}$, 5V/$\overline{3V}$, PWRDWN, CLKDIV2 and CLKDIV1.
18	J5	Smart Card Connector	Smart card connector. When inserting a card (credit card size format), contacts must face up.
11	J6	Smart Card Connector	SIM/SAM smart card format connector. J6 is wired in parallel to the smart card connector J5 (underneath the PCB). No SIM/SAM should be inserted when using the credit-card size connector J5.
Jumpers:			
3	JP1	Clock Selection	Jumper to select between a crystal or an external clock as the frequency reference to the device. The default setting is for a crystal.
19	JP2	VPC Select	Jumper to select the value of the power supply for the smart card DC-DC converter (73S8023C input VPC). To support both card voltages, JP2 must be set to position 3.3V. The default setting is 3.3V.
2	JP3	VDD Select	Jumper to select the digital voltage which supplies the 73S8023C. **Must be set for 3.3V.**
8	JP4	–	Not used.
16 15	JP5 JP6	Card Polarity Detect Select	The setting of JP5 and JP6 depends on the type of smart card connector used (nominally open or closed) and which 73S8023C card presence switch input is used. The switch is nominally open for the 73S8023C Demo Board. The jumpers can be set to: 1. Use of PRES (default): JP5 set to PRES; JP6 set to VDD. 2. Use of $\overline{PRES}$: JP5 set to PREB; JP6 set to GND.
13	JP7	CLKSEL	Three pin header. Set to VDD for sync operation.
17	JP8	CS	Three pin header. Set to VDD for normal operation.
21	JP9	CLKOUT	Two pin header. Outputs the buffered version of XTALIN.
22	JP10	STROBE	Two pin header. Controls clock signal when CLKSEL=1.

Item #	Schematic/ Silkscreen Reference	Name	Function
Test Points:			
10	TP1	Pin 18* (VDDF_ADJ)	VDD voltage fault adjustment. The pin to the left is connected to the VDDF_ADJ pin of the 73S8023C and the pin to the right is GND. When either a resistor R3, or a resistor network R1 and R3 is populated on the board, it adjusts the VDD fault level that internally triggers a card deactivation sequence. By default, the resistors R1 and R3 are not connected. This provides a VDD fault level of 2.3V typical (internally set to the 73S8023C). Refer to the *73S8023C Data Sheet* for further information about VDD fault level and determination of the resistor values. *The silkscreen is in error. It is shown as 'Pin 18' when actually it is Pin 17.
20	TP2	Factory Test	Factory test pin. Do not connect.
7 12 6 14 5 4	TP3 TP4 TP5 TP6 TP7 TP8	VCC I/O RST C8 CLK C4	2-pin test points for each respective smart card signal. The pin label name is the respective signal (i.e. VCC, CLK) and the 2nd pin is GND.

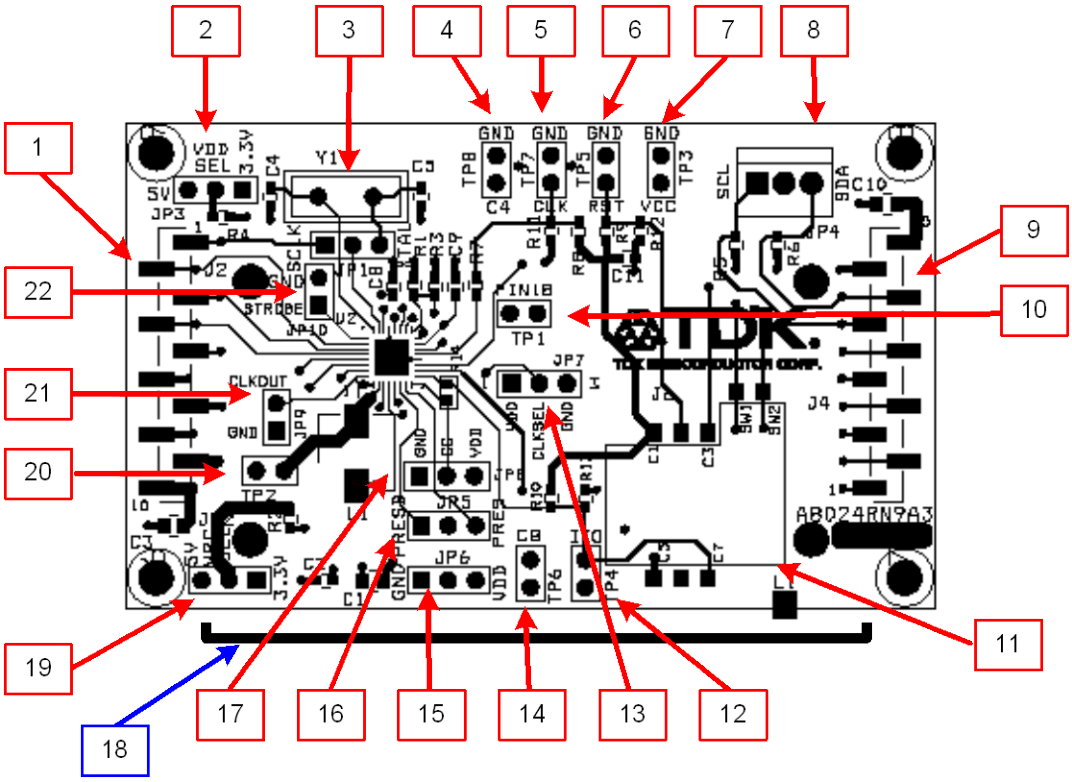

Figure 3: 73S8023C Demo Board Connectors, Jumpers and Test Points

3.2 Recommended Operating Conditions and Absolute Maximum Ratings

Table 2 lists the recommended operating conditions and Table 3 lists the absolute maximum ratings. Operation outside these rating limits may cause permanent damage to the device.

Table 2: Recommended Operating Conditions

Parameter	Rating
Supply Voltage V_{DD}	2.7 to 3.6 VDC
Supply Voltage V_{PC}	2.7 to 3.6 VDC
Ambient Operating Temperature	-40 °C to +85 °C
Input Voltage for Digital Inputs	0 V to V_{DD} + 0.3 V

Table 3: Absolute Maximum Ratings

Parameter	Rating
Supply Voltage V_{DD}	-0.5 to 4.0 VDC
Supply Voltage V_{PC}	-0.5 to 4.0 VDC
Input Voltage for Digital Inputs	-0.3 to (VDD+0.5) VDC
Storage Temperature	-60 °C to 150 °C
Pin Voltage	-0.3 to (VDD+0.5) VDC
Pin Current	±100 mA
ESD Tolerance – Card interface pins	+/- 6 kV
ESD Tolerance – Other pins	+/- 2 kV

ESD testing on Card pins is HBM condition, 3 pulses, each polarity referenced to ground.

3.3 73S8023C Pin Description

Table 4: 73S8023C Card Interface Pins

Name	Pin #	Description
I/O	9	Card I/O: Data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX1	11	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX2	10	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
RST	14	Card reset: provides reset (RST) signal to card.
CLK	13	Card clock: provides clock signal (CLK) to card. The rate of this clock is determined by crystal oscillator frequency or external clock input and CLKDIV selections.
PRES	7	Card Presence switch: active high indicates card is present. Should be tied to GND when not used, but it includes a high-impedance pull-down resistor.
$\overline{\text{PRES}}$	6	Card Presence switch: active low indicates card is present. Should be tied to V_{DD} when not used, but it includes a high-impedance pull-up resistor.
VCC	15	Card power supply: logically controlled by sequencer output of LDO regulator. Requires an external filter capacitor to the card GND.
GND	12	Card ground.

Table 5: 73S8023C Miscellaneous Pins

Name	Pin #	Description
XTALIN	23	Crystal oscillator input: can either be connected to crystal or driven as a source for the card clock.
XTALOUT	24	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as external clock input.
VDDF_ADJ	17	V_{DD} fault threshold adjustment input: this pin can be used to adjust the V_{DDF} values (controls deactivation of the card). Must be left open if unused.
NC	4	Non-connected pin.

Table 6: 73S8023C Power and Ground Pins

Name	Pin #	Description
VDD	20	System interface supply voltage and supply voltage for internal circuitry.
VPC	3	DC-DC converter power supply source.
GND	1	DC-DC converter ground.
GND	21	Digital ground.
LIN	2	External inductor. Connect external inductor from pin 2 to VPC. Keep the inductor close to pin 2.

Table 7: 72S8023C Microcontroller Interface Pins

Name	Pin #	Description
$\overline{\text{CMDVCC}}$	18	Command VCC (negative assertion): Logic low on this pin causes the LDO regulator to ramp the V_{CC} supply to the card and initiates a card activation sequence, if a card is present.
5V/$\overline{\text{3V}}$	31	5 volt / 3 volt card selection: Logic one selects 5 volts for V_{CC} and card interface, logic low selects 3 volt operation. When the part is to be used with a single card voltage, this pin should be tied to either GND or V_{DD}. However, it includes a high impedance pull-up resistor to default this pin high (selection of 5V card) when not connected.
PWRDN	5	Power Down control input. Active high. When the Power Down mode is set high, all internal analog functions are disabled to place the 73S8023C in its lowest power consumption mode. The Power Down mode is only allowed out of a card session (i.e. when CMDVCC = 1)
CLKDIV1 CLKDIV2	29 30	Sets the divide ratio from the XTAL oscillator (or external clock input) to the card clock. These pins include pull-down resistors.
$\overline{\text{OFF}}$	22	Interrupt signal to the processor. Active low - multi-function indicating fault conditions and/or card presence. Open drain output configuration; includes an internal 22 kΩ pull-up to $V_{DD.}$
RSTIN	19	Reset Input: This signal is the reset command to the card.
I/OUC	26	System controller data I/O to/from the card. Includes a pull-up resistor to $V_{DD.}$
AUX1UC	27	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to $V_{DD.}$

CLKDIV1	CLKDIV2	CLOCK RATE
0	0	XTALIN/8
0	1	XTALIN/4
1	1	XTALIN/2
1	0	XTALIN

Name	Pin #	Description
AUX2UC	28	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to $V_{DD.}$
CLKSEL	16	Selects CLK and RST operational mode. When CLKSEL is low (default), the circuit is configured for asynchronous card operation and the control of CLK and RST is managed by the sequencer. When CLKSEL is high, the CLK signal is a buffered copy of STROBE and the RST signal is directly controlled by RSTIN.
CLKOUT	32	CLKOUT is a buffered version of the signal on pin XTALIN.
STROBE	25	When CLKSEL = 1, the signal CLK is controlled directly by STROBE.
CS	8	When CS = 1, the control and signal pins are configured normally. When CS is set low, CMDVCCB, RSTIN, 5V/3V, CLKDIV1, CLKDIV2, CLKSEL, and STROBE are latched. I/OUC, AUX1UC, and AUX2UC are set to high-impedance pull-up mode (3 µA pull-up to VDD) and do not pass data to or from the smart card.

3.4 73S8023C Pinout

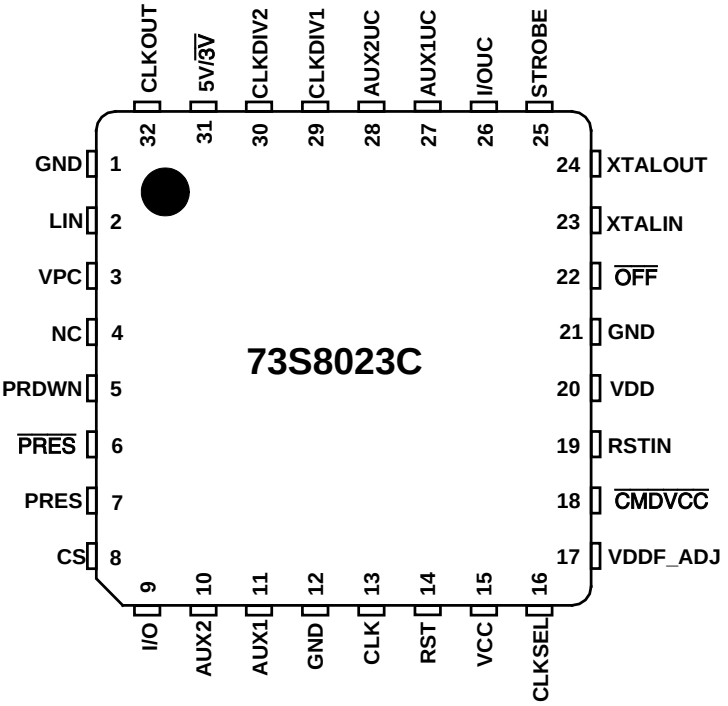

Figure 4: 73S8023C 32QFN Pinout (Top View)

4 Design Considerations

4.1 General Layout Rules

- Route the auxiliary signals away from card interface signals.
- Keep the CLK signal as short as possible and with few bends in the trace. Keep the route of the CLK trace to one layer (avoid vias to other plane). Keep the CLK trace away from other traces, especially RST and VCC. Filtering of the CLK trace is allowed for noise purpose. Up to 30 pF to ground is allowed at the CLK pin of the smart card connector. In addition, the zero ohm series resistor, R7, can be replaced for additional filtering (no more than 100 Ω).
- Keep the VCC trace as short as possible. Make the trace a minimum of 0.5 mm thick. In addition, keep the VCC away from other traces, especially RST and CLK.
- Keep the trace from L1 to pin 2 of the IC as short as possible.
- Keep the RST trace away from the VCC and CLK traces. Up to 30 pF to ground is allowed for filtering.
- Keep the 0.1 μF capacitor close to the VDD pin of the device and directly take the other end to ground.
- Keep the 0.1 μF capacitor close to the VPC pin of the device and directly take the other end to ground.
- Keep the 3.3 μF (1.0 μF for NDS) capacitor close to the VCC pin of the smart card connector and directly take other end to ground.

4.2 Optimization for Compliance with EMV and NDS

The default configuration of the demo board contains a 27 pF capacitor (C12) from the CLK pin of the smart connector to ground and a 27 pF capacitor (C13) from the RST pin of the smart connector to ground. These capacitors serve as filters for the CLK and RST signals in the case of long traces or test equipment perturbations. The capacitor on CLK reduces ringing on the trace, reduces coupling to other traces and slows down the edge of the CLK signal. The capacitor on RST helps the perturbation specification in a noisy environment. The filter capacitors can be useful in the EMV test environment and have no effect on NDS testing.

C12 and C13 are represented on both the schematic and the BOM. These capacitors are optional filter capacitors on the smart card lines CLK and RST, respectively for each card interface. These capacitors may be adjusted (value not to exceed 30 pF) or removed to optimize performance in each specific application (PCB, card clock frequency, compliance with applicable standards etc).

The default VCC capacitor of 3.3 μF is required to meet the dynamic VCC (smart card supply) transient current requirement as specified in the EMV2000 version 4.0 specification. For compliance with NDS, a smaller capacitor of 1 μF is required to meet the activation discharge time specification.

5 73S8023C Demo Board Schematics, PCB Layouts and Bill of Materials

5.1 Schematic

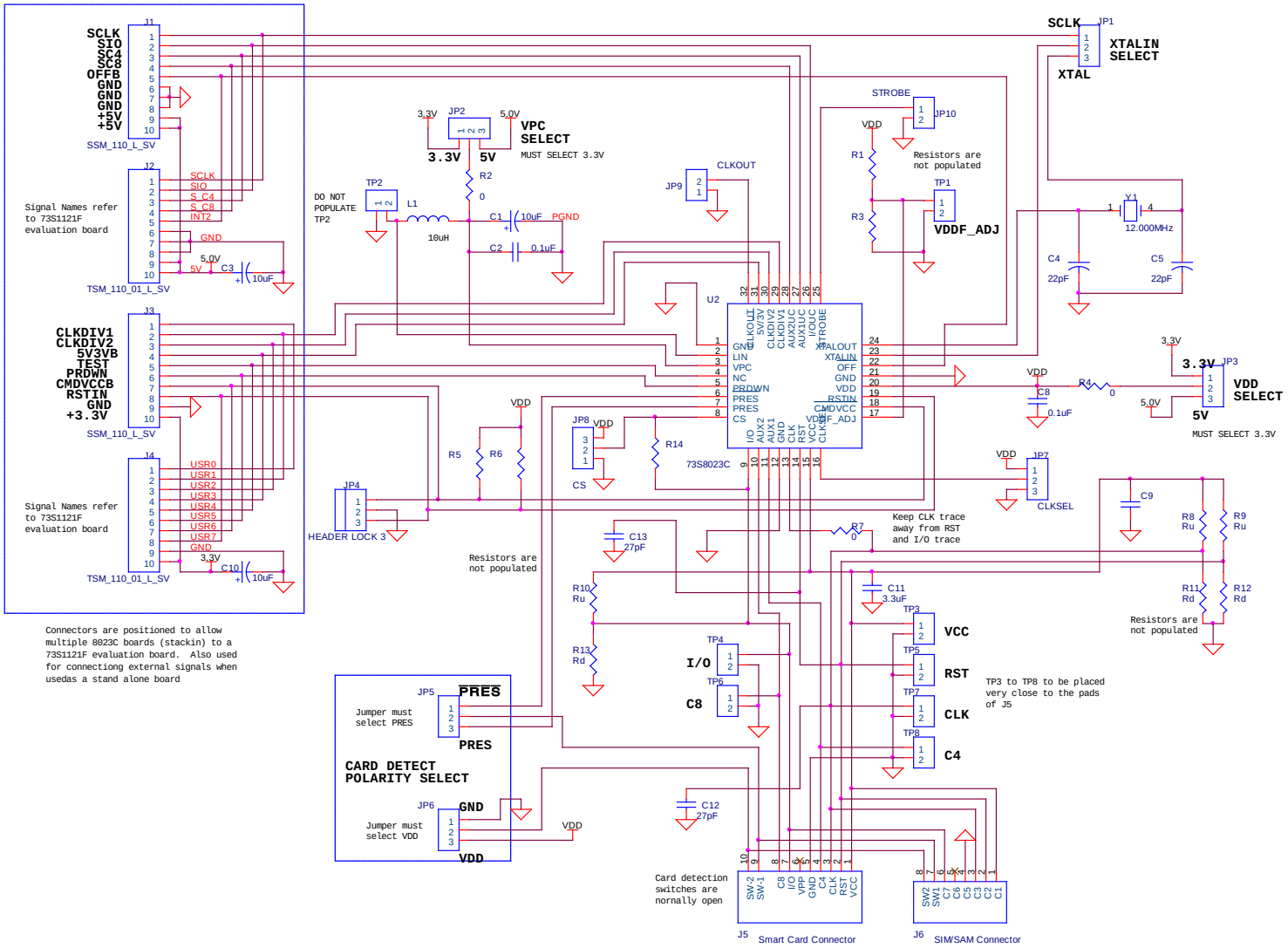

Figure 5: 73S8023C Demo Board Electrical Schematic

5.2 Bill of Materials

Table 8 provides the bill of materials for the 73S8023C Demo Board schematic provided in Figure 5.

Table 8: 73S8023C Demo Board Bill of Materials

Item	Quantity	Reference	Part	PCB Footprint	Digikey Part Number	Part Number	Manufacturer
1	3	C1,C3,C10	10 µF	805	PCC2225CT-ND	ECJ-2FB0J106M	Panasonic
2	2	C2,C8	0.1 µF	603	PCC1762CT-ND	ECJ-1VB1C104K	Panasonic
3	2	C4,C5	22 pF	603	PCC220ACVCT-ND	ECJ-1VC1H220J	Panasonic
4	1	C9	X	603	X	X	not populated
5	1	C11	3.3 µF	805	PCC1925CT-ND	ECJ-2YB0J335K	Panasonic
6	2	C12, C13	27 pF	402	PCC270CQCT-ND	ECJ-0EC1H270J	Panasonic
7	7	JP1,JP2,JP3,JP5, JP6,JP7,JP8	HEADER 3	3pins, 2.54 mm pitch	S1011-36-ND	PZC36SAAN	Sullins
8	1	JP4	X	3pins, 2.54 mm pitch	X	X	not populated
9	2	JP9,JP10	HEADER 2	2X1_Header	S1011-36-ND	PZC36SAAN	Sullins
10	2	J1,J3	SSM_110_L_SV	SSM_110_L_SV	X	SSM_110_L_SV	Samtec
11	2	J2,J4	TSM_110_01_L_SV	TSM_110_01_L_SV	X	TSM_110_01_L_SV	Samtec
12	1	J5	Smart Card Connector	ITT_CCM02-2504	ccm02-2504-ND	ccm02-2504	ITTCannon
13	1	J6	SIM/SAM Connector	ITT_CCM03-3754	CCM03-3754CT-ND	CCM03-3754	ITTCannon
14	1	L1	10 µH		445-1186-1-ND	SLF7032T-100M1R4-2	TDK
15	3	R2,R4,R7	0	603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
16	6	R1,R5,R6,R8,R9,R10	Ru[1]	603	X	X	
17	4	R3,R11,R12,R13	Rd[1]	603	X	X	
18	7	TP1,TP3,TP4,TP5, TP6,TP7,TP8	TP	2X1_Header	S1011-36-ND	PZC36SAAN	Sullins
19	1	U2	73S8023C	32QFN	X	73S8023C	Teridian Semiconductor
20	1	Y1	12.000 MHz	HC-49US	X190-ND	ECS-120-20-4DN	ECS

[1] Ru and Rd are not populated on the board. They can be implemented to adjust the features of the smart card reader.

5.3 PCB Layouts

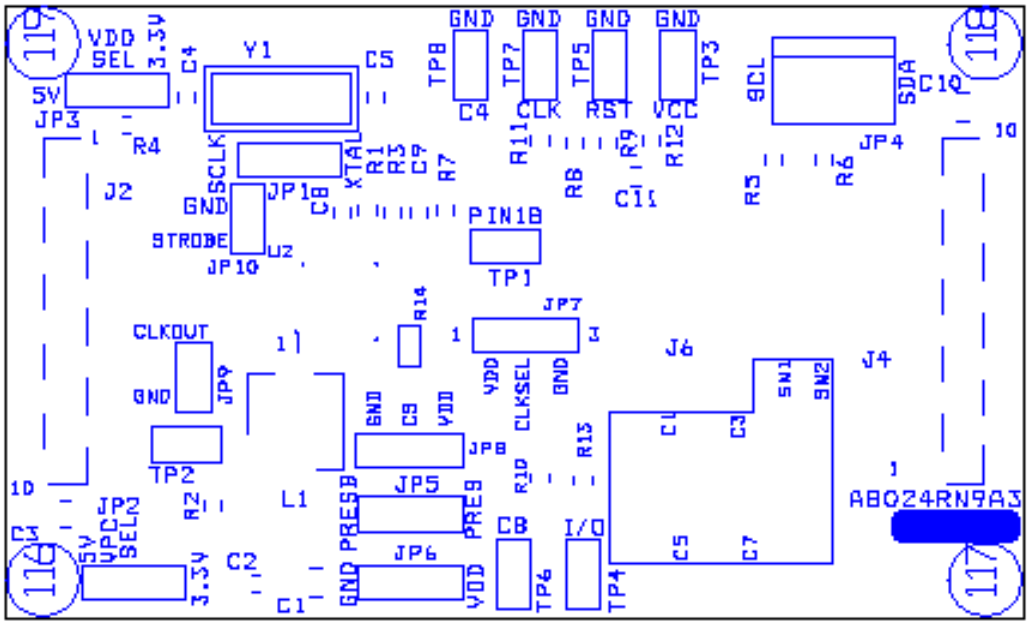

Figure 6: 73S8023C Demo Board Top View

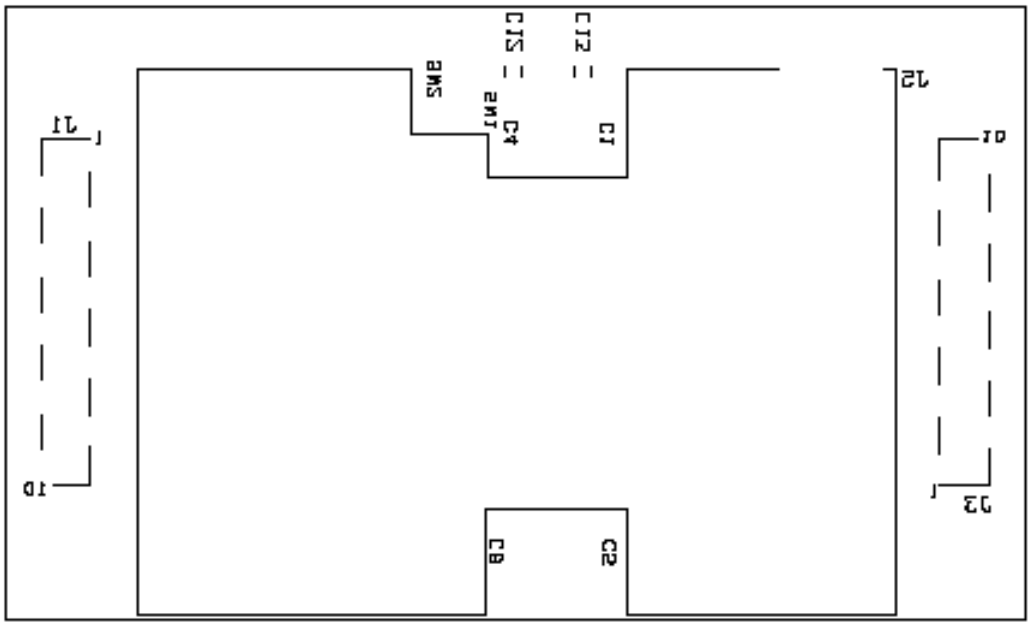

Figure 7: 73S8023C Demo Board Bottom View

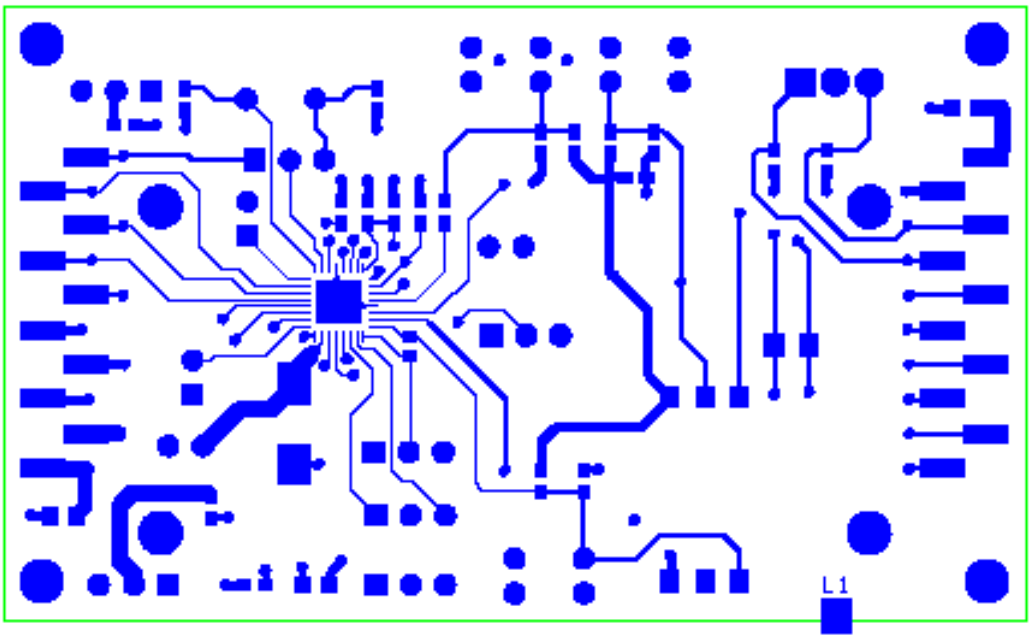

Figure 8: 73S8023C Demo Board Top Signal Layer

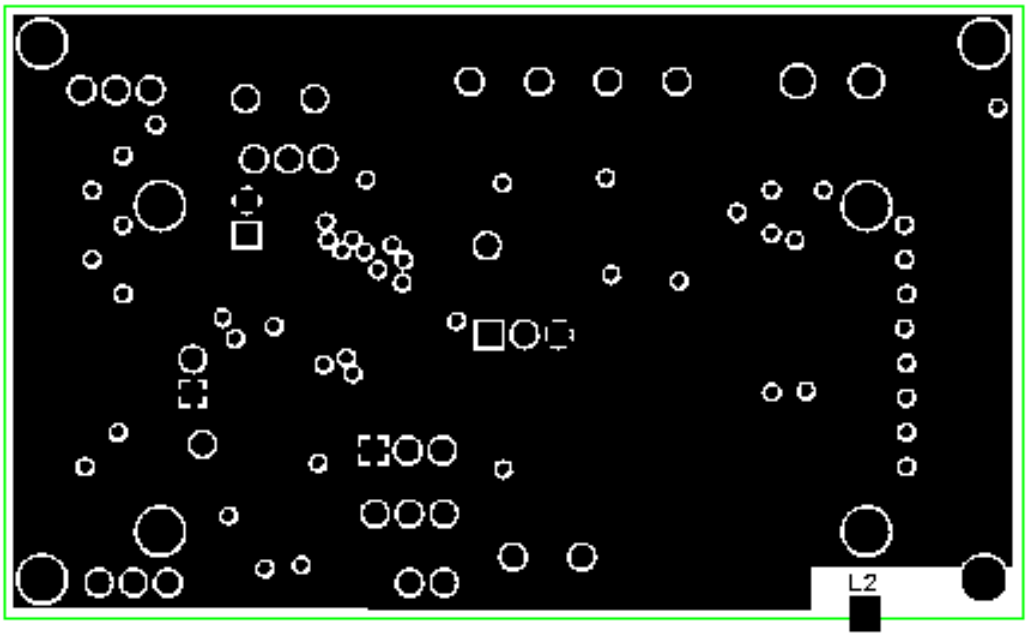

Figure 9: 73S8023C Demo Board Middle Layer 1, Ground Plane

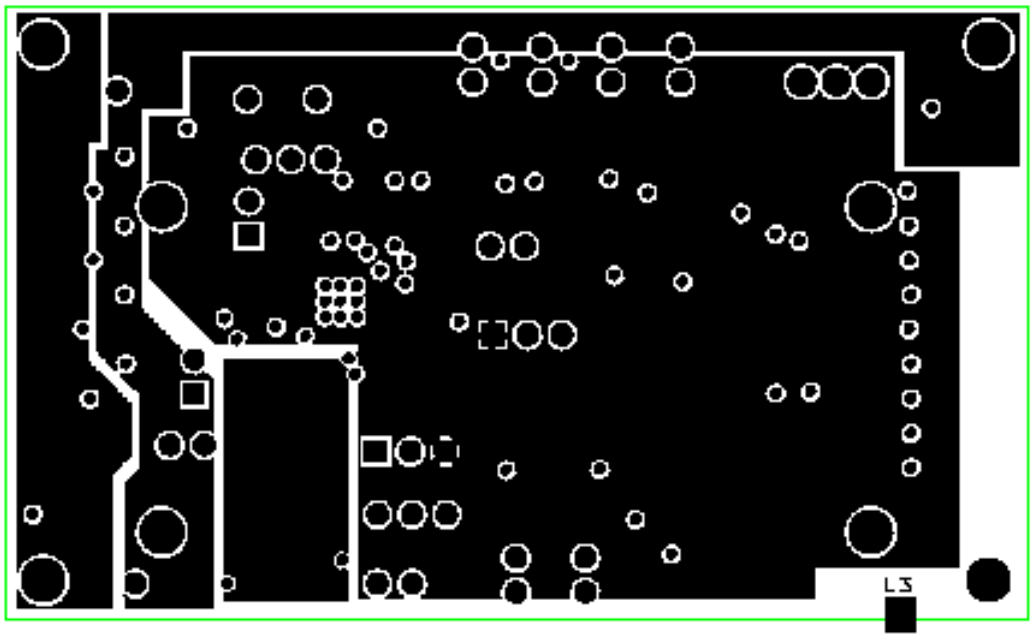

Figure 10: 73S8023C Middle Layer 2, Supply Plane

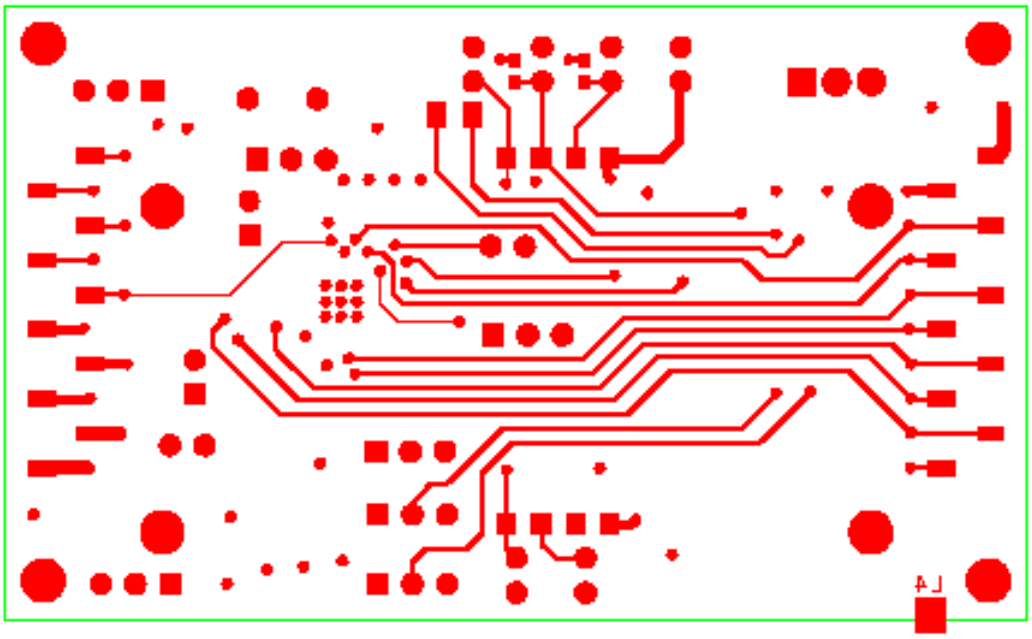

Figure 11: 73S8023C Demo Board Bottom Signal Layer

6 Ordering Information

Table 9 lists the order number used to identify the 73S8023C Demo Board.

Table 9: Order Number

Part Description	Order Number
73S8023C 32-Pin QFN Demo Board	73S8023C-DB

7 Related Documentation

The following 73S8023C documents are available from Teridian Semiconductor Corporation:

73S8023C Data Sheet
73S8023C Demo Board User Manual (this document)

8 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8023C, contact us at:

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Revision History

Revision	Date	Description
1.0	8/3/2004	First publication.
1.1	11/26/2004	Minor corrections.
1.2	8/23/2005	Added new logo.
1.3	11/11/2009	Added Section 1.1, Package Contents. Added Section 1.2, Safety and ESD Notes. Added Section 6, Ordering Information. Added Section 7, Related Documentation. Added Section 8, Contact Information. Miscellaneous editorial changes.