Signetics

74LS1801
Bit Stream Manager

Encoder/Decoder
Product Specification

Logic Products

DESCRIPTION

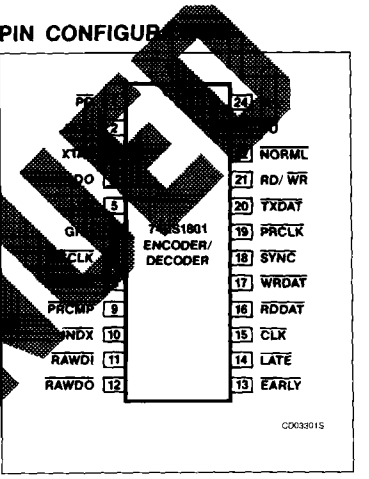
The 74LS1801 Encoder/Decoder (Figure 1) supports disk drive and data communications devices that require fast and reliable data separation capabilities. Although ideally suited for use with the 74LS1802 Serializer/Deserializer, the 74LS1801 is a flexible device which can be implemented in a variety of design applications.

Encoding is possible in FM, MFM, or Differential Manchester formats, making the 74LS1801 invaluable in designs requiring single density disk recording, double density disk recording, or in data communications applications. Included on-chip is a phase-comparator which can be bypassed; this feature is particularly useful in applications that use a complete external phase lock loop.

FEATURES

- **Data rates up to 10MHz**
- **FM, MFM, and Differential Manchester encoding/decoding**
- **Precompensation in MFM write mode**
- **Built-in phase comparator**
- **Single 5-volt power supply**
- **Selectable encoding violation generation/detection formats**

PIN CONFIGURATION



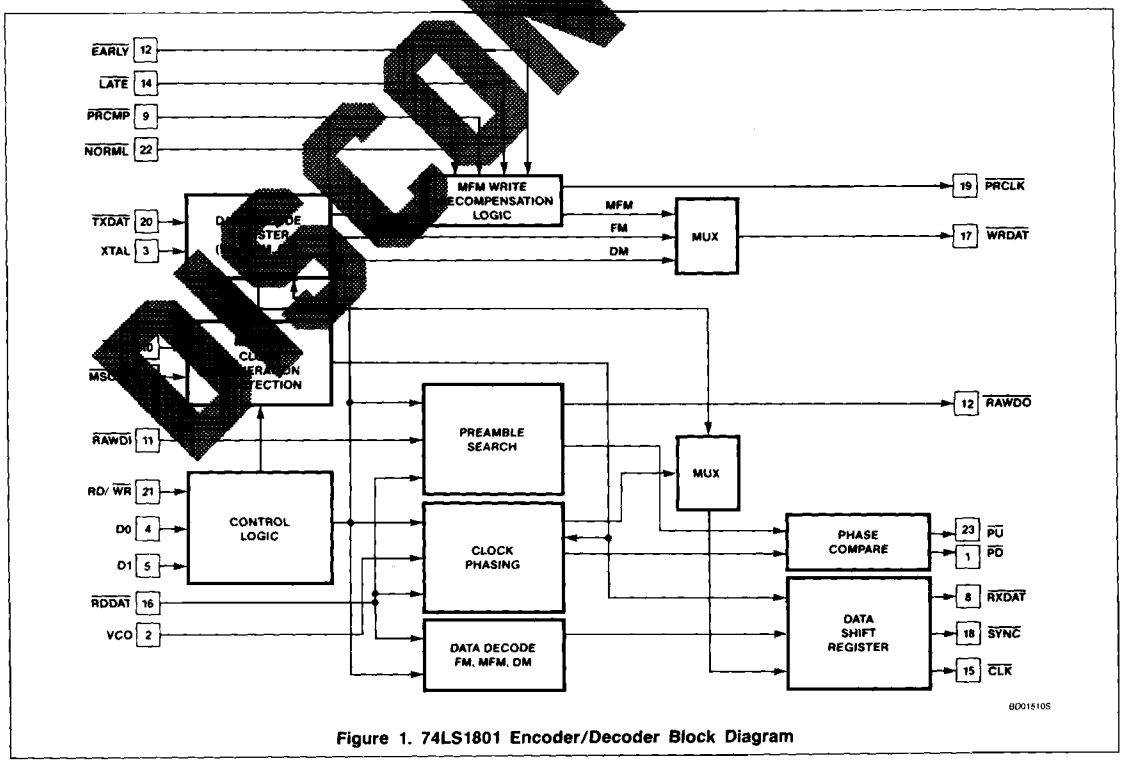
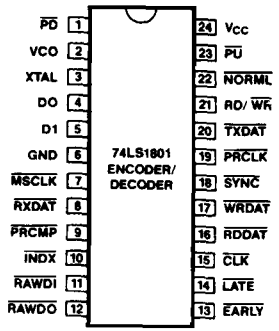


Figure 1. 74LS1801 Encoder/Decoder Block Diagram

PIN DESCRIPTION



PIN NO.	IDENTIFIER	DESCRIPTION
1	$\overline{PD}$	Pump Down – an output from the phase comparator that indicates the frequency of an external VCO is too high as compared to $\overline{RDDAT}$.
2	VCO	Voltage Controlled Oscillator – input used as a phase reference for the error signal read data ($\overline{RDDAT}$).
3	XTAL	An input clock to synchronize the 74LS1801 during write mode; the crystal frequency is two times the serial data rate.
4	D0	Mode Select inputs designating the format
5	D1	(MFM, FM, or Differential Manchester) of serial NRZ data that is to be encoded or decoded.
6	GND	Ground.
7	MSCLK	Missing CLocK – missing clock bits are encoded/detected in the data stream, depending upon the state of this input (Table 2, 3).
8	$\overline{RXDAT}$	Receive DATa – an output consisting of NRZ data decoded from MFM, FM, or Differential Manchester data.
9	$\overline{PRCMP}$	PReCoMP – an input that allows precompensation of MFM encoded data.

PIN NO.	IDENTIFIER	DESCRIPTION
10	$\overline{INDX}$	INDeX – an input that designates the missing clock pattern to be generated during the write mode; in the read mode, determines which data/clock pattern must be recognized as an address mark (Table 2, 3).
11	$\overline{RAWDI}$	RAW Data In – a read data pulse derived from $\overline{RAWDO}$. $\overline{RAWDI}$ is normally tied directly to $\overline{RAWDO}$.
12	$\overline{RAWDO}$	RAW Data Out – a shaped data pulse derived from $\overline{RAWDI}$ that can be processed through an external phase lock loop. $\overline{RAWDO}$ is normally tied directly to $\overline{RAWDI}$.
13	EARLY	Signifies clock rate with respect to crystal reference when an early precompensation is desired.
14	LATE	Signifies clock rate with respect to crystal reference when late pre-compensation is desired.
15	CLK	CLocK – Clock input equal to the frequency of NRZ data.
16	$\overline{RDDAT}$	ReaD DATa – an input of encoded serial data (MFM, FM, or Differential Manchester) that is to be converted to NRZ data.
17	$\overline{WRDAT}$	WRite DATa – an output of encoded serial data (FM, MFM, or Differential Manchester) derived from NRZ data.
18	$\overline{SYNC}$	SYNChronization output – when active low, indicates recognition of valid encoding violation in the $\overline{RDDAT}$.
19	$\overline{PRCLK}$	PRecompensation CLocK – an output used to excite an external delay line.
20	$\overline{TXDAT}$	Transmit Data – an input of NRZ data that is to be encoded to FM, MFM, or Differential Manchester data.
21	RD/$\overline{WR}$	ReaD/WRite – an input designating mode of operation: when high, a read is indicated; when low, a write is indicated.
22	$\overline{NORML}$	NORMaL – a clock input that is used when no precompensation is desired.
23	$\overline{PU}$	Pump Up – an output from the phase comparator that indicates the frequency of an external VCO is too low as compared to $\overline{RDDAT}$.
24	V_{CC}	Supply voltage.

7

FUNCTIONAL OPERATION

The 74LS1801 Encoder/Decoder serves to translate data between disk drive or data communications devices and the 74LS1802 Serializer/Deserializer (or comparable device). Information entering or leaving the Serializer/Deserializer interface is in the form of standard NRZ data and can be encoded to (or decoded from) one of three popular formats:

- Frequency Modulation (FM) — single density disk recordings.
- Modified Frequency Modulation (MFM) — double density disk recordings.
- Differential Manchester — data communications applications.

Read/Write and Format Control

The operational mode of the 74LS1801 is dictated by the RD/$\overline{WR}$ input: when low, a write (encode) is indicated; when high, a read (decode) is designated. In either mode, the format of data being decoded or encoded is controlled by the states of D0 and D1 inputs as shown below:

Table 1. Format Control

D0	D1	RESULTING FORMAT
L	L	MFM
H	L	FM
L	H	Differential Manchester

Following are discussions of the encoding and decoding functions of the 74LS1801, the timing requirements necessary for high-rate data transmittal.

Encoding Logic

When in the encode mode, [illegible] data [illegible] via the $\overline{TXDAT}$ input and after a bit delay, is output on [illegible]. As described in Table 2, output format is dependent [illegible] the states of D0 and D1. Address marks [illegible] from data by omitting [illegible] within the character.

These "missing [illegible]" are generated within the byte following a [illegible] of either all 0's (MFM and FM formats) or all 1's (Differential Manchester format). As described in Table 2, clocks are eliminated according to inputs $\overline{INDX}$, $\overline{MSCLK}$, and the specified encoding format.

When encoding data in the MFM format, $\overline{MSCLK}$ may be enabled during preamble generation and up to the beginning of an address mark. $\overline{MSCLK}$ can then be disabled during the byte following an address mark, or before the final bit of a four bit series in which the first two bits are 0's (e.g., before the final 0 in 0010). In applications utilizing consecutive A1 characters (such as in the case of floppy disk soft-sectored formats), $\overline{MSCLK}$ would remain active until the beginning of the byte following the [illegible].

Table 2. Missing Clocks

$\overline{MSCLK}$	$\overline{INDX}$	FORMAT	RESULTING CLOCK PATTERN Bit Cell Numbers: 0	1	2	3	4	5	6	7
L	H	FM			V	V	V			
L	L	FM			V		V			
L	H	Differential Manchester	V	V		V	[illegible]			
L	L	Differential Manchester	V	V						
L	X	MFM	2nd of 3 [illegible]s missi[illegible]							

NOTES:
X = Don't care
V = Missing Clock

Table 3. Address Mark Identification [illegible]remental Decode Mode

$\overline{MSCLK}$	$\overline{INDX}$	[illegible]DITI[illegible]	[illegible]CTIVE $\overline{SYNC}$ OUTPUT
H	X	[illegible]	First "1" bit after preamble
L	H	[illegible]	$A1_{16}$ with missing clocks
L	L	[illegible]	[illegible]y byte with missing clocks

The 74LS1801 [illegible] provides [illegible] compensation capabilities [illegible] encoding [illegible] the MFM form[illegible] [illegible]e $\overline{PRCMP}$ signal (low) synchr[illegible] [illegible] according to a clock [illegible] pr[illegible] [illegible] three inputs: E[illegible] [illegible]locks [illegible]fted early in time, L[illegible] – a [illegible] s[illegible] late in time, or N[illegible] – a c[illegible] rovided when no precompens[illegible] is r[illegible]d. These inputs are supplied by [illegible]nal delay line which, in turn, is excited by the $\overline{PRCLK}$ output (see Typical Syst[illegible] Configuration, Figure 2.)

[illegible]ncoding in FM or Differential Manchester formats, missing clocks are only generated in the first byte following a preamble of zeroes. The most significant bit of this byte must be a "1"; for example, address marks F8, FB, FC, or FE. $\overline{MSCLK}$ may be enabled up to the beginning of an address mark; once an address mark has been transmitted, it is not necessary to disable $\overline{MSCLK}$.

Decoding Logic

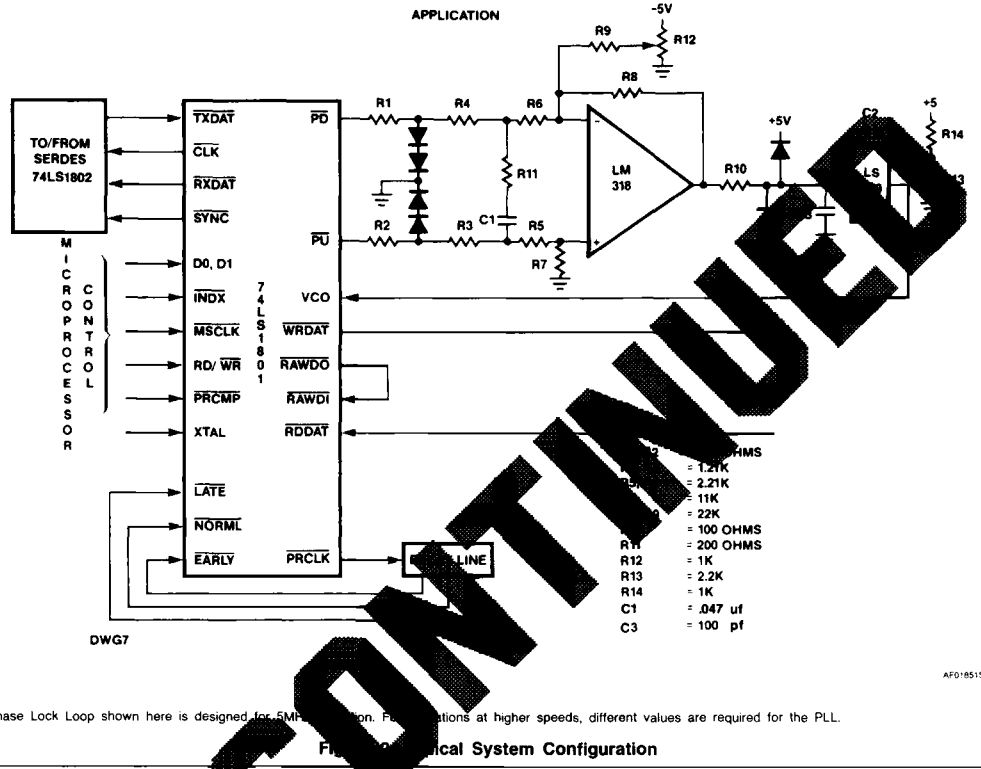
In the decode mode, data (MFM, FM, or Differential Manchester) is input via the $\overline{RDDAT}$ input and, after an eleven bit delay, is output as NRZ data on $\overline{RXDAT}$. As described above, input format is defined by the states of D0 and D1. In the MFM format, a minimum preamble length of 34 bits is required to allow for phase synchronization and location of an address mark; when in FM or Differential Manchester mode, a minimum length of 18 bits is required. After a preamble has been recognized, the 74LS1801 searches for an address mark. When an address mark is identified, the $\overline{SYNC}$ output becomes active low, and alerts the 74LS1802 of incoming data. Rules for positive address mark identification are described below and summarized in Table 3.

When $\overline{MSCLK}$ is inactive, $\overline{SYNC}$ is activated on the first "1" data bit following a preamble of zeroes (MFM and FM) or 1's (Differential Manchester). Data is contained in the byte following this bit.

If $\overline{MSCLK}$ is active, the byte following a preamble of all zeroes is checked for the required missing clocks (Table 3) and if detected, $\overline{SYNC}$ is activated.

PHASE LOCK LOOP AND DATA SEPARATION LOGIC

Data/clock separation logic requires a clock pulse that is synchronous with read data ($\overline{RDDAT}$); to create this signal, the 74LS1801 employs a Phase Lock Loop. In its simplest form, the PLL consists of an internal phase comparator, an external low pass filter and an external voltage controlled oscillator (VCO). Output from the VCO is continuously fed back to the phase compare circuit and contrasted with data read from the disk or communications device ($\overline{RDDAT}$). A difference in phase is represented as one of two quantized output pulses: Pump Up indicates VCO frequency is too low, whereas Pump Down indicates that the VCO frequency is too high. The resulting output ($\overline{PU}$ or $\overline{PD}$) is then processed by a low-pass filter which outputs a DC voltage proportional to the phase deviation. Accordingly, the VCO frequency is precisely serviced to the rate at which data was recorded. The 74LS1801 provides the capability to bypass internal phase compare logic; a typical application of this feature would be in designs implementing a complete external PLL.



NOTE:
The Phase Lock Loop shown here is designed for 5MH[illegible]ion. F[illegible]ations at higher speeds, different values are required for the PLL.

F[illegible]ical System Configuration

Figure 3 illustrates this application[illegible]is discussed below.

RAW Data Out is a shape[illegible]a g[illegible]ive directly from RDDAT. M[illegible]s, output is generated [illegible]ng e[illegible]of RDDAT: in D[illegible]ntia[illegible]che[illegible]de, output is g[illegible]fro[illegible]h[illegible]g and falling ed[illegible]RAW[illegible]In [illegible]aped data pulse deri[illegible]m R[illegible]D and is used in internal data [illegible]ratio[illegible]gic. The falling edge of RAWDO is in phase with the falling edge of the [illegible]RAWDI is normally tied directly to RAWDO.

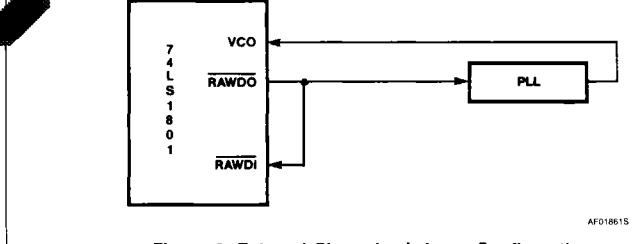
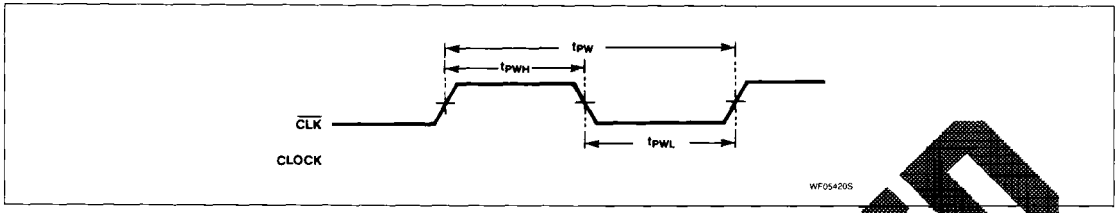
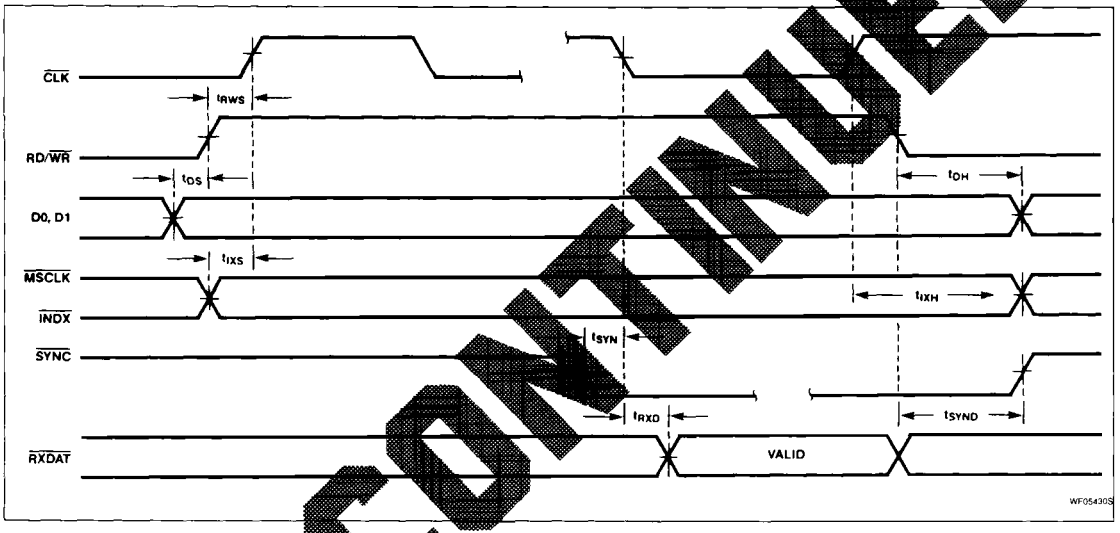


Figure 3. External Phase Lock Loop Configuration

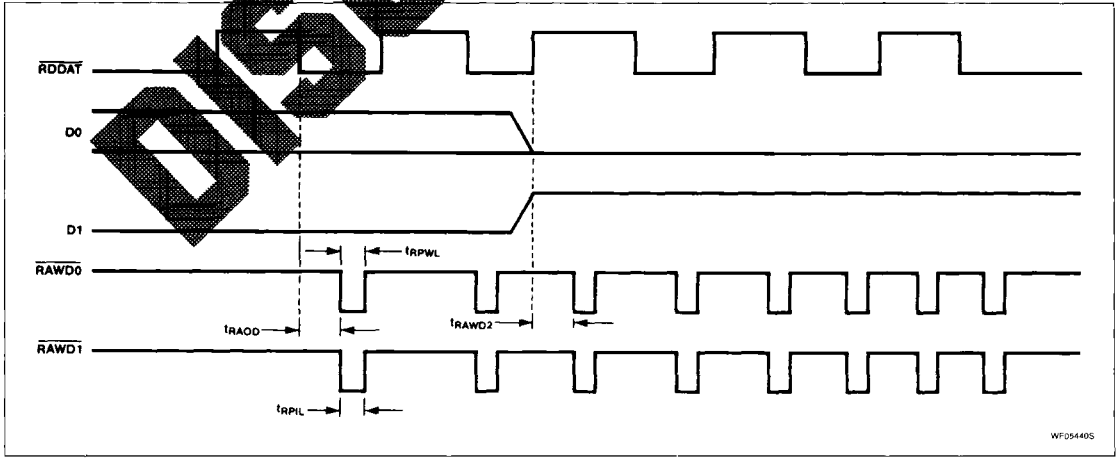
CLOCK CYCLE



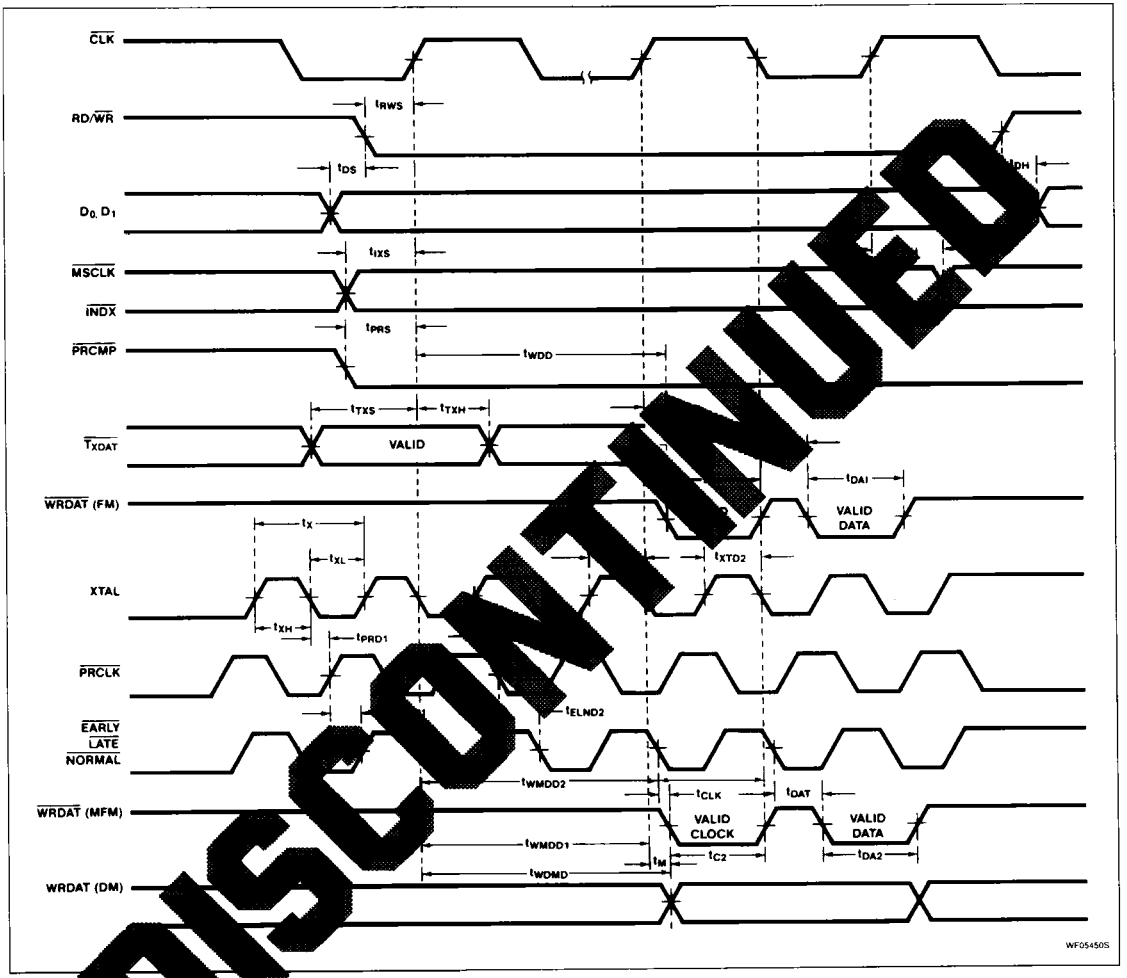
READ CYCLE



OTHER TIMING



WRITE CYCLE TIMING



7

ABSOLUTE MAXIMUM RATINGS

PIN	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
All other pins	Logic input pins	5.5	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V±5%; TA = 0°C to +70°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	COMMENTS
			Min	Typ	Max		
V_{TH}	Input threshold voltage		0.8		2.0	V	
V_{CD}	Input clamp diode voltage	I_N = -18mA			-1.2	V	
I_{IL}	Input low current	V_{IN} = 0.4V					
I_{IH}	Input high current	V_{IN} = 2.7V				µA	
I_I	Max input high current	V_{IN} = 5.5V			100	µA	
V_{OL}	Output voltage low	I_{OL} = 8mA I_{OL} = 20mA			0.5	V V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
V_{OH}	Output voltage high	V_{CC} = 4.5V I_{OH} = 400µA I_{OH} = 1mA	2.5			V V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
I_{OS}	Output short circuit current	V_{out} = 2.5V V_{out} = 0V	-15		-100 -100	mA mA	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
I_{CC}	Supply current				184	mA	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t_{PW}	CLK pulse width	100		
t_{PWL}	CLK low time	50		
t_{PWH}	WR high time	50		
t_X	XTAL cycle time	50		
t_{XH}	XTAL high time	25		
t_{XL}	XTAL low time	25		
t_{RWS}	RD/WR set-up to ↑CLK	0		
t_{DS}	D0, D1 set-up to RD/WR	0		
t_{IXS}	MSCLK, INDX set-up to ↑CLK		35.2	
t_{SYN}	↓SYNC to ↓CLK	2		
t_{RXD}	↓CLK to RXDAT valid			4
t_{DH}	RD/WR to D0, D1 hold	0		
t_{SYND}	RD/WR to SYNC inactive delay			36.4
t_{RAOD}	↓RDDAT to ↓RAWDO delay		29.2	
t_{RPIL}	RAWDI pulse width	20*		
t_{RPWL}	RAWDO pulse width			40*
t_{WDMD}	TXDAT to WRDAT (DM)			t_{PW} + 41.2
t_M	↑CLK to WRDAT delay		41.2	
t_{RAWD2}	↑RDDAT to ↓RAWDO delay		32.2	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t_{DA2}	DATA bit duration		23.0	
t_{IXH}	↑$\overline{CLK}$ to $\overline{MSCLK}$, $\overline{INDX}$ hold			
t_{PRS}	$\overline{PRCMP}$ set-up to ↑$\overline{CLK}$			0
t_{TXS}	$\overline{TXDAT}$ set-up to ↑$\overline{CLK}$			
t_{TXH}	$\overline{TXDAT}$ hold time			
t_{WDD}	$\overline{TXDAT}$ to $\overline{WRDAT}$ clock delay (FM data)		t_{PW} +	
t_D	↑$\overline{CLK}$ to clock delay (FM data)		36.3	
t_{C1}	Clock bit duration (FM)		19	
t_{R1}	Clock & data bit separation			
t_{DA1}	Data bit duration (FM)			
t_{XTD1}	↑XTAL to ↑$\overline{CLK}$ delay		35.2	
t_{XTD2}	↑XTAL to ↓$\overline{CLK}$ delay		32.2	
t_{PRD1}	↓XTAL to ↑$\overline{PRCLK}$ delay		26.3	
t_{PRD2}	↑XTAL to ↓$\overline{PRCLK}$ delay		28.3	
t_{ELND1}	↑$\overline{PRCLK}$ to $\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ rising edge	t_{PW}		¼ t_{PW}
t_{ELND2}	↓$\overline{PRCLK}$ to $\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ falling edge	¾ t_{PW}		0
t_{WMDD2}	$\overline{TXDAT}$ to $\overline{WRDAT}$ data delay (MFM)			3.5 x t_{PW}
t_{WMDD1}	$\overline{TXDAT}$ to $\overline{WRDAT}$ clock delay (MFM)			3.0 x t_{PW}
t_{CLK}	$\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ falling edge to clock [illegible] delay (MFM)		12.1	
t_{C2}	Clock bit duration (MFM)		23.0	
t_{DAT}	$\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ falling edge to data [illegible] delay (MF[illegible]		12.1	

*Tabular entries with an asterisk are parameters that are guarantee[illegible]; these values were determined either by system bench testing or by Signetics' characterization procedures. All other tabular entries are ta[illegible] direc[illegible]sults run at range of operational frequencies; these values are not tested or guaranteed.

7