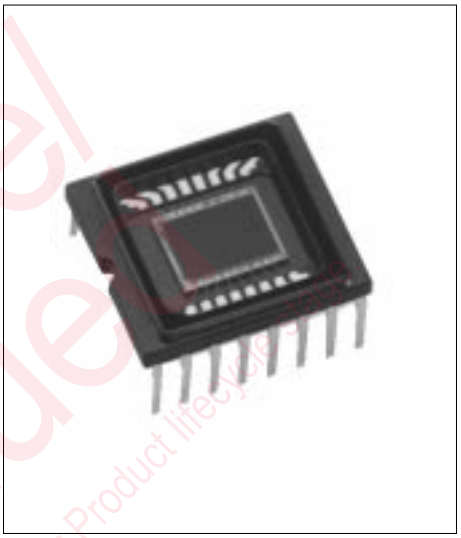
MN37181FT

6 mm (type-1/3) 410k pixel Hyper-D CCD

■ Overview

The hyper-D CCD is a CCD area image sensor featuring an ultra-wide dynamic range that far surpasses anything achieved by the competition. It has 1/3-type 410k pixels. The CCD can read the following two types of signals at the same time and advance them to the signal output stage:normal image signals shot at normal shutter speeds and high-brightness image signals shot at hgih shutter speeds. By synthesizing the two signals in an external circuit, an ultla-wide dynamic range of twenty times wider than that of the conventional CCD can be obtained.
With this ultla-wide dynamic range, the CCD can provide sharp image signals for both bright and dark areas. Accordingly, this CCD is suitable for such applications as security cameras and cameras for vehicles, which typically involve high contrast between the scene's bright and dark regions.



Part Number	Size	System	Color or B/W
MN37181FT	6mm(type-1/3)	NTSC	Color

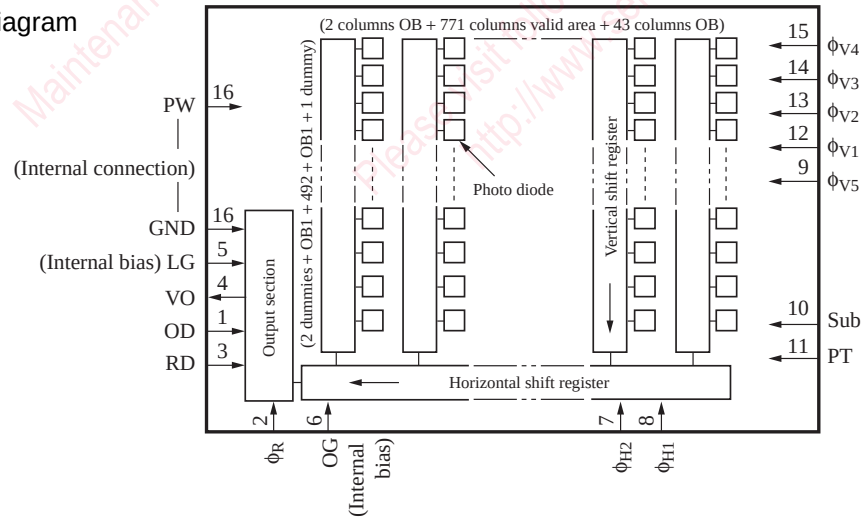
■ Features

- Indusutry leading ultra wide dynamic range (D range:20times the conventional CCD) A clear image can be obtained even when there is a high contrast between bright and dark regions.
- This high speed horizontal CCD can operate at the same voltage (5V) but at twice the speed of conventional models. The external circuit can be simplified.

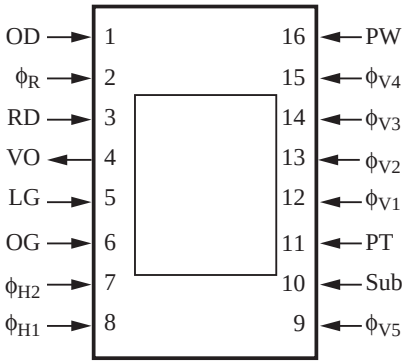
■ Applications

- Security camera. Camera for vehicle, and industrial use. Image input camera for personal computer

■ Block Diagram



■ Pin Assignments



(Top View)

■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	11	PT	P-well for protection circuit
2	ϕ_R	Reset pulse	12	ϕ_{V1}	Vertical shift register clock pulse 1
3	RD	Reset drain			
4	VO	Video output	13	ϕ_{V2}	Vertical shift register clock pulse 2
5	LG	Output load transistor gate			
6	OG	Output gate	14	ϕ_{V3}	Vertical shift register clock pulse 3
7	ϕ_{H2}	Horizontal register clock pulse 2			
8	ϕ_{H1}	Horizontal register clock pulse 1	15	ϕ_{V4}	Vertical shift register clock pulse 4
9	ϕ_{V5}	Vertical shift register clock pulse 5			
			16	PW	P-well
10	Sub	Substrate			

■ Absolute Maximum Ratings and Operating Conditions

Parameter	Symbol	Rating		Operating condition			Unit
		min	max	min	typ	max	
Reset drain voltage	V_{RD}	– 0.2	18.0	14.5	15.0	15.5	V
Output drain voltage	V_{OD}	– 0.2	18.0	14.5	15.0	15.5	V
Output load transistor gate voltage	V_{LG}	Supplied internally					V
Output gate voltage	V_{OG}	Supplied internally					V

■ Absolute Maximum Ratings and Operating Conditions (continued)

Parameter		Symbol	Rating		Operating condition			Unit
			min	max	min	typ	max	
Protection P-well voltage		V_{PT} *2	– 10.0	0.2	$\phi_{V(L)}$ – 1.2	$\phi_{V(L)}$ – 1.0	$\phi_{V(L)}$ – 0.7	V
P-well voltage		V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage	H-L	$V_{\phi R(H-L)}$ *3	—	15	4.7	5.0	5.3	V
	Bias	$V_{\phi R(Bias)}$ *3	– 0.2	—	Supplied internally			V
Horizontal register clock pulse voltage 1		$V_{\phi H1(H)}$	—	15	4.7	5.0	5.3	V
		$V_{\phi H1(L)}$	– 0.2	—	0	0	0	
Horizontal register clock pulse voltage 2		$V_{\phi H2(H)}$	—	15	4.7	5.0	5.3	V
		$V_{\phi H2(L)}$	– 0.2	—	0	0	0	
Vertical shift register clock pulse voltage 1		$V_{\phi V1(H)}$ *2	—	18	14.5	15.0	15.5	V
		$V_{\phi V1(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V1(L)}$ *2	– 10	—	– 9.8	– 9.5	– 9.2	
Vertical shift register clock pulse voltage 2		$V_{\phi V2(M)}$ *2	—	15	– 0.2	0	0.2	V
		$V_{\phi V2(L)}$ *2	– 10	—	– 9.8	– 9.5	– 9.2	
Vertical shift register clock pulse voltage 3		$V_{\phi V3(H)}$ *2	—	18	14.5	15.0	15.5	V
		$V_{\phi V3(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V3(L)}$ *2	– 10	—	– 9.8	– 9.5	– 9.2	
Vertical shift register clock pulse voltage 4		$V_{\phi V4(M)}$ *2	—	15	– 0.2	0	0.2	V
		$V_{\phi V4(L)}$ *2	– 10	—	– 9.8	– 9.5	– 9.2	
Vertical shift register clock pulse voltage 5		$V_{\phi V5(H)}$ *2	—	18	14.5	15.0	15.5	V
		$V_{\phi V5(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V5(L)}$ *2	– 10	—	– 9.8	– 9.5	– 9.2	
Substrate voltage		V_{Sub} *1	– 0.2	40	Supplied internally			V
		ϕV_{Sub} *4			24.0	24.5	25.0	
Operating temperature		T_{opr}	– 10	70	—	25	—	°C
Storage temperature		T_{stg}	– 30	80	—	—	—	°C

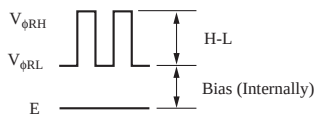
Note) 1. Standard light input defines

Standard light input is the one when the exposure is done at a lens aperture of F8, using a light source of 2856 K and 1050 nt, and placing a color temperature conversion filter LB-40 (HOYA) and an IR cutting filter CAW-500 (t = 2.5 mm) in the light path.

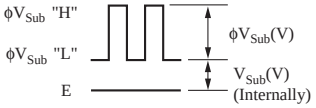
2. *1: V_{Sub} internal settings guarantee blooming at 400 times light input of the standard light input.
3. *2: V_{PT} is set so that the following conditions are set for VL of the vertical shift clock.

$V_{PT} \leqq VL$

4. *3:



5. *4: V_{Sub} when using electronic shutter function

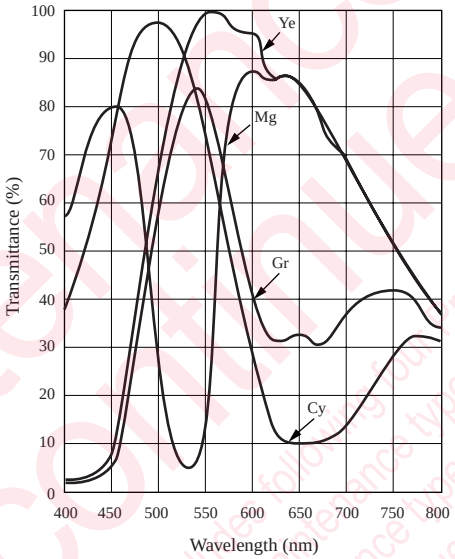


■ Optical Characteristics

Part Number	Color or B/W	Effective pixels H	Effective pixels V	S/N typ (dB)	Saturation output typ (mV)	Sensitivity F8 typ (mV)	Vertical smear Sm typ(%)	Image lag typ (%)	Horizontal resolution typ (TV-lines)	Vertical resolution typ (TV-lines)
MN37181FT	Color	771	492	60	700	300	0.01	0	480	350

■ Graphs of Characteristics

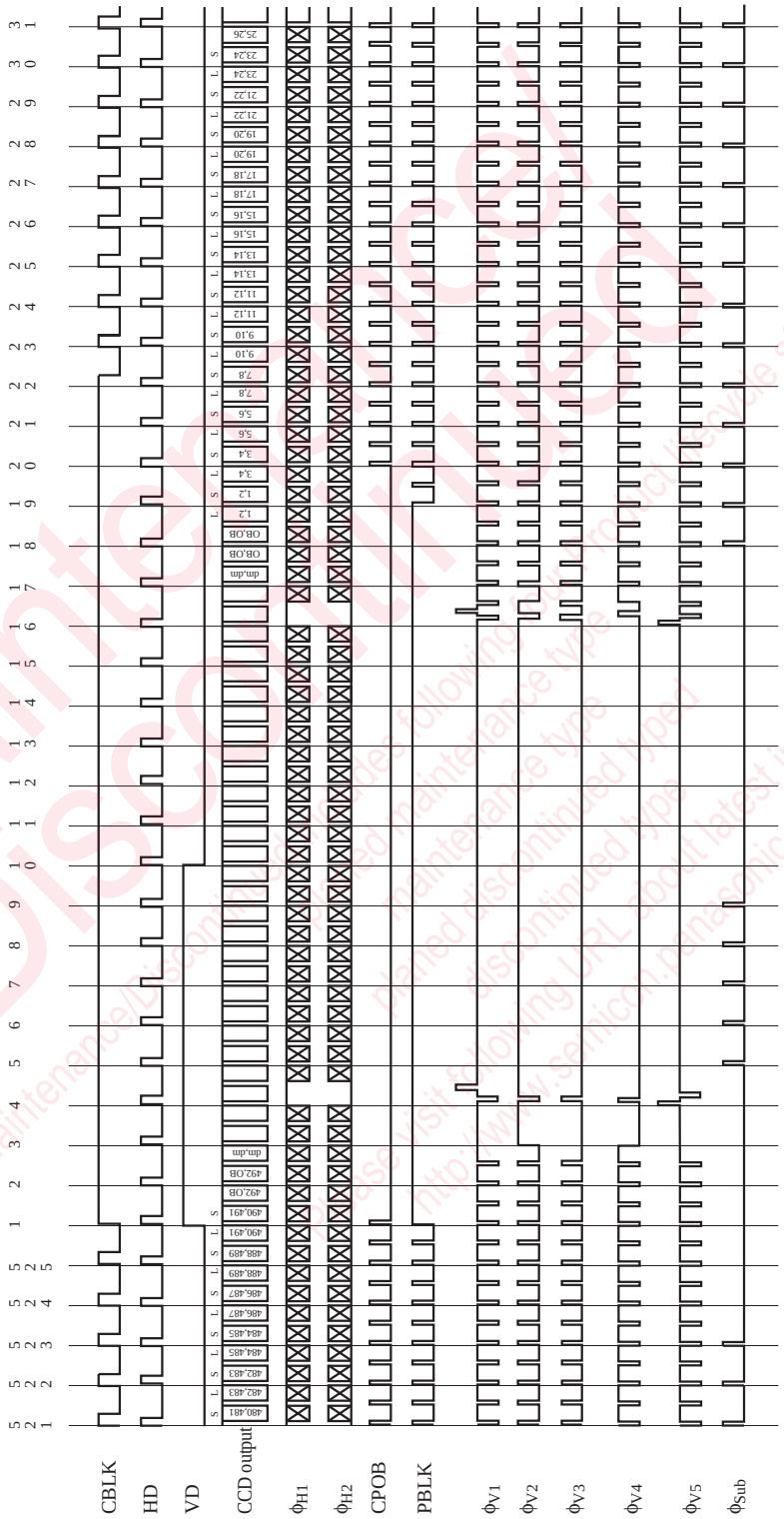
CCD On-Chip Filter Spectral Responsive Characteristics



■ Timing Diagram

• V Rate timing

< Field A >

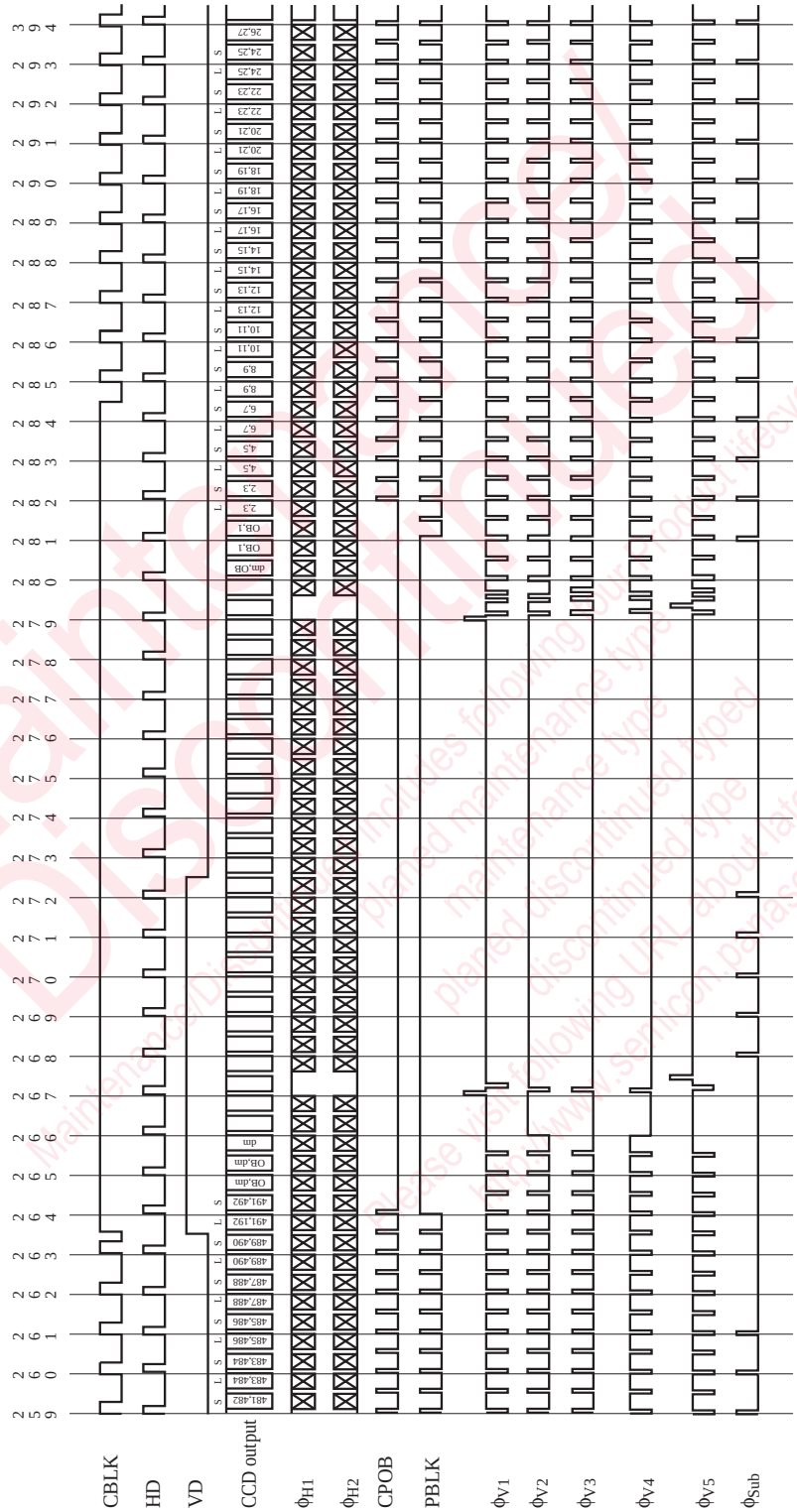


Note) 1. Signal electric charge - L: Long exposure, S: Short exposure
2. Sub applies only for shutter setting.
3. dm : Dummy

■ Timing Diagram (continued)

• V Rate timing

< Field B >

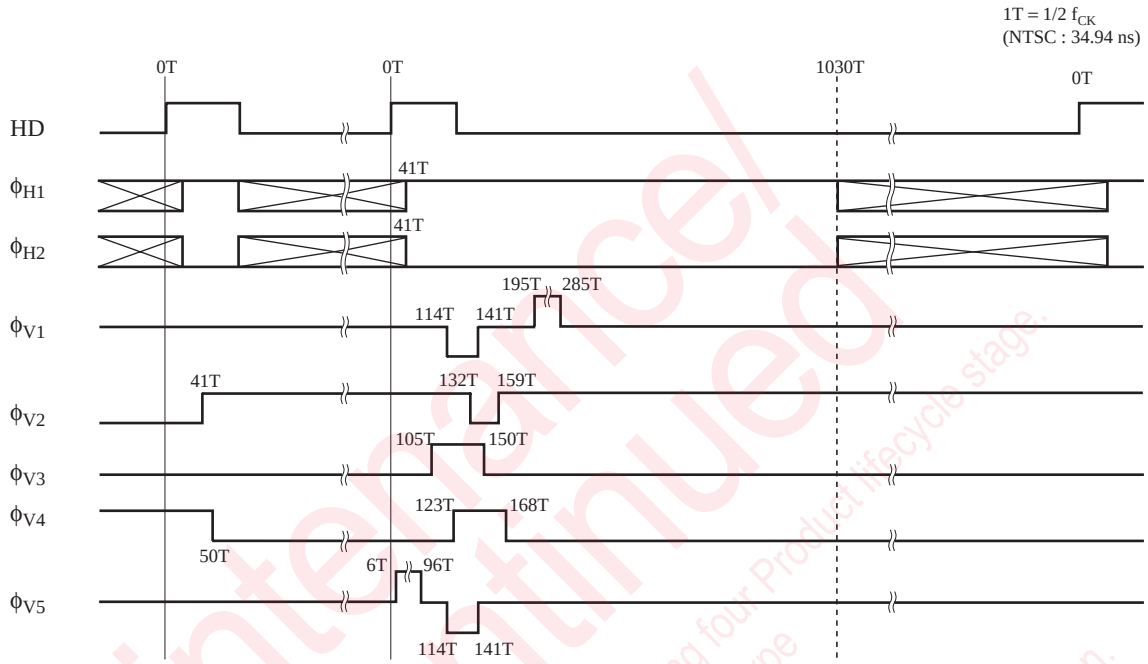


Note) 1. Signal electric charge - L: Long exposure, S: Short exposure
2. Sub applies only for shutter setting.
3. dm : Dummy

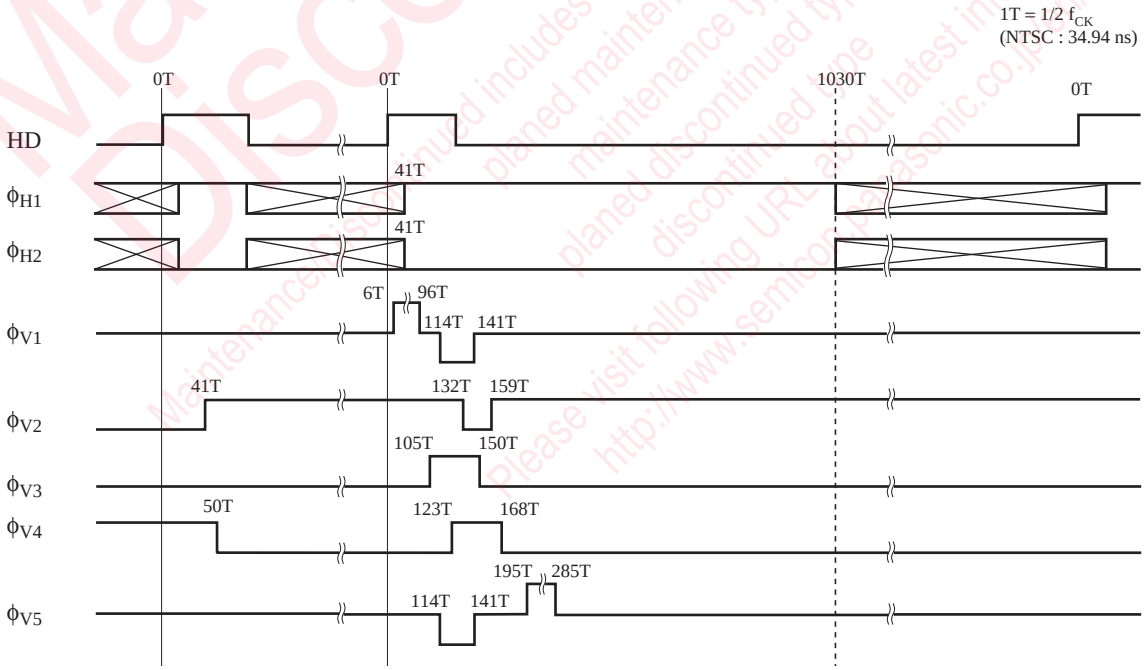
■ Timing Diagram (continued)

• V Rate timing

< Readout enlargement on Long side (Field A)>



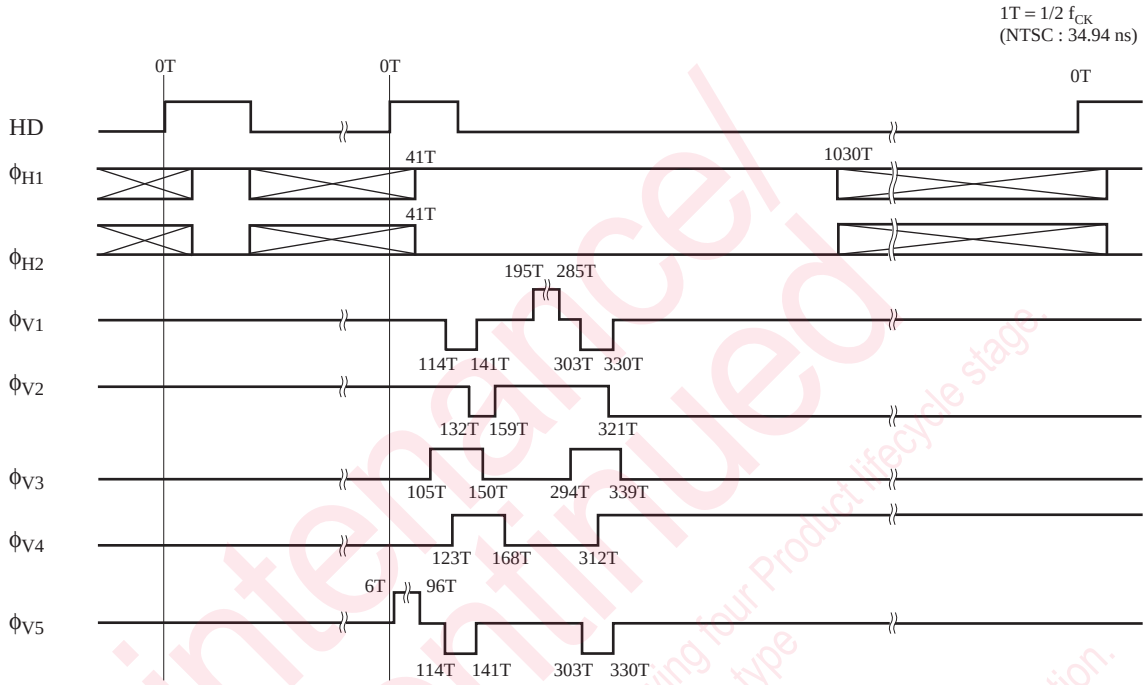
< Readout enlargement on Long side (Field B) >



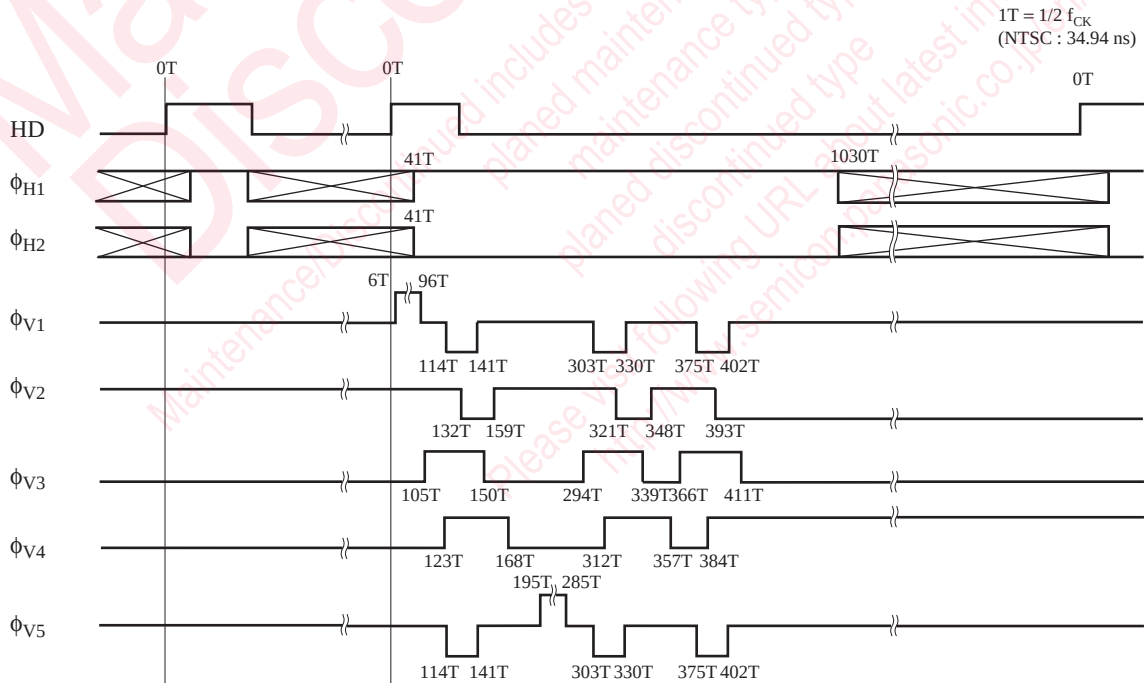
■ Timing Diagram (continued)

• V Rate timing (continued)

< Readout enlargement on short sides (Field A) >

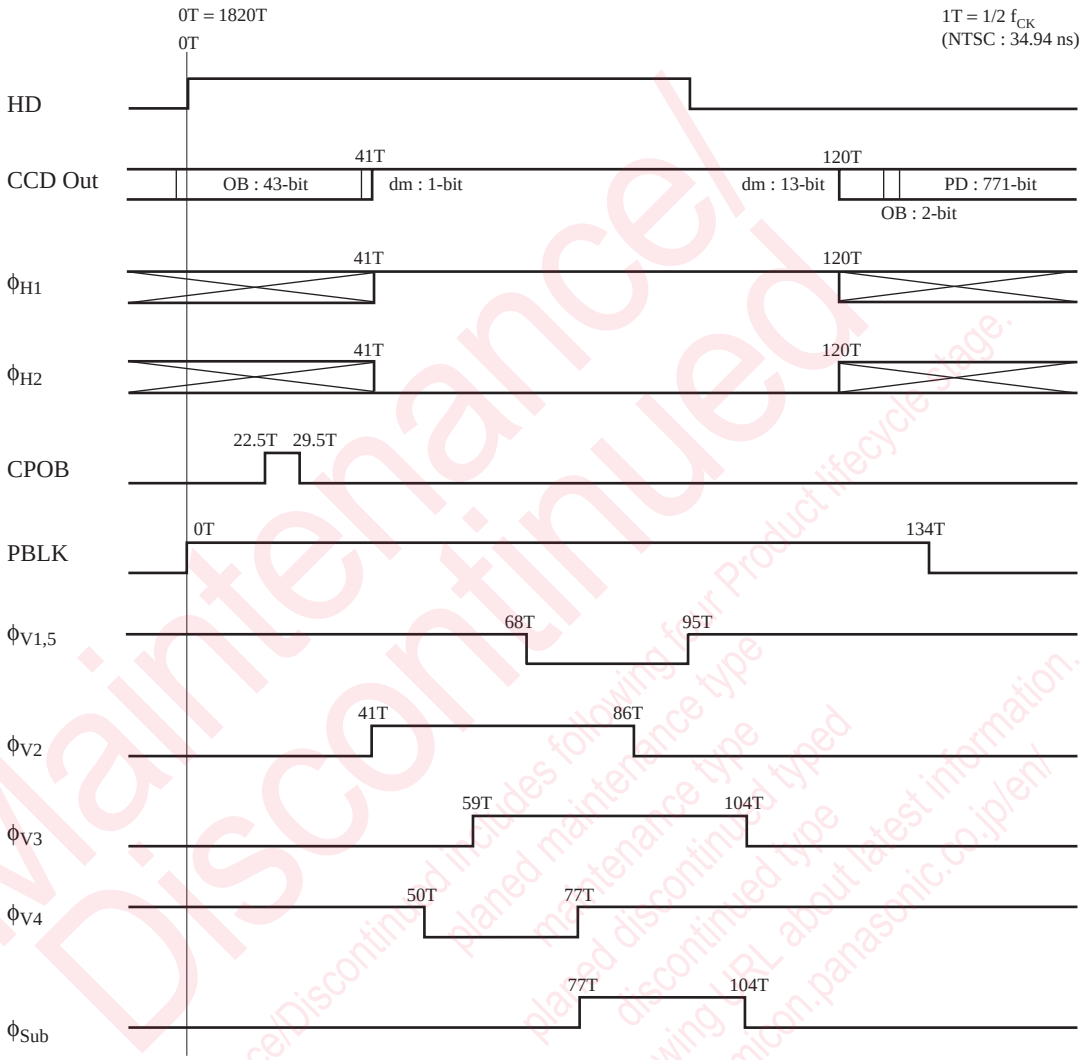


< Readout enlargement on short side (Field B) >



■ Timing Diagram (continued)

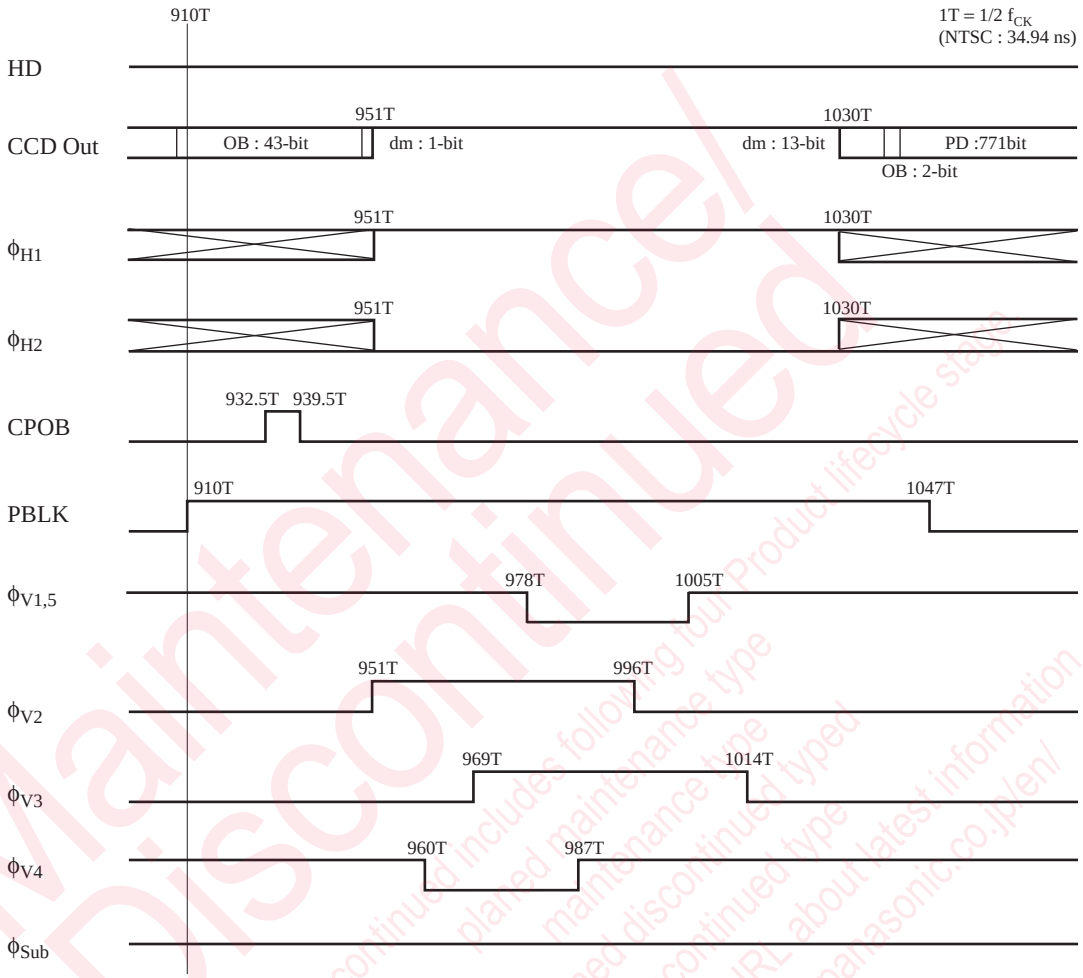
• H Rate timing chart 1



Note) dm : Dummy

■ Timing Diagram (continued)

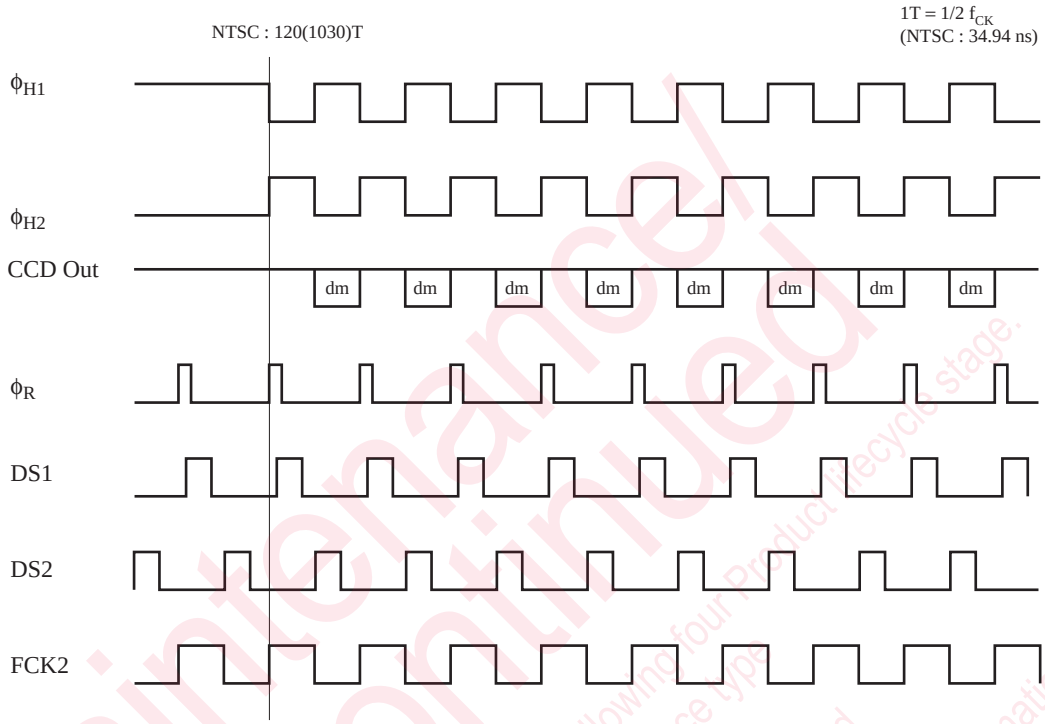
• H Rate timing chart 2



Note) dm : Dummy

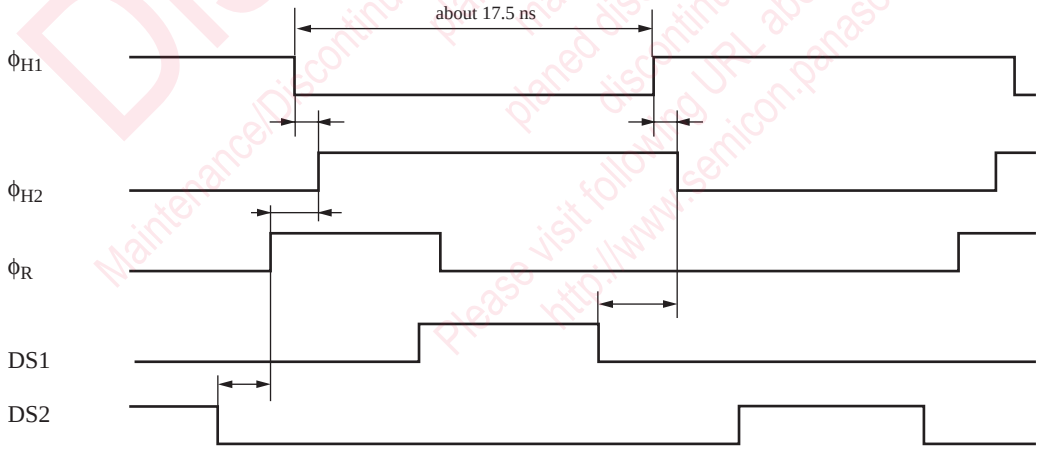
■ Timing Diagram (continued)

• High speed pulse timing



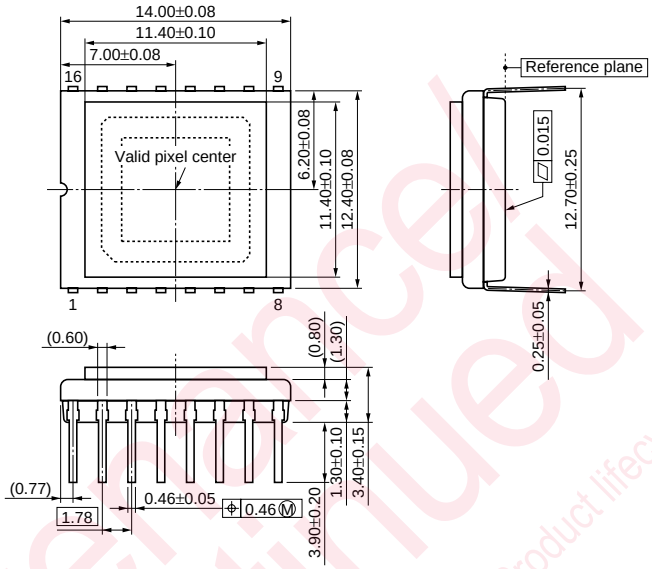
Note) dm : Dummy

< Details >



■ Package Dimensions (Unit：mm)

• WDIP016-P-0500C



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