WIDE DRAM

2 MEG x 8 DRAM

5.0V, FAST-PAGE-MODE (MT4C2M8A1/2)
3.0/3.3V, FAST-PAGE-MODE (MT4LC2M8A1/2)

FEATURES

- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: 12 row-addresses, 9 column-addresses (64ms)
- High-performance CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- Low power, 5mW standby; 400mW active, typical (5V)
- All device pins are TTL-compatible
- 4,096-cycle refresh (2,048-cycle refresh available as MT4(L)C2M8B1/2)
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8A2 only)

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Power Supply	
5V ±10% only	4C
3.0/3.3V ±10% only	4LC
• MASKED WRITE	
Not available	A1
Available	A2
• Packages	
Plastic 28-pin SOJ (400 mil)	DJ
Plastic 28-pin TSOP (400 mil)	TG
Plastic 32-pin SOJ (400 mil)	DL
Plastic 32-pin TSOP (400 mil)	TL

- Part Number Example: MT4LC2M8A1DJ-6

PART DESCRIPTION

MT4C2M8A1	5V, NONMASKED WRITE
MT4C2M8A2	5V, MASKED WRITE
MT4LC2M8A1	3.0/3.3V, NONMASKED WRITE
MT4LC2M8A2	3.0/3.3V, MASKED WRITE

PIN ASSIGNMENT (Top View)

28-Pin SOJ (DC-4) / 28-Pin TSOP (DD-3)

Signal	Pin	Pin	Signal
Vcc	1	28	Vss
DQ1	2	27	DQ8
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
$\overline{\text{WE}}$	6	23	$\overline{\text{CAS}}$
$\overline{\text{RAS}}$	7	22	$\overline{\text{OE}}$
*A11	8	21	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

32-Pin SOJ (DC-5) / 32-Pin TSOP (DD-4)

Signal	Pin	Pin	Signal
Vcc	1	32	Vss
DQ1	2	31	DQ8
DQ2	3	30	DQ7
DQ3	4	29	DQ6
DQ4	5	28	DQ5
NC	6	27	$\overline{\text{CAS}}$
$\overline{\text{WE}}$	7	26	$\overline{\text{OE}}$
$\overline{\text{RAS}}$	8	25	NC
NC	9	24	NC
*A11	10	23	A9
A10	11	22	A8
A0	12	21	A7
A1	13	20	A6
A2	14	19	A5
A3	15	18	A4
Vcc	16	17	Vss

*NC on 11 row-address version

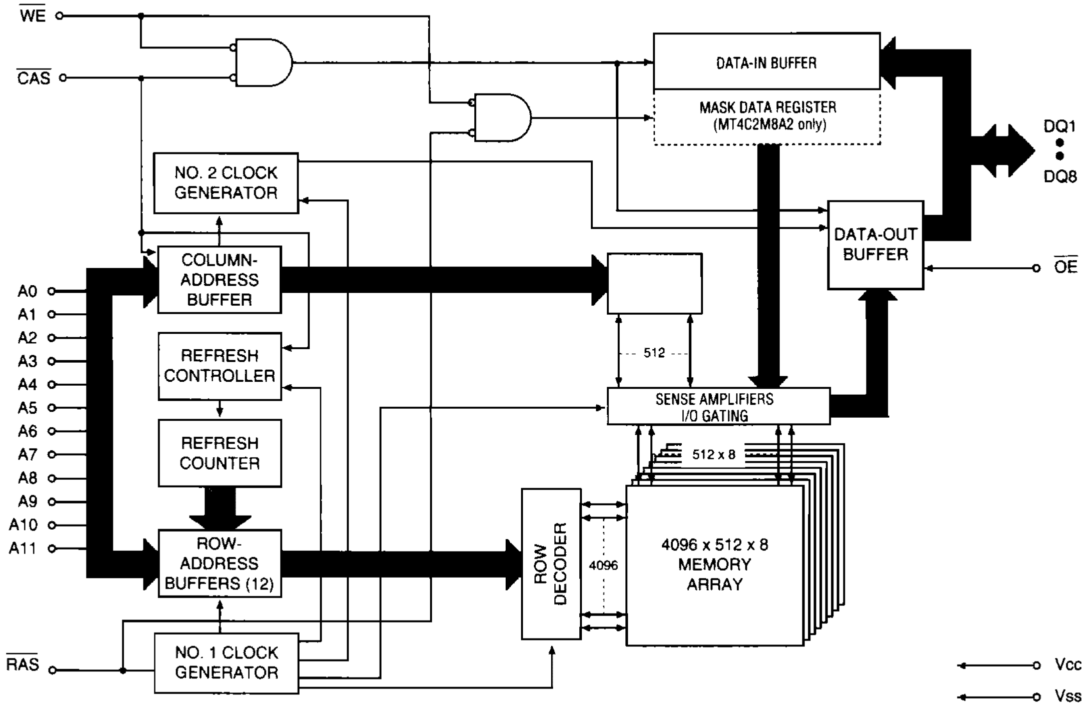
GENERAL DESCRIPTION

The MT4C2M8A1/2 and MT4LC2M8A1/2 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8A1/2 and the MT4LC2M8A1/2 are the same DRAM versions except that the MT4LC2M8A1/2 are low voltage versions of the MT4C2M8A1/2. The MT4LC2M8A1/2 are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made to the MT4C2M8A1/2 also apply to the MT4LC2M8A1/2, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by $\overline{\text{RAS}}$ latching 12 bits (A0-11) and then $\overline{\text{CAS}}$ latching 9 bits (A0-A9).

The MT4C2M8A2 has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM
4096 ROWS



PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 12 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C2M8A2 only).
23	27	$\overline{CAS}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
6	7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a mask enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED WRITE cycle (MT4C2M8A2).
22	26	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
10-13, 16-21, 9, 8	12-15, 18-23, 11, 10	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only).
	6, 9, 24, 25	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	Vcc	Supply	Power Supply: +5V ±10% (C), 2.7V to 3.6V (LC)
15, 28	17, 32	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First, RAS is used to latch 12 bits (A0-A11) then, CAS latches 9 bits (A0-A8).

The CAS control also determines whether the cycle will be a refresh cycle (RAS-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW.

READ or WRITE cycles are selected by WE. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by OE and WE.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-12) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS-ONLY, CBR, or HIDDEN) so that all 4,096 combinations of RAS addresses (A0-11) are executed at least every 64ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

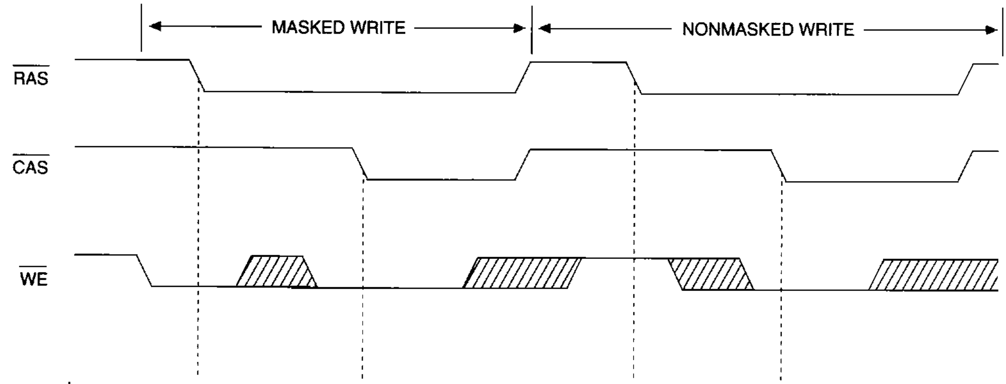
MASKED WRITE ACCESS CYCLE (MT4C2M8A2 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of WE at RAS time. A MASKED WRITE is selected when WE is LOW at RAS time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8A2 MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).



	STORED DATA	MASK DATA	INPUT		STORED DATA
DQ1	1	0	X		1
•	1	1	0	------>	0
•	1	0	X		1
•	1	1	0	------>	0
	1	0	X		1
	1	1	0	------>	0
	1	0	X		1
DQ8	1	1	0	------>	0

ADDRESS 0

STORED DATA	MASK DATA	INPUT DATA		STORED DATA
1	X	1	------>	1
0	X	1	------>	1
1	X	1	------>	1
0	X	1	------>	1
1	X	0	------>	0
0	X	0	------>	0
1	X	0	------>	0
0	X	0	----->	0

ADDRESS 1

X = NOT EFFECTIVE (DON'T CARE)

DON'T CARE

Figure 1
MT4C2M8A2 MASKED WRITE EXAMPLE

WIDE DRAM

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1, 2
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided (MT4C2M8A2 only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss (5V) ....-1V to +7V
Voltage on Vcc supply relative to Vss (3V) ....-1V to +4.6V
Operating Temperature, T_A (ambient) ....0°C to +70°C
Storage Temperature (plastic) ....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.1mA)	VOL		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; Vcc = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	90	mA	3, 32
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	90	mA	3

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; Vcc = 2.7V to 3.6V)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	90	mA	3, 32
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	90	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
READ-WRITE cycle time	^{t}RWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		95		100		ns	
Access time from RAS	^{t}RAC		60		70		80	ns	14
Access time from CAS	^{t}CAC		15		20		20	ns	15
Output Enable	^{t}OE		15		15		15	ns	
Access time from column-address	^{t}AA		30		35		40	ns	
Access time from CAS precharge	^{t}CPA		35		40		45	ns	
RAS pulse width	^{t}RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST-PAGE-MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^{t}RSH	15		20		20		ns	
RAS precharge time	^{t}RP	40		50		60		ns	
CAS pulse width	^{t}CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^{t}CSH	60		70		80		ns	
CAS precharge time	^{t}CPN	10		10		10		ns	16
CAS precharge time (FAST-PAGE-MODE)	^{t}CP	10		10		10		ns	
RAS to CAS delay time	^{t}RCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	^{t}CRP	5		5		5		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Row-address hold time	^{t}RAH	10		10		10		ns	
RAS to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Column-address setup time	^{t}ASC	0		0		0		ns	
Column-address hold time	^{t}CAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	^{t}AR	50		55		60		ns	
Column-address to RAS lead time	^{t}RAL	30		35		40		ns	
Read command setup time	^{t}RCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^{t}RRH	0		0		0		ns	19
CAS to output in Low-Z	^{t}CLZ	3		3		3		ns	33
Output buffer turn-off delay	^{t}OFF	3	15	3	20	3	20	ns	20, 29, 33

WIDE DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

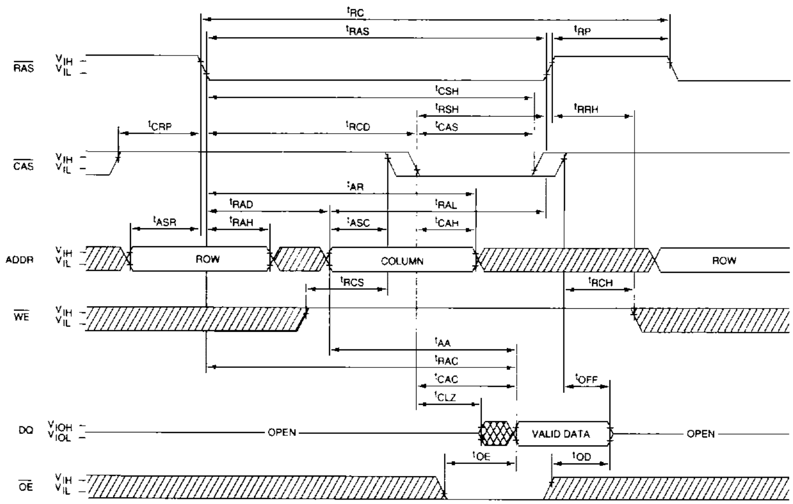
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	10		15		15		ns	26
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	tRWL	15		20		20		ns	26
Write command to CAS lead time	tCWL	15		20		20		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Column-address to WE delay time	tAWD	55		60		65		ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	tREF		64		64		64	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CBR REFRESH)	tCSR	5		5		5		ns	5
CAS hold time (CBR REFRESH)	tCHR	15		15		15		ns	5
WE hold time (MASKED WRITE and CBR REFRESH)	tWRH	15		15		15		ns	26
WE setup time (CBR REFRESH)	tWRP	10		10		10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Output disable	tOD	3	15	3	15	3	15	ns	29, 33
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		15		ns	28

NOTES

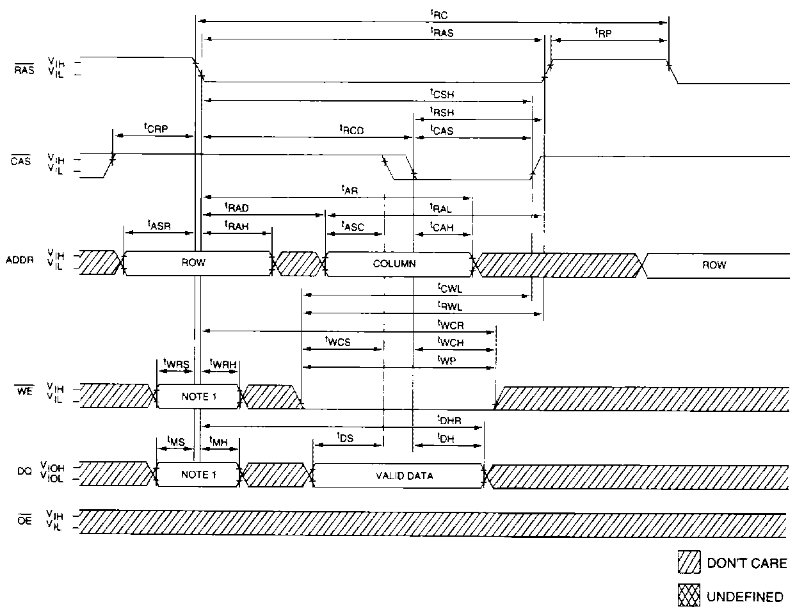
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C2M8A2 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
30. The 5V version is restricted to operate between 4.5 V and 5.5V only.
31. The 3.0/3.3V version is restricted to operate between 2.7V and 3.6V only. The -6 speed version is only valid for V_{CC} = 3.09V to 3.6V whereas the -7 and -8 speed versions are valid for V_{CC} = 2.7V to 3.6V.
32. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
33. The 3ns minimum is a parameter guaranteed by design.

WIDE DRAM

READ CYCLE

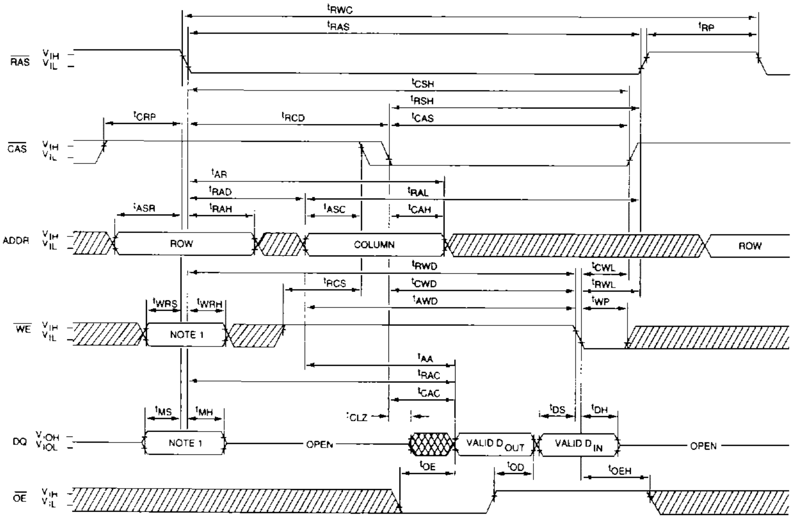


EARLY-WRITE CYCLE

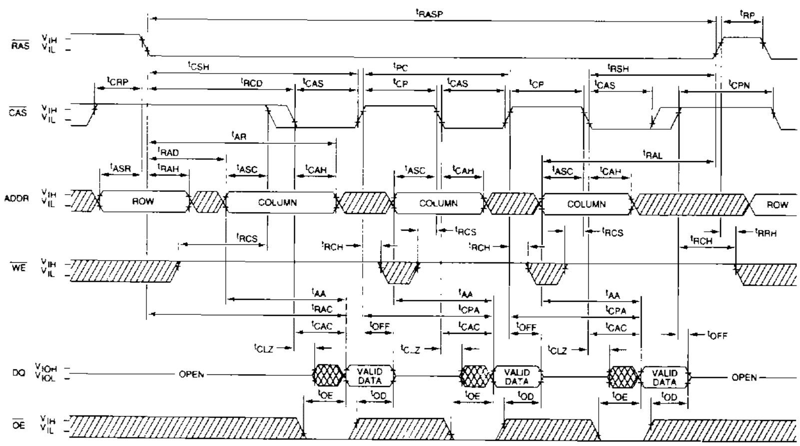


NOTE: 1. Applies to MT4C2M8A2 only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE

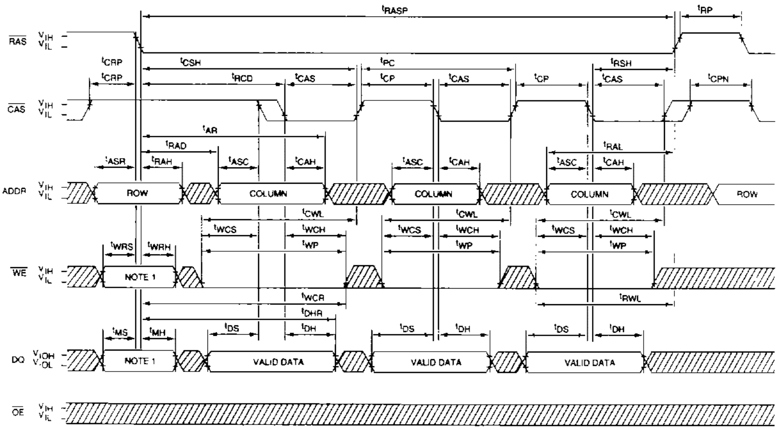


DON'T CARE

UNDEFINED

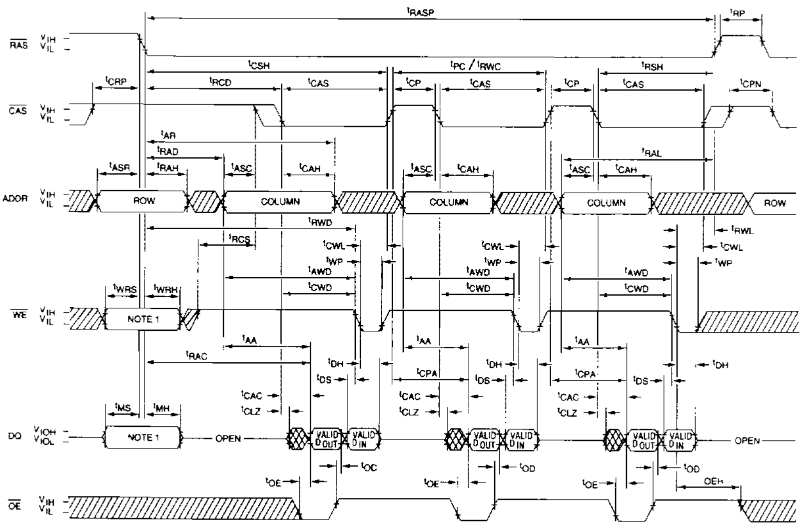
NOTE: 1. Applies to MT4C2M8A2 only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE

(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

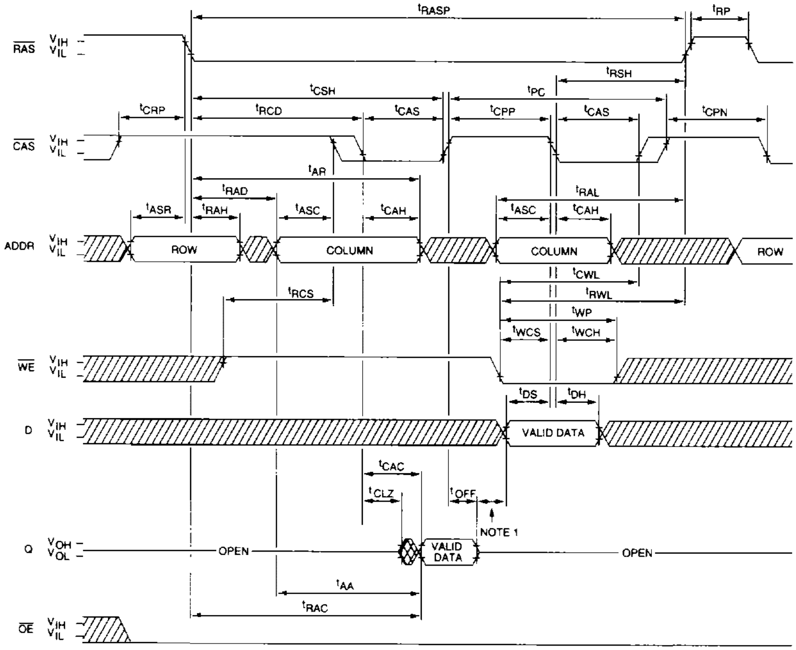


DON'T CARE

UNDEFINED

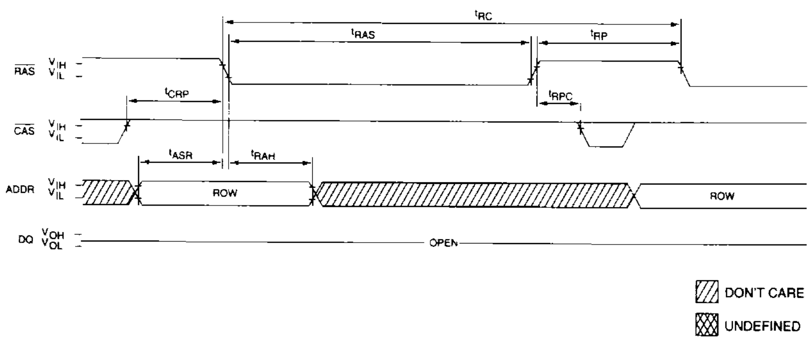
NOTE: 1. Applies to MT4C2M8A2 only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

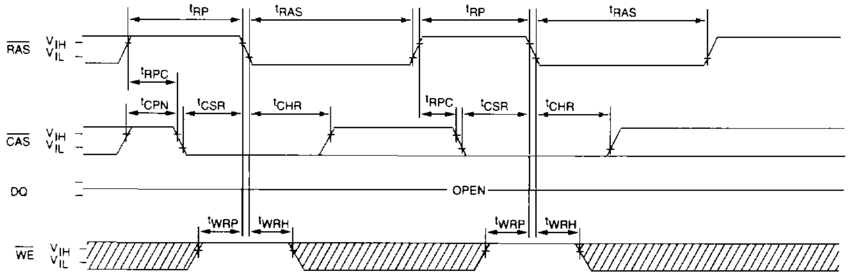


NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A11; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)