DESCRIPTION

The 82S114 and 82S115 are field programmable and include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S114 and 82S115 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S114/115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S114/115, F.

FEATURES

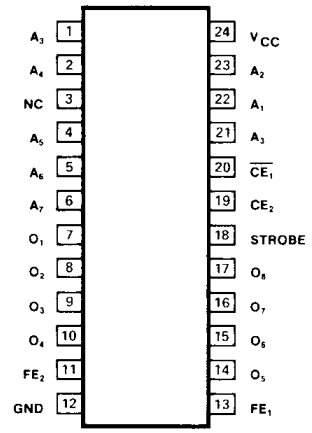
- **Address access time:**
  N82S114/115: 60ns max
  S82S114/115: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S114/115: -100μA max
  S82S114/115: -150μA max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**

APPLICATIONS

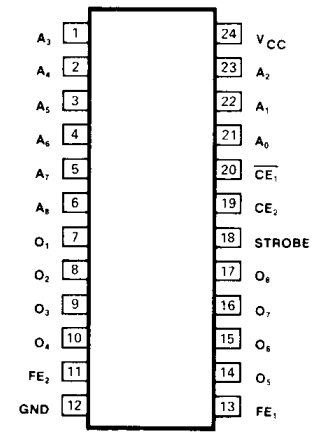
- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS

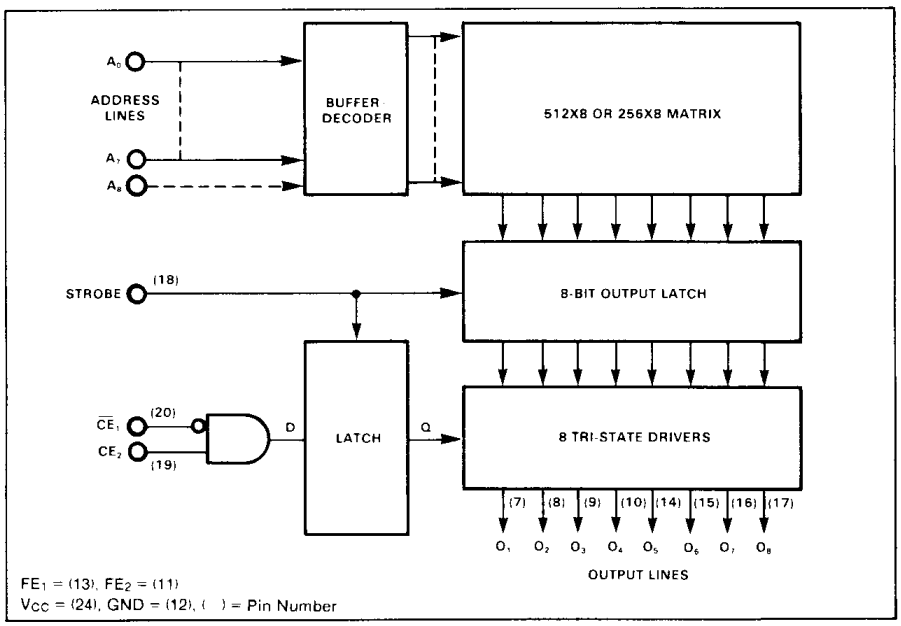
F,N PACKAGE
82S114



F,N PACKAGE
82S115



BLOCK DIAGRAM



FE1 = (13), FE2 = (11)
VCC = (24), GND = (12), ( ) = Pin Number

BIPOLAR MEMORY

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S114/115	0 to +75	
	S82S114/115	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S114/115: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S114/115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[6]	N82S114/115			S82S114/115			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA		0.4	0.45		0.4	0.5	
V_{OH}	High	$\overline{CE}_1$ = Low, CE_2 = High, I_{OUT} = -2mA, High stored	2.7	3.3		2.4	3.3		
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_1$ = High or CE_2 = O, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE}_1$ = High or CE_2 = O, V_{OUT} = 0.5V			-40			-100	
I_{OS}	Short circuit[2]	V_{OUT} = OV	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	185	mA
	Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V							pF
C_{IN}	Input	V_{CC} = 5.0V, V_{OUT} = 2.0V		5			5		
C_{OUT}	Output	$\overline{CE}_1$ = High or CE_2 = 0		8			8		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S114/115: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S114/115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

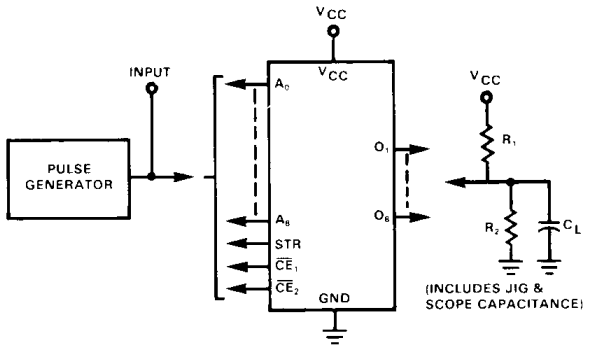
PARAMETER	TO	FROM	TEST CONDITIONS	N82S114/115			S82S114/115			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
Access time			Latched or transparent read[3,5]							ns
T_{AA}[7]	Output	Address			35	60		35	90	
T_{CE}	Output	Chip enable			20	40		20	50	
Disable time										ns
T_{CD}	Output	Chip disable			20	40		20	55	
Setup and hold time			Latched read only[4,5]							ns
T_{CDS} Setup time	Output	Chip enable		40			50			
T_{CDH} Hold time				10	0		15	0		
T_{ADH} Hold time	Output	Address		0	-10		5	-10		
Pulse width										ns
T_{SW} Strobe				30	20		40	20		
Latch time										ns
T_{SL} Strobe				60	35		90	35		
Delatch time										ns
T_{DL} Strobe						30			45	

NOTES on following page.

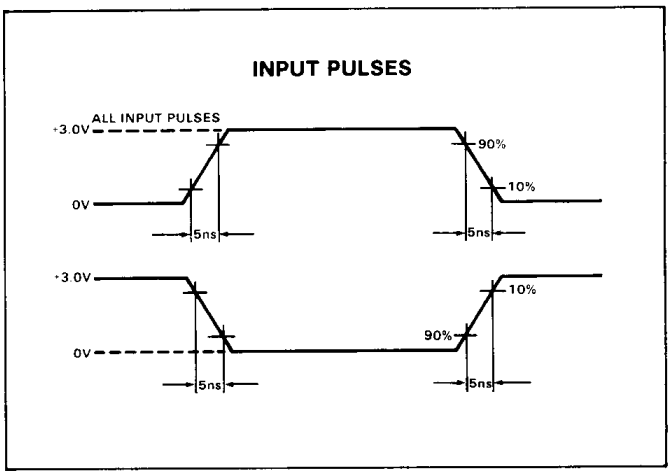
NOTES

1. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
3. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
4. In latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
5. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
6. Positive current is defined as into the terminal referenced.
7. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT

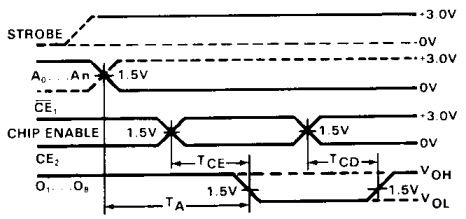


VOLTAGE WAVEFORM



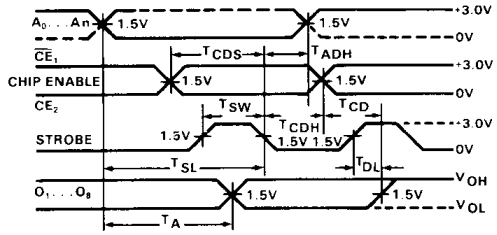
TIMING DIAGRAMS

TRANSPARENT READ [4]



Output Latches Not Used

LATCHED READ [5]



Output Latches Used

PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 200 ± 25mA, Transient or steady state	4.75	5.0	5.25	V
	Verify limit					V
V_{CCVH}	Upper		5.3	5.5	5.7	
V_{CCVL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
I_{CCP}	Programming supply current	V_{CCP} = +5.0 ± .25V	175	200	225	mA
	Input voltage					V
V_{IL}	Low		0	0.4	0.8	
V_{IH}	High		2.4		5.5	
	Input current (FE_1 & FE_2 only)					
I_{IL}	Low	V_{IL} = +0.45V			-100	μA
I_{IH}	High	V_{IH} = +5.5V			10	mA
	Input current (except FE_1 & FE_2)					μA
I_{IL}	Low	V_{IL} = +0.45V			-100	
I_{IH}	High	V_{IH} = +5.5V			25	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	FE_2 programming pulse width		0.3	0.4	0.5	ms
T_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 3ms.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical low. To write logical high, proceed as follows:

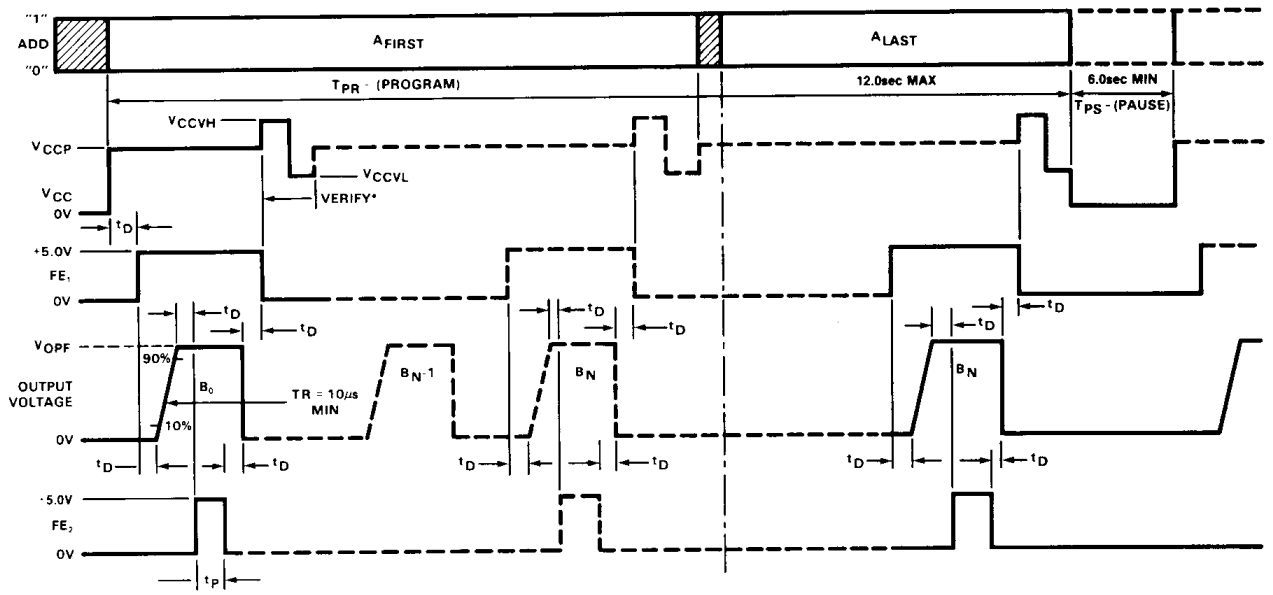
SET-UP

1. Apply GND to pin 12.
2. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
3. Set $\overline{CE}_1$ to logic low, and CE_2 to logic high (TTL levels).
4. Set Strobe to logic high level.

Program-Verify Sequence

1. Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After 10μs delay, apply to FE_1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10mA sourcing current capability.
3. After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit 200mA. Program on output at the time.
4. After 10μs delay, raise FE_2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10mA sourcing current capability.
5. After 10μs delay, remove +17.0V supply from programmed output.
6. To verify programming, after 10μs delay, return FE_1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} and repeat steps 2 through 6 to program other bits at the same address.
8. Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

BIPOLAR MEMORY