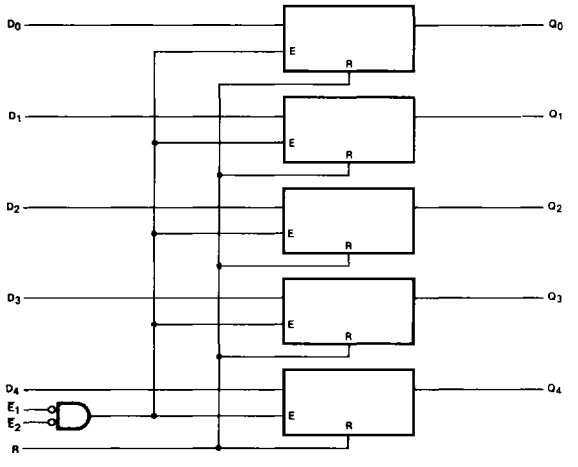
F10175 • F10575
QUINT LATCH

DESCRIPTION — The F10175 and F10575 are high-speed low-power Quint Latches. They feature five D type latches with common Reset and a common 2-input Enable. Data is transferred on the negative edge of the enable and latched on the positive edge. The two Enable inputs are OR-ed together. Propagation delays are typically 2.5 ns from each Data input to the output.

Any change on the Data input appears at the outputs while the Enable inputs are LOW. The outputs are latched on the positive transition of the Enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information. The Reset input is enabled only when the Enable is in the HIGH state.

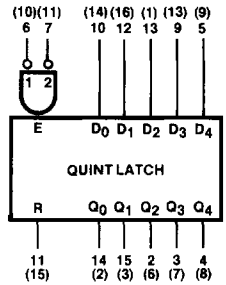
PIN NAMES

D_n	Data Inputs
$\overline{E}_n$	Enable Inputs (Active LOW)
R	Reset
Q_n	Outputs



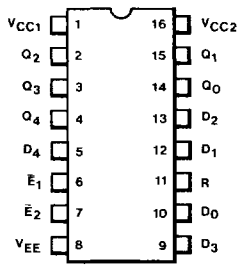
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

D	$\bar{E}_0$	$\bar{E}_1$	R	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q_n
X	X	H	L	Q_n
X	H	X	H	L
X	X	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

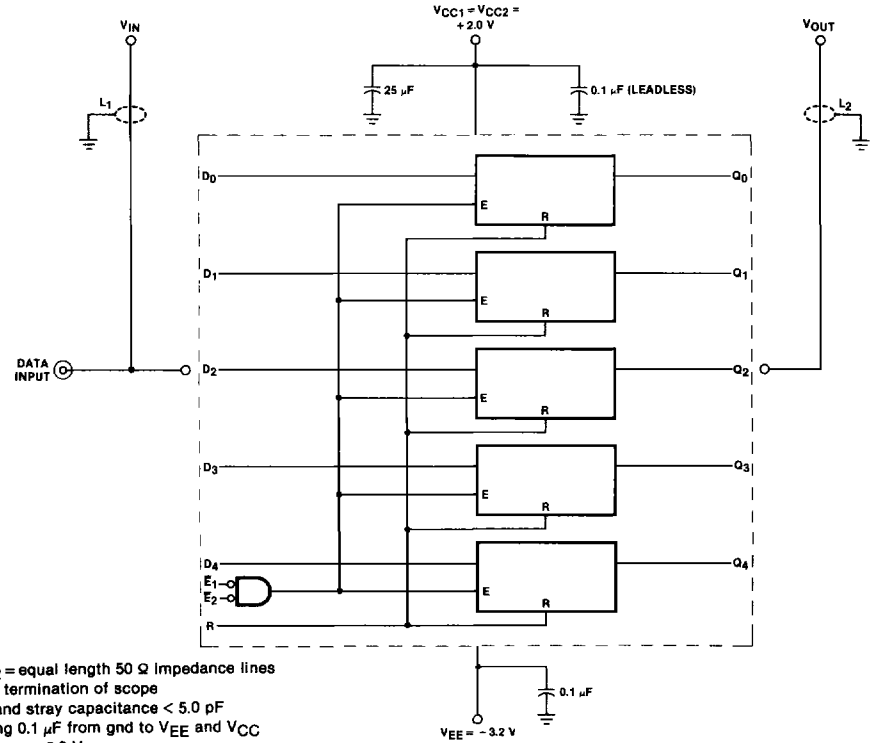
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH Data Enable Reset			 290 645	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−97			mA	25°C	Inputs and Outputs Open

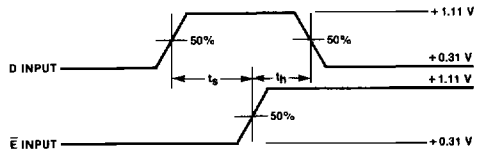
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay Enable to Output	1.0	3.3	4.3	ns	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	1.0	2.5	3.5	ns	
t_{PHL}, t_{PLH}	Propagation Delay Reset to Output	1.0	2.5	3.9	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	See Figure 1
t_s	Set-Up Time Data	2.5	1.5		ns	
t_h	Hold Time Data	1.5	0.5		ns	

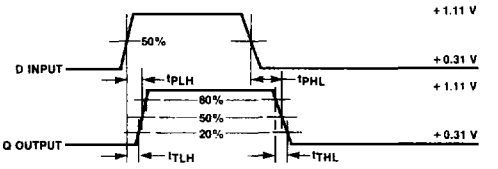
SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V



DATA TO OUTPUT (ENABLE LOW)

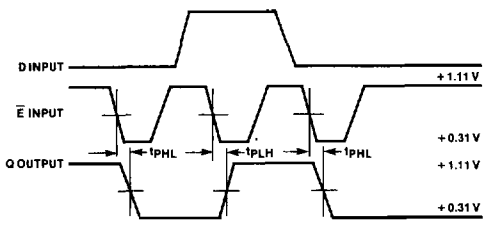


NOTE:

t_s is the minimum time before the positive transition of the enable that information must be present at the data input (D).

t_h is the minimum time after the positive transition of the enable pulse that information must remain unchanged at the data input (D).

ENABLE TO OUTPUT



RESET TO OUTPUT (DATA HIGH)

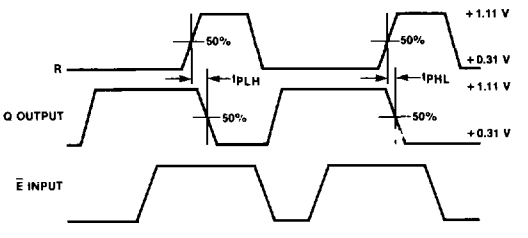


Fig. 1