## INTEGRATED CIRCUIT **TOSHIBA**

TECHNICAL DATA

TOSHIBA MOS INTEGRATED CIRCUIT TC5332201 AP SILICON GATE CMOS

32 MBIT (4,194,304 WORD BY 8 BITS) CMOS MASK ROM

#### **DESCRIPTION**

The TC5332201AP is a 33,554,432-bit Read Only Memory organized as 4,194,304 words by 8 bits. The TC5332201AP is most suitable for application such as program memory, data memory, and character generators.

The TC5332201AP is packaged in a standard 600 mil 42-pin DIP.

#### **FEATURES**

Single 5 V Power Supply

Access Time: 120 ns (max)

Power Dissipation

Operating Current: 45 mA (max) Standby Current: 100 µA (max) Fully Static Operation

• All Inputs and Outputs: TTL Compatible

• Three State Outputs

• TC5332201AP: DIP42-P-600

#### PIN ASSIGNMENT (TOP VIEW)

A19 🛭	1	$\cup$	42	A20
A18 🛭	2		41	] A9
A8 [	3		40	A10
A7 🛚	4		39	<u></u> 11 ∆ [
A6 🛚	5		38	D A12
A5 [	6		37	[] A13
A4 🛭	7		36	D A14
A3 [	8		35	D A15
A2 [	9		34	A16
A1 [	10		33	A17
CE [	11		32	A21
GND [	12		31	GND
OE [	13		30	<u> </u> 40
D0 [	14		29	D7
DC [	15		28	DC
D1 [	16		27	Ď D6
DC [	17		26	DC DC
D2 L	18		25	D5
DC [	19		24	DC DC
D3 🛚	20		23	D4
DC [	21		22	DADD
				•

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#### PIN NAMES

A0 to A21	Address Inputs
D0 to D7	Data Outputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
DC	Don't Care Connection
$V_{DD}$	Power Supply
GND	Ground

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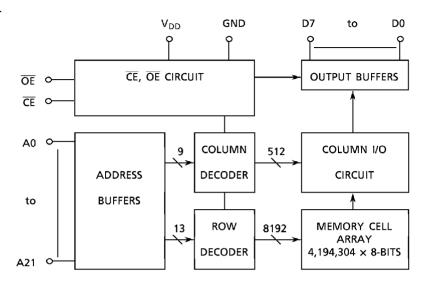
## INTEGRATED CIRCUIT

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### **BLOCK DIAGRAM**



### **MODE SELECTION**

MODE	CE	ŌĒ	D0 to D7	POWER
Read (8-Bit)	L	L	Data Out	Active
Output Deselect	L	Н	High Impedance	Active
Standby	Н	*	High Impedance	Standby

H:  $V_{IH}$  L:  $V_{IL}$  \*:  $V_{IH}$  or  $V_{IL}$ 

## **ABSOLUTE MAXIMUM RATINGS**

SYMBOL	RATING	VALUE	UNIT
$V_{DD}$	Power Supply Voltage	- 0.5 to 7.0	٧
V <sub>IN</sub>	Input Voltage	- 0.5 to 7.0	V
V <sub>OUT</sub>	Output Voltage	0 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>STG</sub>	Storage Temperature	- 55 to 150	°C
T <sub>OPR</sub>	Operating Temperature	- 10 to 70	°C
T <sub>SOLDER</sub>	Soldering Temperature (10 s)	260	°C

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# INTEGRATED CIRCUIT **TOSHIBA**

TECHNICAL DATA

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## DC RECOMMENDED OPERATING CONDITIONS (Ta = $-10^{\circ}$ to $70^{\circ}$ C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> + 0.5	٧
V <sub>IL</sub>	Input Low Voltage	- 0.3	_	0.8	V

## DC CHARACTERISTICS (Ta = $-10^{\circ}$ to $70^{\circ}$ C, $V_{DD} = 5 \text{ V} \pm 10\%$ )

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	$V_{IN} = 0$ to $V_{DD}$	-	± 5.0	μΑ
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 to V <sub>DD</sub>	-	± 5.0	μΑ
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	- 1.0	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	2.0	-	mA
I <sub>DD\$1</sub>	Standby Current	CE = V <sub>IH</sub>	-	2	mA
I <sub>DD\$2</sub>	Standby Current	$\overline{CE} = V_{DD} - 0.2 V$	-	100	μΑ
I <sub>DDO1</sub>	One and in a Course	$V_{IN} = V_{IH}/V_{IL}$ , $t_{cycle} = 120 \text{ ns}$ $I_{OUT} = 0 \text{ mA}$	-	50	mA
I <sub>DDO2</sub>	Operating Current	$V_{IN} = V_{DD} - 0.2 \text{ V/}0.2 \text{ V}$ $t_{cycle} = 120 \text{ ns, } I_{OUT} = 0 \text{ mA}$	-	45	mA

## <u>CAPACITANCE</u> (f = 1 MHz, Ta = 25°C, $V_{DD}$ = 5.0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	$V_{IN} = 0 V$	-	15	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	_	15	pF

Note: This parameter is periodically sampled and is not tested for every component.

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## INTEGRATED CIRCUIT

## **TOSHIBA**

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# AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = $-10^{\circ}$ to $70^{\circ}$ C, $V_{DD} = 5 \text{ V} \pm 10\%$ )

SYMBOL	PARAMETER	MIN	MAX	UNIT
t <sub>CYC</sub>	Cycle Time	120	_	ns
t <sub>ACC</sub>	Address Access Time	_	120	ns
t <sub>CE</sub>	Chip Enable Access Time	_	120	ns
t <sub>OE</sub>	Output Enable Access Time	_	60	ns
t <sub>CEE</sub>	Output Enable Time from CE	0	_	ns
t <sub>OEE</sub>	Output Enable Time from OE	0	-	ns
t <sub>CED</sub>	Output Disable Time from CE	_	45	ns
t <sub>OED</sub>	Output Disable Time from $\overline{\text{OE}}$	_	35	ns
t <sub>OH</sub>	Output Hold Time	5	_	ns

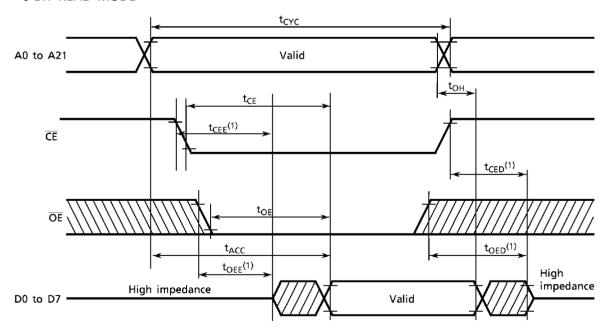
### **AC TEST CONDITIONS**

Output Load : 100 pF + 1 TTLInput Levels  $: 0.6 \, \text{V/}2.4 \, \text{V}$ Timing Measurement Reference Levels Input : 0.8 V/2.2 V

Output: 0.8 V/2.2 V

Input Rise and Fall Time : 5 ns

#### 8-BIT READ MODE



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# INTEGRATED CIRCUIT

## **TOSHIBA**

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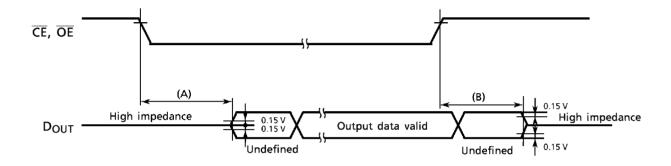
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Note 1

The following parameters are specified:

(A)  $t_{CEE},\,t_{OEE}$  ...... Output Enable Time

(B) t<sub>CED</sub>, t<sub>OED</sub> ..... Output Disable Time



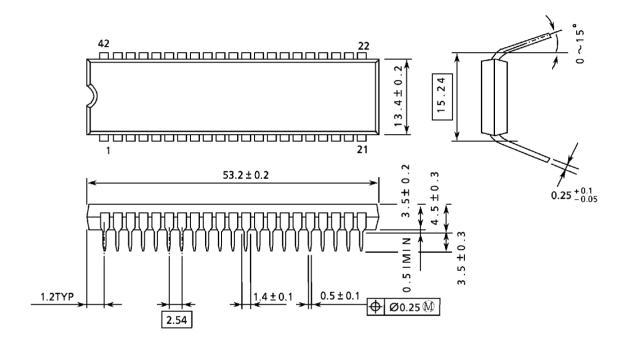
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### **PACKAGE DIMENSIONS**

• Plastic DIP
DIP42-P-600

UNITS: mm



Note: Package width and length do not include mold protrusion. The permissible mold protrusion is 0.15 mm.

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