M02046 Evaluation Module

User Guide

02046-EVMD-001-B
April, 2005

MINDSPEED™

Revision History

Revision	Level	Date	Description
B	Final	April 2005	Completely re-written and expanded.
A	Final	October 2001	Initial Release

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1.0 Operation of Evaluation Module

1.1 Functional Description

The M02046 Evaluation Module has been designed to demonstrate the performance of all versions of the M02046 in a QSOP package. The M02046 is a highly integrated limiting amplifier targeted for use in optical receivers operating up to 1.25 Gbps and is compatible in designs which currently use the Mindspeed MC2046 limiting amplifier.

The evaluation module enables the user to investigate the full functionality of the device and the programming of the signal detect level. The high speed data inputs and outputs are AC-coupled, with controlled impedance lines and good quality SMA connectors providing the interface to test equipment.

Features:

- Supports all versions of the part
  - -14 (3.3V only, CMOS ST output)
  - -15 (3.3/5V, CMOS ST output
  - -24 (3.3V only, PECL ST output)
  - -25 (3.3/5V, PECL ST output)
- SMA connectors for all high-speed I/O connections with AC-coupling to the IC allowing direct connection of inputs and outputs to test equipment
- Operates with Differential input levels up to 1200 mV_{PP}
- Signal Detected (SD) indication
- Optional ROSA connection pads

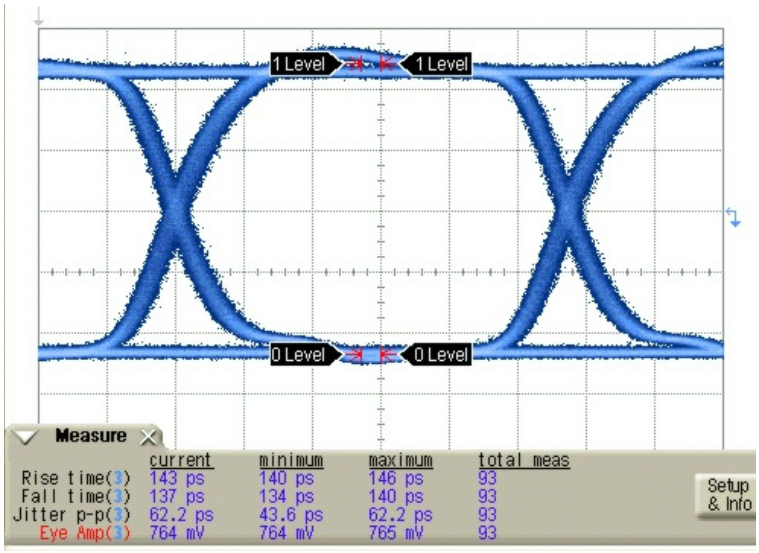
Programmability

- Selectable data output power down/squelch operation (Jam)
- Selectable Signal Detect LED operation
- Signal Detect threshold level adjustment (with resistor change)

Test Points Available

- Signal Detect and LOS Outputs
- Jam input
- VCC3 input voltage in 3.3V operation
- 3.3V regulator output voltage in 5V operation
- ST/LOS threshold setting voltage (STSet)

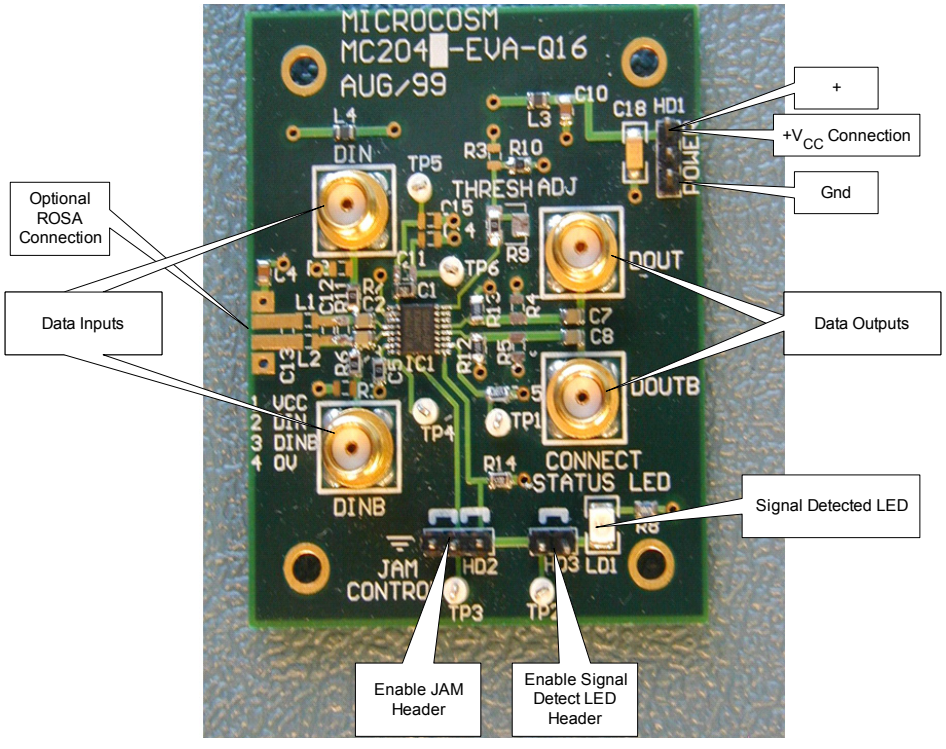
Figure 1-1. Typical 1.25 Gbps Eye Diagram



10 mV_{PP} differential input
1.25 Gbps

160 mV/div
140 ps/div

Figure 1-2. M02046 on an MC2046 EVM



1.1.1 Power

A single positive 3.3V (± 7.5%) or 5V (± 7.5%) power supply is required to power this module. Power is applied via 3 pin header HD1. Either 3.3V or 5V is applied to pin 1 and ground is connected to either pin 2 or 3. The correct polarity can be verified by C18, the 10uF electrolytic capacitor adjacent to HD1 which has a marking on its positive connection.

NOTE: This EVM supports both the 3.3V only versions of the part (-14 and -24) and the 3.3/5V versions (-15 and -25). Please note which device is present on the EVM before applying 5V.

The typical operating current of the EVM under nominal conditions is 50 - 55 mA.

1.1.2 Data Inputs

Data is applied via SMA Edge launched connectors SK1 and SK2. The module is designed to accommodate differential input signals up to 1200 mVpp (600 mV_{PP} single-ended). Since the inputs are AC-coupled, the input common mode level is rejected.

1.1.3 PECL Data Outputs

The differential data PECL outputs are available at the SMA outputs SK3 and SK4 and can be directly connected to 50 Ω test equipment. Note that a true PECL load is 50 Ω to V_{CC} - 2V. In practice, the thevenin equivalent is used because of the difficulty of creating the V_{CC} - 2V voltage. However, the thevenin equivalent has the drawback of being dependent on the actual V_{CC} voltage.

The M02046 EVM allows the user through component selection to setup several possible output termination configurations. Both outputs have two resistive connections: one provides a pull-up to V_{CC} and the other provides a pull-down to ground. Resistors R4 and R5 connect their respective output to V_{CC} while R12 and R13 connect their respective output to ground. The actual values used are determined by the value of V_{CC} and whether or not true PECL output levels are required. Table 1-1 lists the possible combinations.

NOTE: This EVM comes configured for 3.3V operation. For 5V operation first ensure the device is a -15 or -25 revision and then change the output PECL termination resistors (R12 and R13) from 150 ohm to 300 ohm.

Table 1-1. Termination Resistor Values

Supply	$R_{Pull-Down}$ (R12 and R13)	$R_{Pull-Up}$ (R4 and R5)	C_{AC} (C7 and C8)	Note
3.3 V	150	open	100 nF	**This is the default condition for the EVM.** Pseudo 3.3V PECL termination recommended for driving a BERT without reducing the edge speed. However, is not a valid PECL load and does not meet the PECL VOH and VOL requirements.
5.0 V	300	open	100 nF	Pseudo 5V PECL termination recommended for driving a BERT without reducing the edge speed. However, is not a valid PECL load and does not meet the PECL VOH and VOL requirements.
3.3 V	130	82	shorted	Thevenin equivalent 3.3V PECL termination. When driving into a high-Z load will give valid PECL voltage levels. However, voltage level exceeds the maximum input levels for a typical BERT.
5.0 V	82	130	shorted	Thevenin equivalent 5.0V PECL termination. When driving into a high-Z load will give valid PECL voltage levels. However, voltage level exceeds the maximum input levels for a typical BERT.
3.3 V	130	82	100 nF	Thevenin equivalent 3.3V PECL termination suitable for driving a BERT. However, the addition of the 50 Ω BERT input impedance will decrease the edge speed as noted below.
5.0 V	82	130	100 nF	Thevenin equivalent 5.0V PECL termination suitable for driving a BERT. However, the addition of the 50 Ω BERT input impedance will decrease the edge speed as noted below.

NOTE: Terminating the outputs with an equivalent thevenin PECL load AND AC-coupling to 50 Ω test equipment presents a load to the PECL outputs requiring more current than the defined PECL termination of 50 Ω to V_{CC} - 2V. This will attenuate the output swing slightly and reduce edge speeds seen at the 50 Ω test equipment.

1.1.4 Signal Detect (ST) and Loss of Signal Function (LOS)

The signal detect threshold is established by R_{ST} (Reference designator C1 on the EVM) between pins one (ST_{SET}) and two of the device. The default factory value is 7.50 kΩ which corresponds to an ST assert level of ~8 mV_{PP} and an ST deassert level of ~5 mV_{PP}. When the differential input voltage is greater than the programmed threshold at ST_{SET}, ST is asserted and LOS is de-asserted. Decreasing the differential input level below the ST_{SET} threshold de-asserts ST and asserts LOS. Connecting header HD3 will illuminate LED LD1 when the differential input signal is above the ST threshold, i.e. "signal present", and turn the LED off when loss of signal has occurred.

To adjust the ST threshold level, R_{ST} must be replaced with a new value. Figure 1-3 has been included to aid the selection of the appropriate resistance R_{ST} and desired ST threshold setting level.

More detailed description of the ST function is included in the data sheet.

Figure 1-3. Signal Detect Characteristic (Full Range)

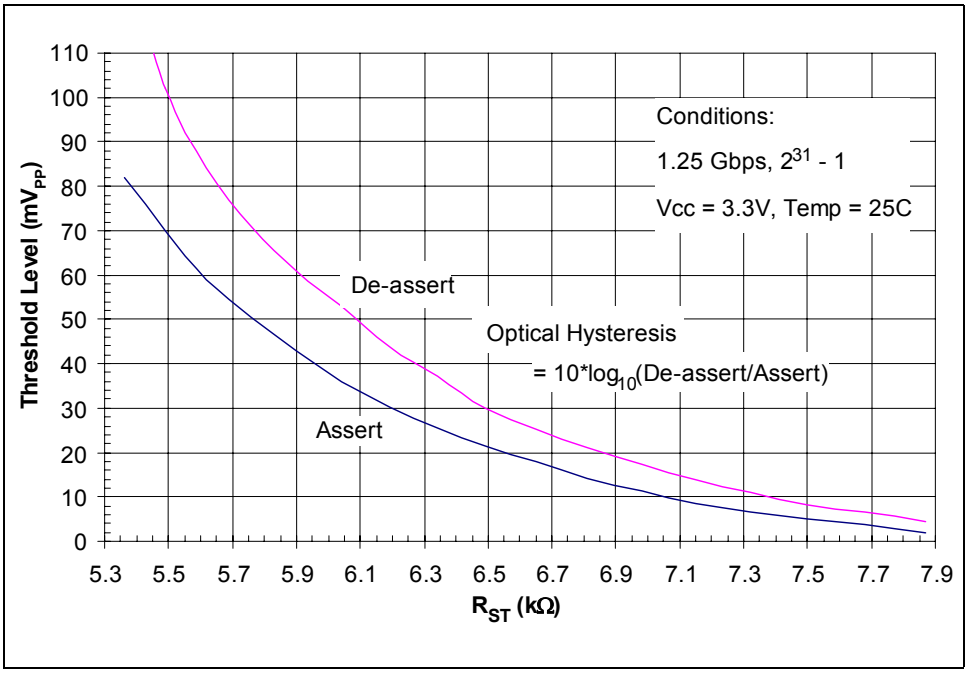


Figure 1-4. Signal Detect Characteristic (Low Input Signal)

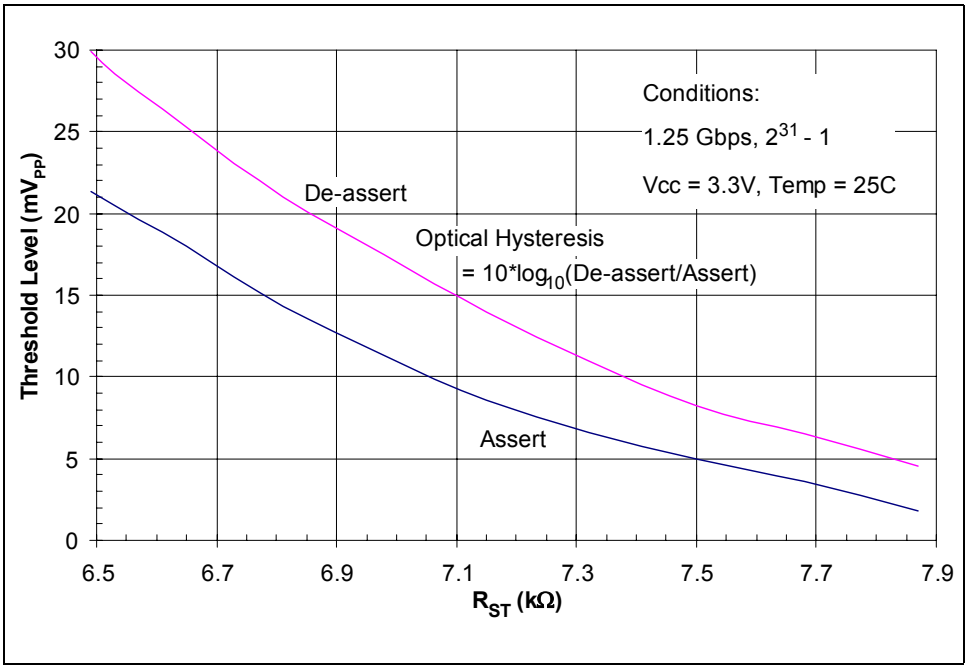
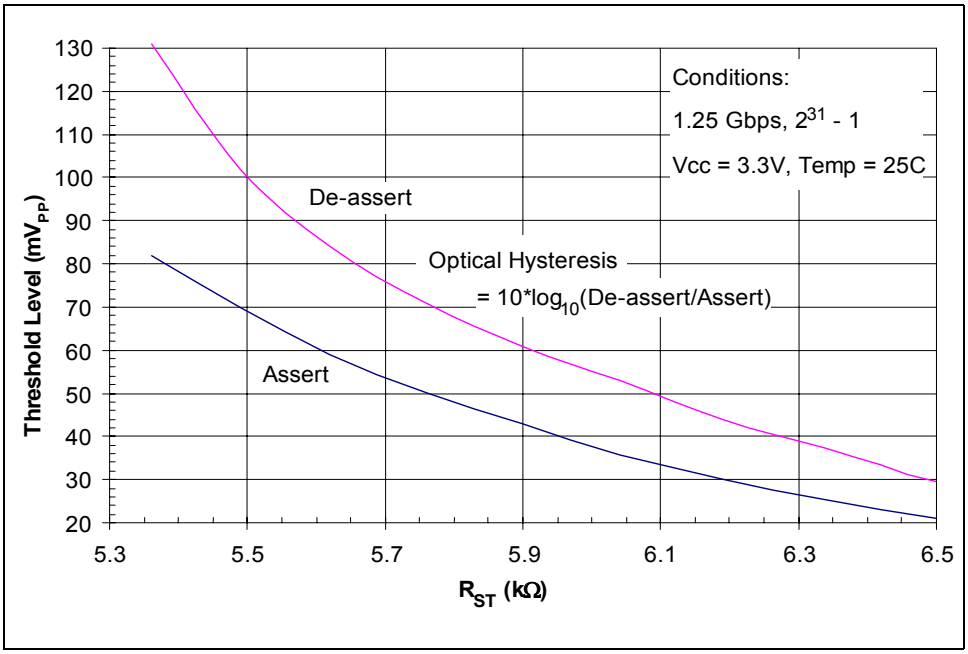


Figure 1-5. Signal Detect Characteristic (High Input Signal)



1.1.5 JAM

JAM is a CMOS compatible input that can be used to inhibit the data outputs when forced to a logic high. If connected directly to the LOS output pin, then when LOS is asserted the data outputs will be forced to logic “one” state ensuring that no data is propagated through the system. Header HD2 (JAM Control) provides the flexibility to either connect LOS to JAM or leave unconnected.

2.0 EVM Bill of Materials

Table 2-1. Bill of Materials

Qty	Vendor	Part Number	Reference Designators	Description
1	KOA	RK73H1JLTD75000	C1 **(R_{ST})**	RES CHIP THICK FILM 7.50K OHM 1/10W 1% 0603
3	KEMET ELECTRONICS	C0603C104K5RACTU	C2-C4	CAP CERAMIC 50V 0.1UF 10% X7R 0603
1	Yageo America	9C06031A0R00JLHFT	C5 (3.3V Only)	RES 0.0 OHM 1/10W 5% 0603 SMD
1			C5 (3.3/5V)	No Connect
5	KEMET ELECTRONICS	C0603C104K5RACTU	C6-C10	CAP CERAMIC 50V 0.1UF 10% X7R 0603
5			C11 - C15	Typically No Connect
2	KEMET ELECTRONICS	C0603C101K5RACTU	C16, C17	CAP CERAMIC 50V 100PF 10% X7R 0603
5	PANASONIC	ECJ-3YF1A106Z	C18	CAP CERAMIC 10V 10UF +80/-20% Y5V 1206
2	SULLINS ELECTRONICS	PZC03SAAN	HD1, HD2	HEADER MALE 3 Pin 100 MIL STRAIGHT SINGLE ROW 1X3
1	SULLINS ELECTRONICS	PZC02SAAN	HD3	HEADER MALE 2 Pin 100 MIL STRAIGHT SINGLE ROW 1X2
2			L1, L2	Typically No Connect
2	Murata	BLM21RK601SN1	L3, L4	INDUCTOR CHIP FERRITE 600 OHM at 100MHZ, 200MA, 0805
1	Kingbright	AA3528SRC	LD1	3.5x2.8 mm SMD chip LED VF = 1.85V at ID = 20mA
4	Johnson Components	142-0701-201	J1, J2, J3, J4	Vertical Through-hole SMA Connector
3			R1, R2, R3	Typically No Connect
2	KOA	RK73H1JLTD1300F	R4, R5 Typically Open (optional Thevenin PECL high termination. 130 Ω for V_{CC} = 3.3V, 82 Ω for V_{CC} = 5V and also use R11 and R12)	RES CHIP THICK FILM 130 OHM 1/10W 1% 0603
		RK73H1JLTD82R5F		RES CHIP THICK FILM 82.5 OHM 1/10W 1% 0603
3	Yageo America	9C06031A0R00JLHFT	R6, R7, R8	RES 0.0 OHM 1/10W 5% 0603 SMD

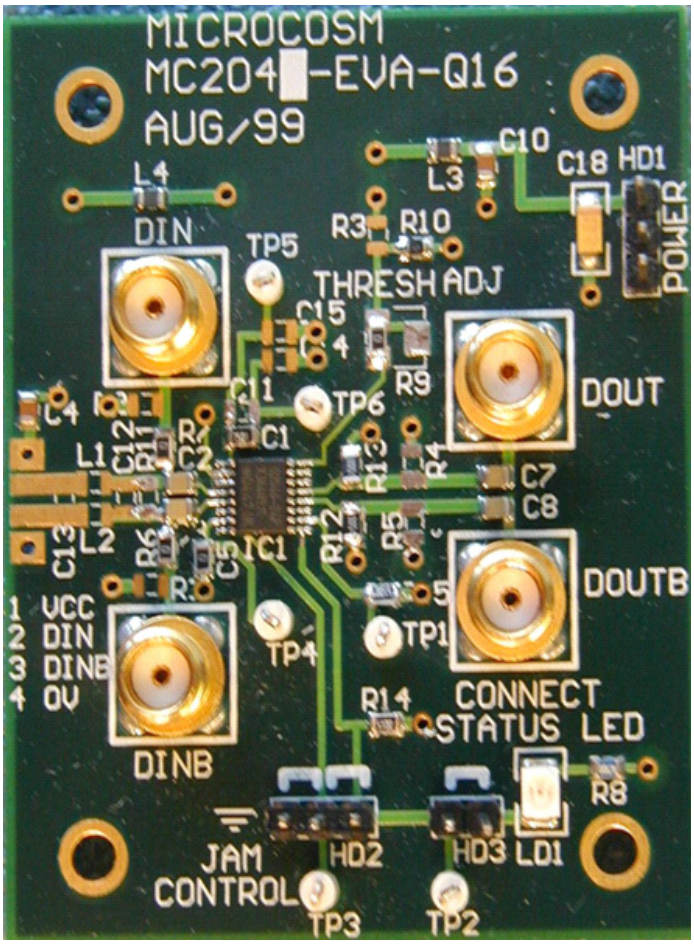
Table 2-1. Bill of Materials

Qty	Vendor	Part Number	Reference Designators	Description
1	BOURNS, INC.	3214W-1-202G	R9	RES ADJUSTABLE 2KOHM 1/2W 10% 4MM SQUARE SMD TOP ADJUST
2	KOA	RK73H1JLTD1000F	R10, R11	RES CHIP THICK FILM 100 OHM 1/ 10W 1% 0603
2	KOA	RK73H1JLTD1500F	R12, R13 Typically, R12 = R13 = 150 Ω for V_{CC} = 3.3V and R12 = R13 = 300 Ω for V_{CC} = 5V For optional Thevenin PECL low termination. 82 Ω for V_{CC} = 3.3V, 130 Ω for V_{CC} = 5V and use R4 and R5	RES CHIP THICK FILM 150 OHM 1/ 10W 1% 0603
		RK73H1JLTD3010F		RES CHIP THICK FILM 300 OHM 1/ 10W 1% 0603
		RK73H1JLTD1300F		RES CHIP THICK FILM 130 OHM 1/ 10W 1% 0603
		RK73H1JLTD82R0F		RES CHIP THICK FILM 82.0 OHM 1/ 10W 1% 0603
1			R14	No Connect
1			R15 (CMOS Status Output versions -14 or -24 only)	
1	KOA	RK73H1JLTD5100F	R15 (PECL Status Output versions -15 or -25 only)	RES CHIP THICK FILM 510 OHM 1/ 10W 1% 0603
11	Keystone	5012	TP1- TP6	White THROUGH_HOLE PC TEST POINT, WITH EYE
1	Mindspeed Technologies	M02046	U1	Limiting Amplifier

3.0 Schematics and Layout

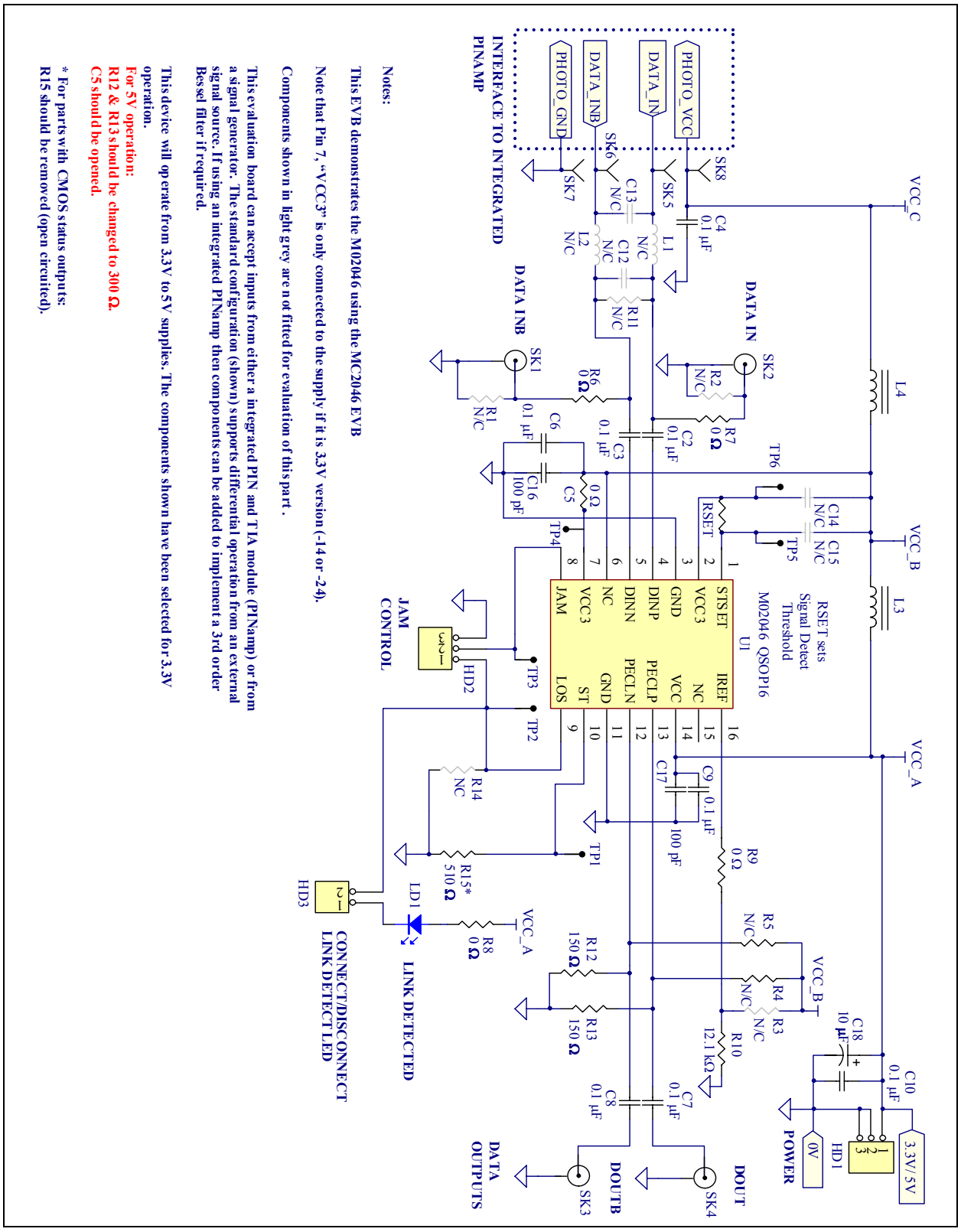
3.1 Board Layout

Figure 3-1. Board Layout



3.2 Schematics

Figure 3-2. Schematic Diagram



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