HIGH SPEED CMOS GATE ARRAYS

■ DESCRIPTION

The S-MOS SLA10000 series is a channel-less gate array manufactured on S-MOS' state-of-the-art 0.8 micron double-metal SiCMOS process. The series consists of 11 arrays ranging from 9,000 to 101,800 usable gates and from 128 to 432 I/O. The SLA10000 series has been tailored for high performance designs with typical gate delays of .3 nanoseconds. Additionally, high-speed silicon efficient RAM functions are offered as customized cells. The series has a selectable output drive capability of 2, 6, 12 or 24 milliamps (two output buffers can be used in parallel to obtain 48 milliamps). The arrays are offered in a wide variety of packages including 64 – 256 pin quad flat packs. The SLA10000 series is supported by S-MOS' own design system with NavNet schematic editor, as well as most major CAD systems including Mentor, Valid, Viewlogic, FutureNet, Synopsys/ Verilog and OrCAD.

■ FEATURES

- .76 micron drawn channel length (N-channel)
- Very high speed: tpd (2-input power NAND)(typ, FO = 2 & 2mm AL) = 0.3 ns/gate
- High Drive
  - 24mA for a single output
  - 48 mA for parallel outputs
- Low gate–to–pads ratio for high pin count applications
- Megacells compatible
- Fully migratable to S–MOS standard cell families

■ PRODUCT CONFIGURATION

Array	Raw Gates	Usable Range		Total # of Pads
		Min	Max	
SLA1020	20216	9097	11523	128
SLA1024	24424	10746	13922	140
SLA1029	29120	12521	16016	152
SLA1034	34138	14338	18776	164
SLA1039	39644	16650	21804	176
SLA1049	49489	20290	26230	196
SLA1060	60653	24868	32146	216
SLA1073	73353	29342	39000	236
SLA1081	81320	32528	41000	248
SLA1152	152256	53290	68515	336
SLA1255	254743	89160	101897	432

NOTE: All arrays have 4 power / GND pads included within total pad count.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	Vss -0.3 to 7.0	V
Input Voltage	V_{IN}	Vss -0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	Vss-0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	-65 to +150	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.50	5.0	5.50	V
Input Voltage	V_{IN}	Vss		V_{DD}	V
Operating Temperature	T_{OPR}	-20		85	°C

■ PERFORMANCE CHARACTERISTICS (Under Recommended Operating Conditions)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low level input voltage					
V_{IL}	CMOS Level				1.0	V
	TTL Level				0.8	V
	High level input voltage					
V_{IH}	CMOS Level		3.5			V
	TTL Level		2.0			V
	Positive going threshold voltage					
V_{T+}	CMOS Schmitt Trigger	V_{DD} = 5.0			4.0	V
	TTL Schmitt Trigger	V_{DD} = 5.0			3.0	V
	Negative going threshold voltage					
V_{T-}	CMOS Schmitt Trigger	V_{DD} = 5.0	0.8			V
	TTL Schmitt Trigger	V_{DD} = 5.0	0.6			V
	Hystereisis voltage					
V_H	CMOS Schmitt Trigger	V_{DD} = 5.0	0.3			V
	TTL Schmitt Trigger	V_{DD} = 5.0	0.1			V
I_{IL}	Low level input current	V_{IN} = V_{SS} No pull-up			1.0	µA
I_{IH}	High level input current	V_{IN} = V_{DD} No pull-up			1.0	µA
	Low level output voltage					
	LOT + OSC	I_{OL} = 50µA			V_{SS} +0.4V	V
V_{OL}	Type 1	I_{OL} = 2mA			V_{SS} +0.4V	V
	Type 2	I_{OL} = 6mA			V_{SS} +0.4V	V
	Type 3	I_{OL} = 12mA			V_{SS} +0.4V	V
	Type 4	I_{OL} = 24mA			V_{SS} +0.4V	V
	High level output voltage					
	LOT + OSC	I_{OH} = 50µA	V_{DD} -0.4V			V
V_{OH}	Type 1	I_{OH} = 1mA	V_{DD} -0.4V			V
	Type 2	I_{OH} = 2mA	V_{DD} -0.4V			V
	Type 3	I_{OH} = 4mA	V_{DD} -0.4V			V
	Type 4	I_{OH} = 8mA	V_{DD} -0.4V			V
	Pull up resistor	V_{DD} = 5.0				KΩ
R_{PU}	Type 1		25		100	
	Type 2		50		200	
	Type 3		100		400	
	Pull down resistor	V_{DD} = 5.0				KΩ
R_{PD}	Type 1		25		100	
	Type 2		50		200	
	Type 3		100		400	
I_{OZ}	Tri-state leakage current				1.0	µA
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			6		pF
C_{BID}	Bi-directional pad capacitance			10		pF

■ MACRO LIBRARY

Function	Cell Name	Gates
SIMPLE GATES		
2–INPUT NAND GATE	NA2	1
3–INPUT NAND GATE	NA3	2
4–INPUT NAND GATE	NA4	2
2–INPUT NOR GATE	NO2	1
3–INPUT NOR GATE	NO3	2
4–INPUT NOR GATE	NO4	2
3–INPUT AND GATE	A3	2
6-INPUT AND GATE	A6	4
8-INPUT AND GATE	A8	5
3–INPUT OR GATE	O3	2
6–INPUT OR GATE	O6	4
8–INPUT OR GATE	O8	5
EXCLUSIVE OR GATE	EXO	3
EXCLUSIVE NOR GATE	EXN	3
COMPLEX GATES		
2–AND 2–WIDE 3–INPUT NOR GATE	AN23	2
3–AND 2–WIDE 4–INPUT NOR GATE	AN14	2
2–AND 2–WIDE 4–INPUT NOR GATE	AN24	2
2–AND 3–WIDE 4–INPUT NOR GATE	AN34	2
2–AND 3–WIDE 6–INPUT NOR GATE	AN36	5
2–AND 2–WIDE 3–INPUT OR GATE	AO23	2
3–AND 2–WIDE 6–INPUT OR GATE	AO26	4
4–AND 2–WIDE 8–INPUT OR GATE	AO28	5
2–AND 2–WIDE 3–INPUT NAND GATE	ON23	2
3–AND 2–WIDE 4–INPUT NAND GATE	ON14	2
2–AND 2–WIDE 4–INPUT NAND GATE	ON24	2
2–AND 3–WIDE 4–INPUT NAND GATE	ON34	2
2–AND 2–OR 2–WIDE 4–INPUT NAND GATE	ON44	2
2–OR 3–WIDE 6–INPUT NAND GATE	ON36	5
2–OR 2–WIDE 3–INPUT AND GATE	OA23	2
INVERTERS/BUFFERS		
NORMAL INVERTER	IN1	1
POWER INVERTER	IN2	1
POWER INVERTER	IN4	2
NORMAL BUFFER	BUF1	1
FLIP-FLOPS		
LATCH	LF	4
LATCH WITH RESET	LFR	5
LATCH WITH SET	LFS	5
D–FF	DF	6
D–FF WITH RESET	DFR	7
D–FF WITH SET	DFS	7
D–FF WITH SET AND RESET	DFSR	8
JK–FF WITH RESET	JKR	10
JK–FF WITH SET AND RESET	JKSR	11
ADDERS		
1–BIT FULL ADDER	T183	9
COMPARATORS		
4–BIT MAGNITUDE COMPARATOR WITH ENABLE	T085	39
8–BIT MAGNITUDE COMPARATOR	T688	26
COUNTERS		
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161	57
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET AND LOAD	T161E	51
SYNCHRONOUS 2–BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161H	29

■ **MACRO LIBRARY (cont.)**

Function	Cell Name	Gates
COUNTERS (cont.)		
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET AND ENABLE	A161L	46
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET	A161LE	40
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH LOAD AND ENABLE	A161R	52
SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH LOAD	T161RE	46
FULLY SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A163	54
FULLY SYNCHRONOUS 4–BIT BINARY UP COUNTER WITH RESET AND LOAD	A163E	48
RESETABLE R–BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177	39
PRESETABLE 2–BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177H	21
PRESETABLE 4–BIT BINARY UP COUNTER/LATCH WITH LOAD	T177R	38
PRESETABLE 4–BIT BINARY UP COUNTER/LATCH WITH SET AND LOAD	T177V	39
PRESETABLE 2–BIT BINARY UP COUNTER/LATCH WITH SET AND LOAD	T177HV	20
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191	70
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH RESET	A191CE	47
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH LOAD	A191E	63
SYNCHRONOUS 2–BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191H	35
SYNCHRONOUS 4–BIT UP/DOWN COUNTER WITH RESET	A191LE	51
SYNCHRONOUS 4–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193	69
SYNCHRONOUS4–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193L	53
SYNCHRONOUS 2–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193L	36
SYNCHRONOUS 2–BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193HL	27
DECADE COUNTER WITH RESET	A390	34
4–BIT BINARY UP COUNTER WITH RESET	T93V	25
4–BIT BINARY DOWN COUNTER WITH RESET	T393V	25
DECODER/DEMULTIPLEXERS		
BCD–TO–DECIMAL DECODER	T042	29
3–LINE TO 8–LINE DECODE/MULTIPLEXER WITH ENABLE G	A138G2	18
2–LINE TO 4–LINE DECODER/MULTIPLEXER WITH ENABLE G	A139	9
2–LINE TO 4–LINE DECODER/MULTIPLEXER	A139G	6
DFFS/LATCHES		
4–BIT LATCH WITH RESET	T116	17
QUADRUPLE DFF WITH RESET	T175	27
QUADRUPLE DFF WITH Q, XQ WITHOUT RESET	T175R	22
QUADRUPLE DFF WITH Q ONLY	T175RX	22
OCTAL DFF WITH RESET	T175W	54
OCTAL OFF	T175WR	44
OCTAL D–TYPE TRANSPARENT LATCH WITH ENABLE	T373T	26
SELECTORS/MULTIPLEXERS		
4–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T153	12
4–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER	T153G	10
QUADRUPLE 2–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157WG	13
QUADRUPLE 2–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER	T157G	11
OCTAL 2–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157W	25
OCTAL 2–LINE TO 1–LINE DATA SELECTOR/MULTIPLEXER	T157WG	21
SHIFT REGISTERS		
8–BIT PARALLEL–OUT SERIAL SHIFT REGISTER WITH RESET	T164	55
8–BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166	65
4–BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166H	34

■ INTERNAL TRISTATES

S-MOS supports the use of internal tristate busses with the following macro library:

Name	Function	Gates
TSV	Tristate Inverting Buffer	4
TSB	Tristate Buffer	4
T240	Octal Inverting Tristate Buffer	26
T240H	Quad Inverting Tristate Buffer	13
T244	Octal Tristate Buffer	22

Name	Function	Gates
T244H	Quad Tristate Buffer	11
T373	Octal Latch With Tristates	46
T373H	Quad Latch With Tristates	23
T374	Octal DFF With Tristates	72
T374H	Quad DFF With Tristates	36

NOTE: In order to ensure design quality, S-MOS Systems requires the use of certain design practices when using internal tristate cells. Please consult S-MOS Systems for more information.

■ PACKAGE MATRIX

Package Type	No. of Pins	Device code	1020	1024	1029	1034	1039	1049	1060	1073	1081	1152	1255
		No. of Pads	128	140	152	164	176	196	216	236	248	336	432
		Gross Gates	20216	24424	29120	34138	39644	49489	60653	73353	81320	152256	254743
Plastic DIP	28	S28	A										
	40	C40	A										
Plastic QFP	64	QFP–5	Q	Q									
	64	QFP–13	A	A	A								
	80	QFP–5	A*	A*	A*	A*	A*	A*	A*	LQ	LQ		
	80	QFP–14	A	A	A	A	A	A	A				
	100	QFP–5	A*	A*	A*	A*	A*	A*	A*	LQ	LQ		
	100	QFP–15	A	A	A	A	A	A	A				
	120	QFP–8	A*	A*	A*	A*	A*	A*	A*	A*	A*		LQ
	128	QFP–5	A*	A*	A*	L	A*	A*	A*	LQ			
	128	QFP–8	A	A	A*	A*	A*	A*	A*	A*	A*		LQ
	144	QFP–8	L	L	A*	A*	A*	A*	A*	A*	A*		LQ
	144	QFP–17		L	A	A	A	A	A	Q	A*		LQ
	160	QFP–8		L	L	A*	A	A*	A*	A*			
	184	QFP–16						Q	A	A	A		LQ
	196	QFP–9							A*	A			LQ
	208	QFP–8							A	A*	A*	Q	LQ
	232	QFP–10											LQ
	256	QFP–9											Q
PLCC	44	J44	Q										
	68	J68	A										
	84	J84	A*	A*	A*	A*	A*	A*	A*	A*	A*		LQ
Ceramic PGA	132	P132				A							

A: Available
*: Pin–Pad table exist
L: Need Lead frame development (2.5 months for new lead frame development)
Q: Need Qualification (reliability test) (2.5 months for reliability test)
LQ: Need Lead frame and Qualification (reliability test)(2.5 months for new lead frame development and/or 2.5 months for reliability test)

■ PROCESS TECHNOLOGY

The SLA10000 Series is fabricated on our highly automated 6" fabrication line located in Fujimi, Japan. The process is similar to that used for high-volume 1 Meg SRAM which has been in production since 1988.

N-Channel is .76 micron drawn (0.6 micron effective) and P-Channel length is 1.2 micron drawn (.8 micron effective).

■ PROPAGATION DELAY TIMES

The propagation delay values printed in our cell libraries and used in simulation are derived from actual measurements of silicon, not spice simulations. The measured coefficient parameters are:

● Delay Multiplier

	5%	10%
Min	0.65	0.60
Max	1.60	1.75

5% Factor
Voltage: 4.75 to 5.25 volts
Temperature = 0 to 70°C

10% Factor
Voltage: 4.50 to 5.50 Volts
Temperature = –20 to 85°C

Name	Function	From	To	Best Case		Worst Case		Loads
				tplh (ns)	tphl (ns)	tplh (ns)	tphl (ns)	
NA2	2–INPUT NAND	IN	OUT	.07	.05	.15	.11	0
				.12	.09	.28	.20	1
				.18	.13	.40	.30	2
NO2	2–INPUT NOR	IN	OUT	.09	.03	.23	.06	0
				.18	.05	.45	.12	1
				.27	.08	.66	.17	2
IN1	1 x INVERTER	IN	OUT	.05	.03	.12	.06	0
				.10	.05	.25	.12	1
				.16	.08	.38	.17	2
IN4	4 x INVERTER	IN	OUT	.03	.02	.08	.04	0
				.04	.03	.11	.05	1
				.06	.04	.15	.07	2
DF	D FLIP–FLOP	CLK	Q	.39	.47	.95	1.16	0
				.44	.49	1.08	1.22	1
				.50	.52	1.20	1.27	2
IBT	TTL LEVEL INPUT BUFFER	IN	OUT	.41	.39	1.00	.95	0
				.43	.42	1.05	1.01	1
				.45	.44	1.09	1.08	2
$\overline{UO1}$	2mA OUTPUT DRIVER	IN	PAD	1.20	1.89	2.95	4.64	10pF
				4.56	6.46	11.22	15.88	50pF
				8.76	12.16	21.55	29.93	100pF
$\overline{UO2}$	6mA OUTPUT DRIVER	IN	PAD	.75	1.17	1.84	2.86	10pF
				2.77	3.55	6.79	8.46	50pF
				5.28	6.29	12.98	15.46	100pF

BEST CASE	WORST CASE
Temperature = 0°C Ambient	Temperature = 70°C Ambient
Supply Voltage = 5.25V	Supply Voltage = 4.75V
Process = Best case	Process = Worst Case

- **Workstation Support**

Schematic capture, electrical rule checking, design rule checking, simulation and timing verification are supported on Daisy, Mentor, Valid, NavNet and Intergraph workstations. In addition, our proprietary LADS software, used with NavNet, ViewLogic, OrCad or FutureNet, is available for IBM PCs and compatibles. LADS is also available on Sun and Apollo platforms.
LADS includes ERC, DRC, logic simulation and timing verification up to 6,000 gates using PCs with 640K of memory or up to 20,000 gates in PCs equipped with 4 megabytes of extended memory.

- **Standard Cell Migration**

The SLA10000 Series can be easily migrated to the SSC5000 Series 0.8μm standard cells. This is made possible by the identical and compatible design tools shared by the two design methodologies. As such, the gate array macro library is a subset of the standard cell macro library.

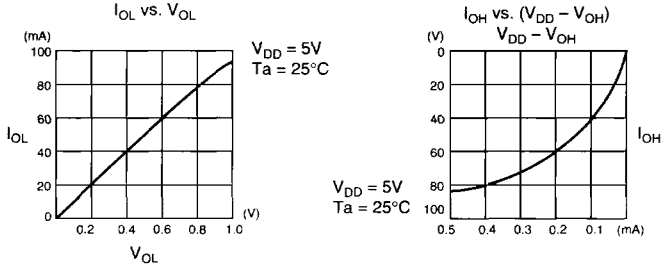
- **Megacells**

Due to the design of the SLA10000 Series, fully routed and characterized megacells be implemented effectively alongside of random logic. Available:

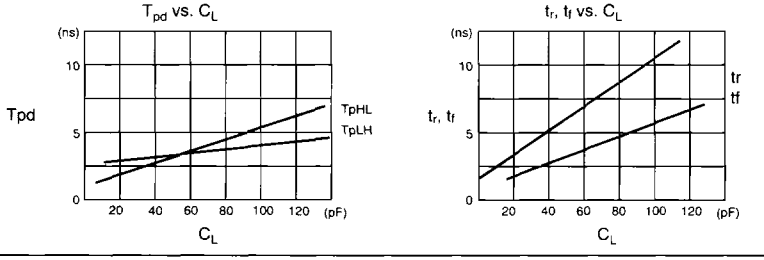
B8259	B82288
B8237	B146818
B82284	B8250
B8255	B8251
B16C550	B8254
	B–80

■ PERFORMANCE CURVES

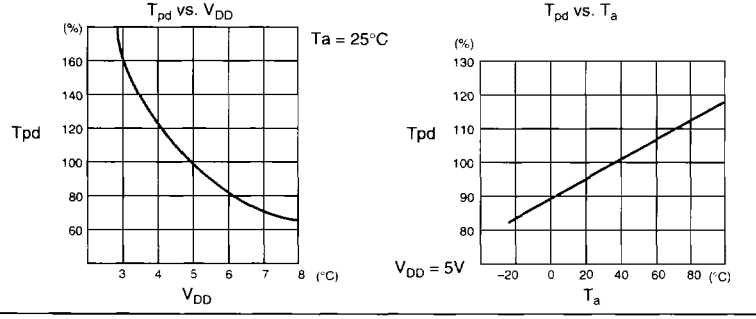
Current (Type 4 Output Buffer)



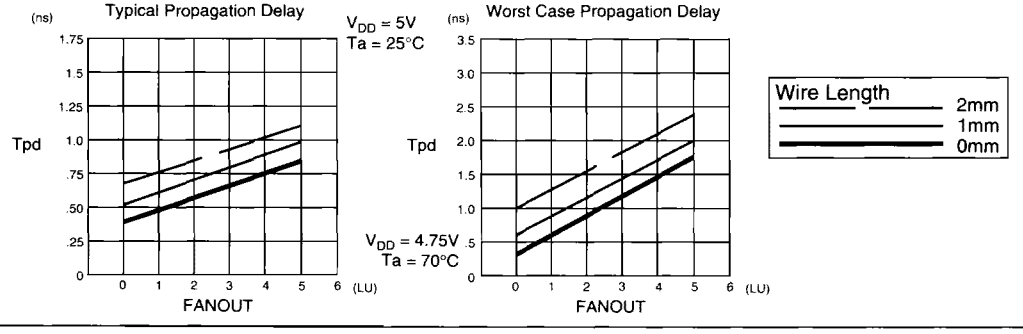
Type 2 Output Buffer Delay Characteristics



Propagation Delay Characteristics



Propagation Delay Including Interconnect



■ S–MOS Systems ASIC Design Flow