UBA2013/L3

HB driver IC with PFC for fluorescent rings

Rev. 00.01 — 23 February 2007 Preliminary data sheet

1. General description

The UBA2013/L3 is a high voltage IC intended to drive and control fluorescent lamps. The IC can handle both cold and warm ignition of the lamp. It contains a T_{ON}-controlled PFC function, a half bridge controller circuit with level shifter and an internal bootstrap diode to drive an external half bridge. UBA2013/L3 also offers a functionality to properly handle fault conditions such as capacitive mode switching, end-of-lamp-life and overcurrent. UBA2013/L3 is designed for wide-input mains voltage (120 V - 277 V) applications.

2. Features

2.1 Half bridge

- Suitable for cold and warm ignition
- Adjustable preheat time
- Adjustable ignition voltage
- Integrated bootstrap function
- Protection for lamp failure and end-of-life
- Adjustable preheat current
- Single ignition attempt
- Automatic restart after relamping
- Protection for capacitive mode

2.2 PFC

- Three pin PFC controller using T_{ON} control
- Critical mode operation
- Overvoltage/overcurrent protection

3. Applications

The UBA2013/L3 can provide the drive and control function for a wide range of half bridge based ballast applications at different mains voltages.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA2013T	SO16	plastic small outline package; 16 leads; body width 3.9mm	SOT109-1

5. Block diagram

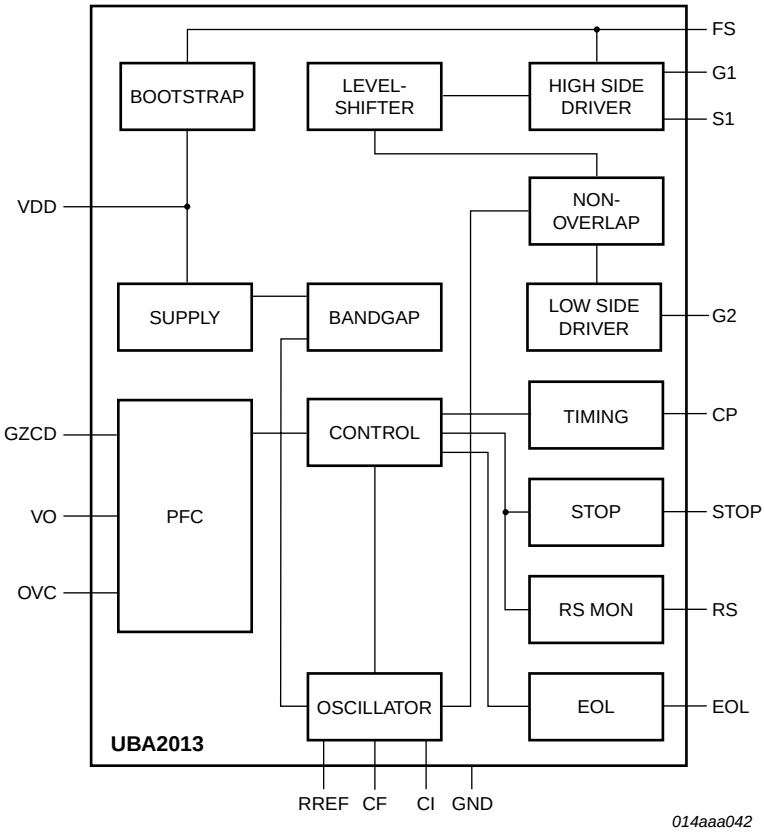


Fig 1. Block diagram of UBA2013/L3

6. Pinning information

6.1 Pinning

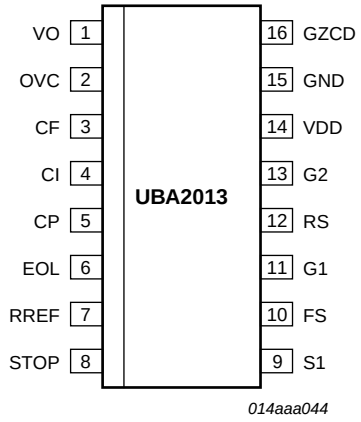


Fig 2. Pin configuration for UBA2013/L3

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VO	1	PFC output voltage sensing
OVC	2	PFC overvoltage/current
CF	3	Oscillator capacitor
CI	4	Integrating capacitor
CP	5	Timing capacitor
EOL	6	End-of-life
RREF	7	Reference resistor
STOP	8	Stop
S1	9	Source high side transistor (T1)
FS	10	High side floating supply
G1	11	Gate high side transistor (T1)
RS	12	Current sensor
G2	13	Gate low side transistor (T2)
VDD	14	Low voltage supply
GND	15	Ground
GZCD	16	PFC gate and ZCD

7. Functional description

7.1 Start-up state

Initial start up can be achieved by means of charging the VDD low voltage supply capacitor (C2 in the application diagram Figure 6) via an external start-up resistor. Start-up state is one of the non-oscillating sub-states. MOSFET T2 conducts and T1 is non-conducting, ensuring bootstrap capacitor C3 to be charged. In this state the circuit will be reset. The GZCD pin is pulled down and $I_{VO(ref)}$ is not active. If $V_{STOP} < V_{STOP(reset)}$ at the transition of V_{DD} exceeding $V_{DD(start)}$, the IC will enter the oscillating state. If not it will enter the stop state.

7.2 Half bridge oscillator

Oscillation of the half bridge is controlled by a built-in current-controlled oscillator which generates a sawtooth waveform at the CF pin. The sawtooth frequency is twice the half bridge frequency, and is determined by the capacitor at the CF pin and the current-out of pin CF, as controlled by the voltage at the CI pin. Frequency modulation is achieved by charging and discharging the CI capacitor. The IC brings MOSFETs T1 and T2 alternately into conduction with a duty factor of just below 50% each (except for situations where V_{RS} exceeds $V_{RS(clamp)}$). Figure 3 represents the timing of the IC. The circuit block 'non-overlap' generates a non-overlap time t_{no} that ensures periods of exclusive conduction of T1 or T2. Time t_{no} depends on the reference current I_{RREF}.

7.3 Oscillating state

Oscillating state can be entered:

- when in the startup state $V_{STOP} < V_{STOP(reset)}$ at the moment V_{DD} reaches $V_{DD(start)}$,
- when in the VddLow state, when $V_{STOP} < V_{STOP(ref)}$ at the moment V_{DD} reaches $V_{DD(start)}$.

The oscillating state has three sub-states: the preheat state, the ignition state and the burn state. The circuit always starts oscillating in the preheat state.

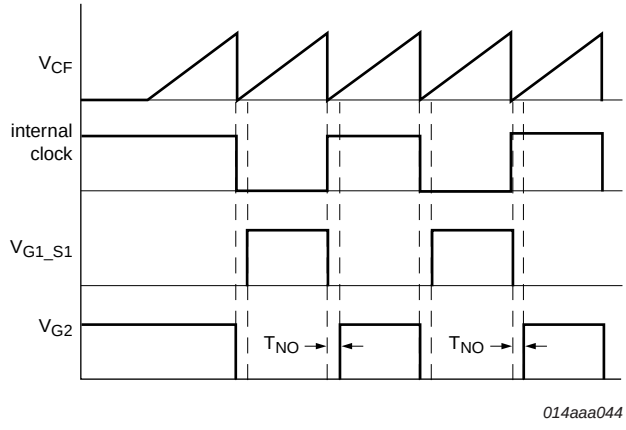


Fig 3. Oscillator timing

7.4 Preheat state

The circuit starts oscillating at the half-bridge frequency f_{start} (approximately 2.5 x f_B). The frequency gradually decreases until a user-defined value of the preheat current is reached. The slope of the decrease in frequency is determined by the capacitor at the CI pin. During preheat, the circuit monitors the inductor current by measuring the voltage across external resistor RS at the end of the conduction of T2 with decision level $V_{RS(ph)}$. The frequency is decreased for as long as $V_{RS} < V_{RS(ph)}$. The frequency is increased for $V_{RS} > V_{RS(ph)}$. During preheat the STOP pin is discharged to ground via a switch with an on resistance of $R_{STOP(disch)}$. The cycle-by-cycle excess charge control mechanism described in the ignition state is not active during the preheat state. The preheat time is determined by capacitor CP. For cold ignition the preheat time can be reduced by choosing a smaller CP capacitor. The circuit can be locked in the preheat state by connecting pin CP to ground.

7.5 Ignition state

After the preheat time the ignition state is entered and the frequency will sweep down due to charging of the capacitor at the CI pin with the internally fixed current $I_{CI(charge)}$. During this decrease in frequency, the circuit approaches the resonance frequency of the load. This will cause a high voltage across the load, which normally ignites the lamp.

In order to limit voltages and currents in the resonant circuit in case of non- or delayed ignition, a cycle-by-cycle excess charge control mechanism is used to prevent deep saturation and to limit the lamp voltage. When the voltage at pin RS exceeds $V_{RS(clamp)}$ the impedance of the pin changes from essentially infinite to essentially zero. If a current is flowing into pin RS during the on-state of T2, a fraction k_{Isat} of that current will be fed into the capacitor C_{CF} at pin CF in addition to the oscillator current already flowing into C_{CF}. The amount of current fed into C_{CF} depends on the voltage across RS and the value of resistor R, see Figure 4. The increased current rapidly (but not instantly) ends the oscillator half-cycle, after which T2 is switched off. The on-time of T1 is not affected and thus the half bridge will run asymmetrically, see Figure 4.

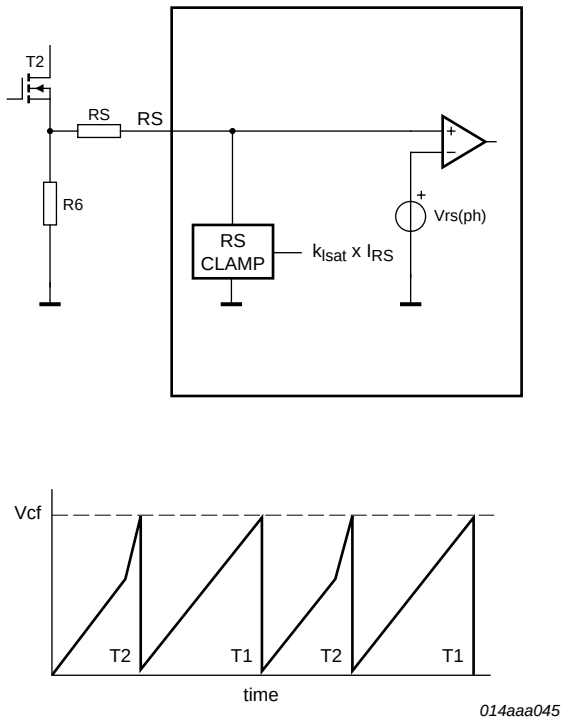


Fig 4. Excess charge control

7.6 Burn state

At the end of the ignition time, the burn state is entered. In this state the voltage at the CI pin will continue to increase until a clamp level is reached corresponding to the minimum frequency f_B. The circuit will continue to oscillate at the minimum frequency, unless capacitive mode is detected. In the burn state the CP pin is pulled to ground with a discharge impedance $R_{CP(disch)}$. The EOL protection is enabled. The excess charge control mechanism will remain active.

7.7 Capacitive mode protection

Capacitive mode protection is active in all oscillating states. The signal across resistor RS (R6 in the application diagram of Figure 6) also gives information about the switching behavior of the half bridge. If the voltage across resistor RS is not below $V_{RS(cap)}$ at the moment of turn-on of T2, the capacitive mode detection circuit assumes the circuit to be in capacitive mode. Upon capacitive mode detection CI is gradually discharged and instantly the frequency gradually increases as long as capacitive mode is detected. The frequency decreases gradually down to the minimum frequency if no capacitive mode is detected. Detecting capacitive mode at the maximum frequency will activate the internal current $I_{STOP(ch)}$ that charges the STOP pin.

7.8 Stop function

For all oscillating states the IC will enter the stop state for $V_{STOP} > V_{STOP(ref)}$. Note that there is no internal stop timing. An external stop timing can be obtained via the RC time of the network R4, R5 and C11, see the application diagram in Figure 6. During preheat the

STOP pin is discharged to ground via a switch with on-resistance $R_{STOP(disch)}$. In case of a VO-low condition (see Section 7.15), the STOP pin is discharged with a current $I_{STOP(dis)}$. Apart from the preheat state or a VO-low condition, the IC will not discharge the STOP pin at any VDD.

7.9 End-of-life protection

The end-of-life circuit is only active in the burn state and consists of a voltage window comparator circuit. It compares the voltage at the EOL pin with two internal reference voltages. When the voltage at the EOL pin is above $V_{EOL(high)}$ or below $V_{EOL(low)}$ the 'end-of-life' protection circuit activates the internal current source $I_{STOP(ch)}$ that charges the STOP pin. The 'end-of-life' protection is not active in case of a VO-low condition (see Section 7.15).

7.10 Non-oscillating state

Transitions to the non-oscillating state are always made during a G2 high condition in the half bridge (lower MOSFET T2 conducting). In the non-oscillating state T1 is off, T2 is on, the PFC control function is stopped by pulling the GZCD pin down to ground continuously, and reference current $I_{VO(ref)}$ is switched off. Additionally, the CP and CI pins are discharged to ground. The non-oscillating state has three sub-states: the start-up state, the stop state and the VddLow state.

7.11 Start-up state

Described at the beginning of this functional description.

7.12 Stop state

The circuit will enter the stop state:

- when in any of the oscillating states $V_{STOP} > V_{STOP(ref)}$,
- when in the VddLow state $V_{STOP} > V_{STOP(ref)}$ at the moment V_{DD} exceeds $V_{DD(start)}$,
- when in the startup state $V_{STOP} > V_{STOP(reset)}$ at the moment V_{DD} exceeds $V_{DD(start)}$.

In the stop state, a clamp circuit is active, limiting the voltage at the VDD pin to $V_{DD(clamp)}$. The IC goes from the stop state into the startup state if V_{DD} drops below $V_{DD(reset)}$.

7.13 VddLow state

The circuit will enter VddLow state in any of the oscillating states when V_{DD} drops below $V_{DD(low)}$. The circuit then goes from VddLow state to:

- the startup state if V_{DD} drops below $V_{DD(reset)}$,
- the stop state if $V_{STOP} > V_{STOP(ref)}$ at the moment V_{DD} exceeds $V_{DD(start)}$, or
- the preheat state if $V_{STOP} < V_{STOP(ref)}$ at the moment V_{DD} exceeds $V_{DD(start)}$.

7.14 PFC function

The internal PFC control block provides a T_{ON} controlled, critical mode power factor correction controller. The T_{ON} is set by the voltage at the VO pin. The duration of the T_{ON} pulse decreases linearly with increasing V_{VO}. The V_{VO} voltage is the result of an error current through the compensation impedance connected at the VO pin. This error current is the difference between a current proportional to the output voltage of the PFC pulling the VO pin high and an internal reference current $I_{VO(ref)}$ pulling the VO pin low.

The external MOSFET is primarily driven via the secondary winding on the inductor L_{P1}. The T_{ON} timing starts the moment V_{GZCD} exceeds $V_{GZCD(start)}$ (below the threshold of the external MOSFET). The external MOSFET is turned on and current builds up in the inductor L_{P1}. At the end of T_{ON} the output driver pulls the GZCD pin down during a defined time T_{OFF}. This turns off the external MOSFET. The inductor current I_{LP1} now flows through the boost diode DP2. The polarity of the voltage across the secondary winding changes to negative, keeping the external MOSFET in the off state. As long as V_{GZCD} is below $V_{GZCD(start)}$ the T_{ON} timing is reset. The current in the inductor decreases linearly to below zero. Just after the zero crossing the polarity of the voltage across the secondary winding becomes positive and makes V_{GZCD} exceed $V_{GZCD(start)}$, starting the T_{ON} timing, turning on the external MOSFET and completing the cycle.

T_{ON} varies linearly from $T_{ON(max)}$ to $T_{ON(min)}$ in the range of V_{VO} from $V_{VO(low)}$ to $V_{VO(low)}+\Delta V_{VO}$. Above a voltage $V_{VO(off)}$ ($>V_{VO(low)}+\Delta V_{VO}$) at the VO pin, T_{ON} is zero and the GZCD pin is continuously pulled down.

The OVC pin is intended for over-voltage and/or over-current protection. The voltage at the OVC pin is compared to a reference voltage $V_{OVC(ref)}$. For $V_{OVC} > V_{OVC(ref)}$ the GZCD pin is pulled down within a time T_{OVC}. As long as $V_{OVC} > V_{OVC(ref)}$ the GZCD pin will be continuously pulled down by the output driver. Additionally, the OVC pin provides protection against an accidental open circuit of the external OVC divider of the PFC output voltage. As long as $V_{OVC} < V_{OVC(low)}$ the GZCD pin is continuously pulled down by the output driver.

In order to prevent persistent ambiguous drive signals for the external MOSFET, for $V_{GZCD} > V_{GZCD(start)}$ the GZCD pin is charged after a delay of T_{GZCD} with a current of $I_{GZCD(on)}$ up to a voltage of $V_{GZCD(active)}$ (above the threshold of the external MOSFET). Note that the voltage at the GZCD pin is not clamped at $V_{GZCD(active)}$: the secondary winding on the inductor L_{P1} can take the GZCD pin up to V_{DD}.

The PFC function is self-starting by means of a current source $I_{GZCD(start)}$ ($<< I_{GZCD(on)}$) which, under oscillation conditions, continuously charges the GZCD pin. In any of the non-oscillating states the current sources $I_{GZCD(start)}$ and $I_{VO(ref)}$ are off and the GZCD pin is continuously pulled down. In oscillating conditions the positive voltage at the VO pin is clamped at a level $V_{VO(clamp)}$: in non-oscillating conditions, the positive voltage at the VO pin is clamped at a level $< V_{VO(off)}$.

7.15 VO-low condition

In order to prevent unintended stopping in case of the mains voltage being too low for the PFC stage to maintain its intended output voltage, this condition is detected in the oscillating state by the current sunk into the VO pin dropping below $k_{VO}*I_{VO(ref)}$, where the constant k_{VO} represents a fraction (typ. 95%) of $I_{VO(ref)}$. In case of a VO-low condition:

- the end-of-life protection is deactivated,

- the stop level is effectively raised by discharging the STOP pin with a current $I_{STOP(dis)}$.

The VO-low condition is overruled when $V_{OVC} < V_{OVC(low)}$.

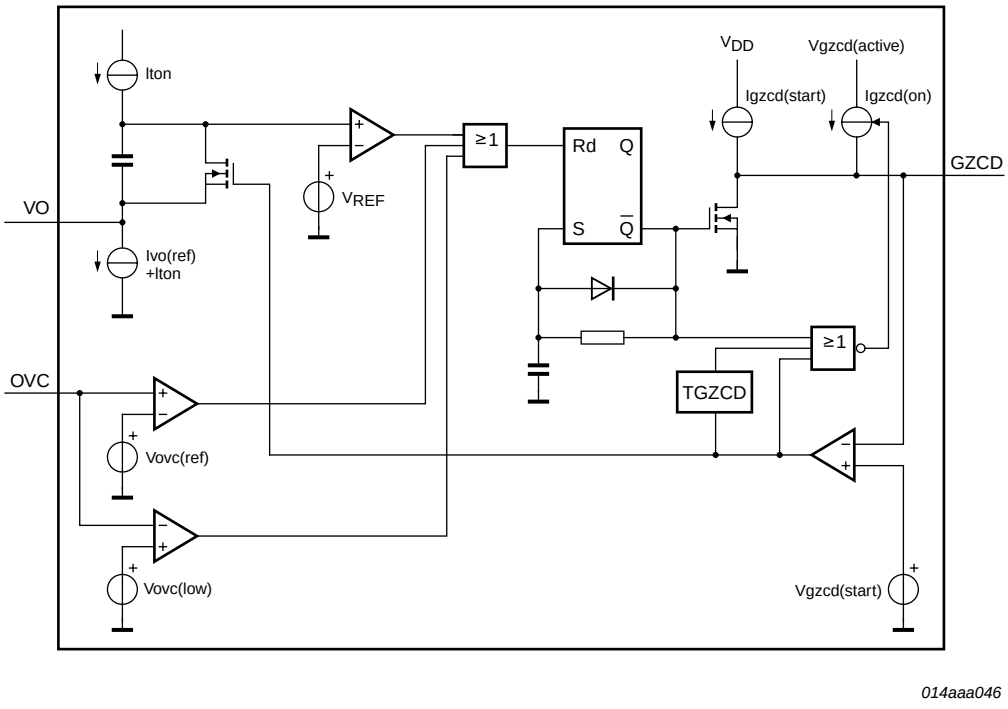


Fig 5. PFC block

7.16 State and transition diagrams

See Section 16.1.

7.17 Charge coupling

Via parasitic capacitive coupling to high-voltage AC signals present in the application, a repetitive AC charge injection might occur at the IC-pins. In the typical application of Figure 6 , the pins R_{REF} and C_F are most sensitive to this charge injection. For a charge coupling of Q_{coupl}, safe functional operation of the IC is guaranteed, irrespective of the current level. Charge coupling at current levels below 50 μA will not interfere with the accuracy of the $V_{RS(cap)}$ and $V_{RS(ph)}$ levels. Charge coupling at current levels below 20 μA will not interfere with the accuracy of any parameter.

8. Limiting values

Table 3. Limiting values

Symbol	Parameter	Conditions		Min	Max	Unit
V_{FS}	High-side floating supply voltage	Operating t<0.5s		0	570 630	V
V_{RS}	Voltage at pin RS		[3]	0	V_{BE}	V
I_{RS}	Current in pin RS	t<1.0µs	[4]	-10	10	mA
V_{G1}	Voltage at pin G1		[3]	V_{S1}-V_{BE}	V_{FS}	V
V_{G2}	Voltage at pin G2		[3]	-V_{BE}	V_{VDD}	V
V_{VDD}	Low-voltage supply	t<0.5s over lifetime		0	15	V
V_{VDD}	Low-voltage supply	In stop state		0	14	V
I_{VDD}	Clamp current in pin VDD				5	mA
V_{GZCD}	Voltage at pin GZCD		[3]	-V_{BE}	V_{VDD}	V
V_{OVC}	Voltage at pin OVC			0	5	V
I_{VO}	Current in pin VO	V_{VDD} = 0V to V_{VDDmax}		0	200	µA
I_{CF}	Current in pin CF	V_{VDD} = 0V to V_{VDDmax}		0	200	µA
I_{EOL}	Current in pin EOL	V_{VDD} = 0V to V_{VDDmax}		-1	1	mA
SR	Slew rate at pins S1, G1 and FS	With respect to ground		-4	4	V/ns
T_j	Junction temperature			-25	150	°C
T_{amb}	Ambient temperature			-25	100	°C
T_{stg}	Storage temperature			-55	150	°C
$V_{esd(HBM)}$	HBM electrostatic handling voltage		[1]			
	pin EOL and G1				<500	V
	pins FS, S1, VDD and G2				1000	V
	pins VO, OVC, CF, CI, CP, RREF, STOP, RS, GZCD				2000	V
$V_{esd(MM)}$	MM electrostatic handling voltage		[2]			
	pin EOL				50	V
	pins FS, G1, S1, VDD and G2				100	V
	pins VO, OVC, CF, CI, CP, RREF, STOP, RS, GZCD				200	V
Q_{coupl}	Charge coupling at pins RREF and CF	Operating		-8	8	pC
R_{RREF}	Reference resistor			22	47	kΩ

[1] In accordance with the Human Body Model (HBM): i.e. equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] In accordance with the Machine Model (MM): i.e. equivalent to discharging a 200 pF capacitor through a 10 Ω series resistor and a 0.75 µH inductor.

[3] At T_{amb} = 25 °C the typical V_{BE} is 0.7 V.

[4] At negative RS currents (typ. < -5 mA) capacitive-mode protection can be triggered.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient SO16	in free air	100	K/W
$R_{th(j-pin)}$	thermal resistance from junction to pin SO16	in free air	50	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{VDD} = 13.0 V; C_{CF} = 100 pF; R_{RREF} = 33 kΩ; C_{CP} = 100 nF; C_{CI} = 100 nF; all voltages referenced to ground unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-voltage supply							
I_{L1}	Leakage current: high-voltage pins	FS, G1, S1 = 630 V, V_{VDD}= 0 V				15	µA
Start-up state							
$V_{DD(start)}$	Start of oscillation			12.1	12.6	13.1	V
$V_{DD(low)}$	Stop of oscillation			9.7	10.2	10.7	V
$V_{DD(hys)}$	Start-stop hysteresis			2.2	2.4	2.6	V
$I_{VDD(nonosc)}$	Non-oscillating current	VVDD = 12 V	[2]	100	150	200	µA
$V_{DD(clamp)}$	Clamp voltage VDD	At 5 mA non-oscillating		10.0	12.0	14.0	V
$V_{DD(reset)}$	Reset voltage		[10]	4.5	5.5	6.5	V
Preheat voltage							
f_{start}	Starting frequency	V_{CI} = 0	[1]	101	112.5	124	kHz
T_{PH}	Preheat time	C_{CP} = 100 nF		574	674	796	ms
$I_{CP(charge)}$	Charge current at CP pin	V_{CP} = 1.0 V			6.0		µA
$I_{CP(discharge)}$	Discharge current at CP pin	V_{CP} = 3.5 V			6.0		µA
$\Delta V_{CP(pk)}$	Peak voltage difference at CP pin	When timing			2.45		V
$V_{CP(min)}$	CP comparator level low			1.10	1.25		V
$V_{RS(ph)}$	Control voltage at RS pin		[5]	365	400	435	mV
Ignition state							
T_{IG}	Ignition time	C_{CP} = 100 nF		512	611	730	ms
$V_{RS(clamp)}$	Saturation current detection level	At $I_{RS(ig)}$ = 0.5 mA			0.75		V
k_{Isat}	Saturation control current gain		[6]	0.45	0.50	0.55	A/A
Burn state							
f_B	Bottom frequency		[1]	43.6	45.0	46.4	kHz
T_{NO}	Non-overlap time			1.05	1.40	1.75	µs
SYM f_B	Symmetry half bridge		[1][9]	0.9	1.0	1.1	
SYM T_{NO}	Symmetry non-overlap time		[11]		1.0		

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 13.0 V; C_{CF} = 100 pF; R_{RREF} = 33 kΩ; C_{CP} = 100 nF; C_{CI} = 100 nF; all voltages referenced to ground unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{tot}	Total supply current		[1][7]		1.5	2.0	mA
$I_{CI(charge)}$	Charge current at CI pin	V_{CI} = 1.5 V		36	44	52	µA
$I_{CI(discharge)}$	Discharge current at CI pin	V_{CI} = 1.5 V		74	90	106	µA
$\Delta I_{CF}/\Delta V_{CI}$	CI transconductance	V_{CI} = 1.5 V			12		µA/V
$V_{RS(cap)}$	Capacitive-mode control voltage		[8]	-40	-20	0	mV
V_{RREF}	Reference voltage			2.425	2.500	2.575	V
$V_{G1(on)}$	On voltage at pin G1	$\|I_{G1}\|$ = 1 mA		10.5			V
$V_{G1(off)}$	Off voltage at pin G1	$\|I_{G1}\|$ = 1 mA				0.3	V
VG2(on)	On voltage at pin G2	$\|I_{G2}\|$ = 1 mA		10.5			V
VG2(off)	Off voltage at pin G2	$\|I_{G2}\|$ = 1 mA				0.3	V
$R_{G1(on)}$	High side driver on resistance	$V_{(G1-S1)}$= 3 V			250		Ω
$R_{G1(off)}$	High side driver off resistance	$V_{(G1-S1)}$ = 3 V			35		Ω
$R_{G2(on)}$	Low side driver on resistance	V_{G2} = 3 V			250		Ω
$R_{G2(off)}$	Low side driver off resistance	V_{G2} = 3 V			35		Ω
V_{drop}	Voltage drop at bootstrap switch	I_{FS} = 5 mA			2.0		V
$R_{CP(disch)}$	On resistance switch at CP pin	V_{CP} = 0.6 V			120		Ω
Stop and end-of-life							
$V_{STOP(ref)}$	Stop reference level			1.21	1.26	1.31	V
$V_{STOP(reset)}$	Stop reset level		[10]	0.95	1.00	1.05	V
$V_{STOP(hys)}$	Stop hysteresis		[10]	0.20	0.25	0.30	V
$I_{STOP(ch)}$	Stop-charge current source	V_{STOP} = 0.75 V		2.0	2.5	3.0	µA
$I_{STOP(dis)}$	Stop discharge current	V_{STOP} = 0.75 V		0.35	0.50	0.65	µA
$R_{STOP(disch)}$	On resistance discharge switch	V_{STOP} = 0.5 V		1.0	2.5	4.0	kΩ
$V_{EOL(high)}$	High level end-of-life comparator			2.9	3.0	3.1	V
$V_{EOL(low)}$	Low level end-of-life comparator			1.9	2.0	2.1	V
Power-factor control							
$I_{VO(ref)}$	Output voltage reference current	V_{VO} = 3.0 V		97	102	107	µA
$V_{OVC(ref)}$	OVC reference level			1.21	1.26	1.31	V
T_{OVC}	Delay OVC comparator				60		ns
$V_{VO(low)}$	VO offset voltage				1.0		V
ΔV_{VO}	VO dynamic range				2.7		V
$I_{GZCD(start)}$	Start-up current at GZCD pin	V_{GZCD} = 0 V		35	42.5	50	µA
$I_{GZCD(on)}$	Turn on current at GZCD pin	V_{GZCD} = 3 V			12		µA
$V_{GZCD(start)}$	GZCD start level			1.9	2.0	2.1	V
$V_{GZCD(active)}$	GZCD active level	I_{GZCD}= 0.5 mA			6.4		V
T_{GZCD}	GZCD turn on delay				0.5		µs
$T_{ON(max)}$	Maximum on time	$V_{VO} = V_{VO(low)}$	[4]	20			µs
$T_{ON(min)}$	Minimum on time	$V_{VO} = V_{VO(off)}$	[3][10]		0.4	0.5	µs
$I_{GZCD(sink)}$	Gate drive sink current	V_{GZCD} = 4 V		200			mA

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 13.0 V; C_{CF} = 100 pF; R_{RREF} = 33 kΩ; C_{CP} = 100 nF; C_{CI} = 100 nF; all voltages referenced to ground unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{OFF}	Duration off pulse			0.9		µs
$V_{OVC(low)}$	OVC low voltage			120		mV
k_{VO}	VO low factor		0.86	0.95	0.99	
$V_{VO(off)}$	Off voltage PFC			3.7		V
$V_{VO(clamp)}$	Active VO clamp voltage	I_{VO} = 200 µA		4.7		V
$V_{VO(pas)}$	Passive VO clamp voltage	I_{VO} = 200 µA, V_{VDD} = 0 V		3.9		V

[1] Excluding situations where the excess charge control mechanism is active.

[2] The non-oscillation current is specified in a temperature range of 0 to 100 °C. For Tj < 0 °C and Tj > 100 °C the maximum start-up current is 350 µA.

[3] Minimum on-time is defined without the external MOSFET. V_{GZCD} is increased from 0 to 10 V in 1µs. T_{ONmin} is defined as the time elapsed between V_{GZCD} exceeding $V_{GZCD(start)}$ and V_{GZCD} being pulled below 3 V at turn-off.

[4] Maximum on-time is defined without the external MOSFET. Parameter is measured with V_{VO} = $V_{VO(low)}$ and V_{GZCD} is increased from 0 to 10 V in 1µs. T_{ONmax} is defined as the time elapsed between V_{GZCD} exceeding $V_{GZCD(start)}$ and V_{GZCD} pulled below 3 V at turn- off.

[5] Data sampling of $V_{RS(ph)}$ is performed at the end of conduction of T2 .

[6] Gain is defined as I_{CF}/I_{RS} with $V_{RS}>V_{RS(clamp)}$.

[7] Total supply current is specified in a T_j temperature range of -20 °C to 125 °C at f_B, excluding gate drive charge.

[8] Data sampling of $V_{RS(cap)}$ is performed at the start of conduction of T2 .

[9] The symmetry SYM f_B is calculated from the quotient SYM $f_B = T1_{tot}/T2_{tot}$, with $T1_{tot}$ being the time between turn-off of G2 and the turn-off of G1, and $T2_{tot}$ the time between turn-off of G1 and the turn-off of G2.

[10] Not measured, guaranteed by design.

[11] The symmetry SYM T_{NO} is defined as the ratio between deadtime1 and deadtime2. Deadtime1 is the time between turning off G1 and turning on G2. Deadtime2 is the time between turning off G2 and turning on G1.

11. Latch-up

Table 6. Latch-up

(Positive currents flow into pins)

Symbol	Parameter	Conditions	Min	Unit
$I_{latch\ up}$	Latch-up current	[1]		
	Pin RS	[1]	-30	mA
	Pin CF	[1]	-50	mA
	Pin STOP	[1]	-80	mA
	Pins VO, OVC, CI, CP, EOL, RREF, STOP, S1, FS, G1, G2, GZCD	[1]	-100	mA

[1] Negative latch-up currents tested at T_j = 150 °C by discharging a 22 mF capacitor through a 50 Ω series resistor. Positive latch-up currents according to quality specification.

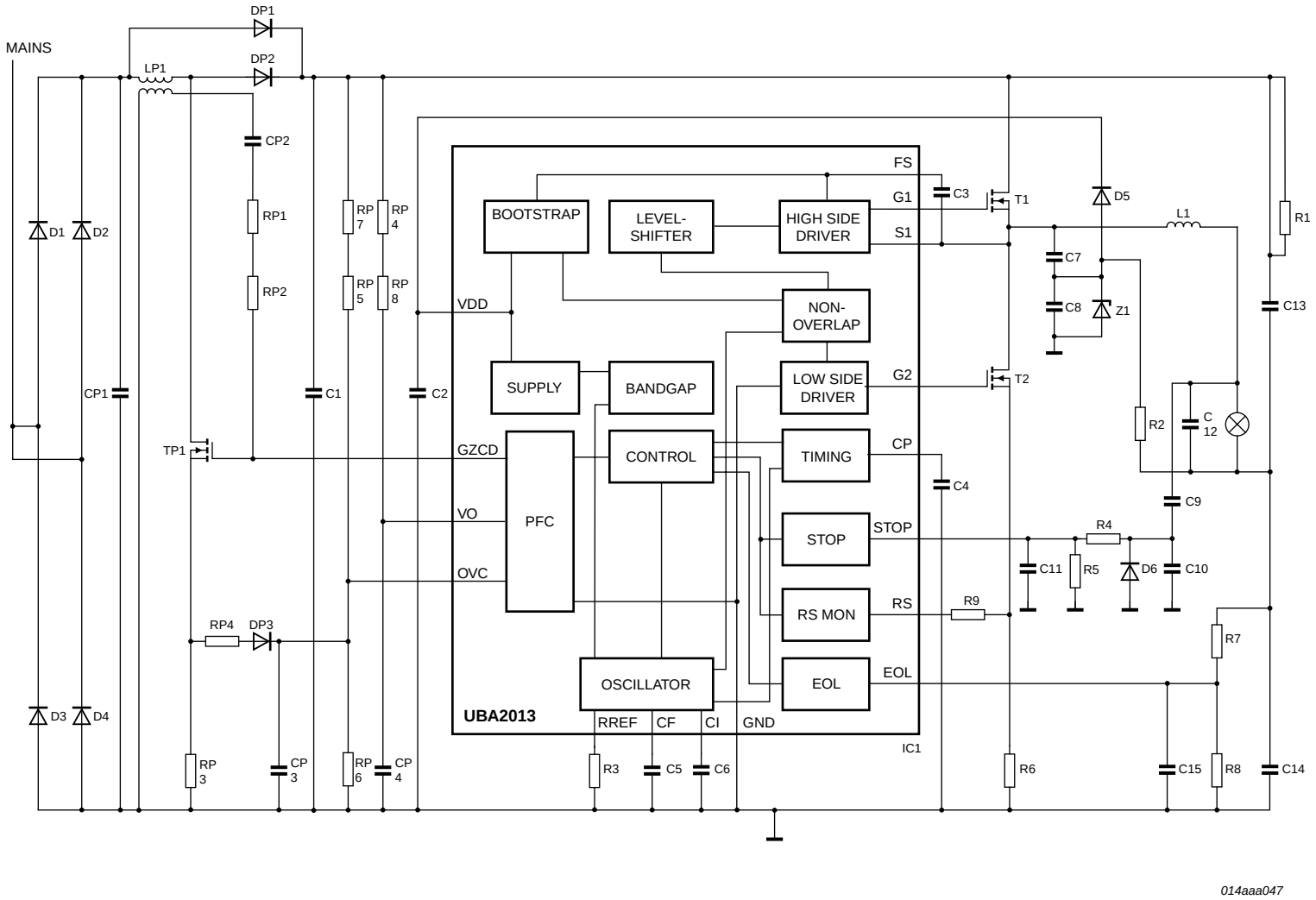


Fig 6. Application diagram of UBA2013L/3

12.1 Design equations

Equation 1 through Equation 5 give the design equations for the UBA2013:

Table 7. UBA2013 parameters (typical)

X1 = 3.24	Rint = 3 kΩ
t = 300ns	Cpar = 5 pF (typ)

Bottom frequency fb is set by RREF and CF:

$$f_B = \frac{1}{2 \times \{[(C_{CF} + C_{par}) \times (X1 \times R_{RREF} - R_{int})] + \tau\}}(Hz) \quad (1)$$

Preheat time Tpreh is set by RREF and CP:

$$T_{preh} = 674 \times \frac{C_{CP}}{100\,nF} \times \frac{R_{RREF}}{33\,k\Omega}(ms) \quad (2)$$

Ignition time Tign is set by RREF and CP:

$$T_{ign} = 611 \times \frac{C_{CP}}{100nF} \times \frac{R_{RREF}}{33k\Omega}(ms) \quad (3)$$

Non-overlap time Tno is set by RREF:

$$T_{no} = 0.15 + 1.25 \times \frac{R_{RREF}}{33k\Omega}(\mu s) \quad (4)$$

PFC on-time Ton:

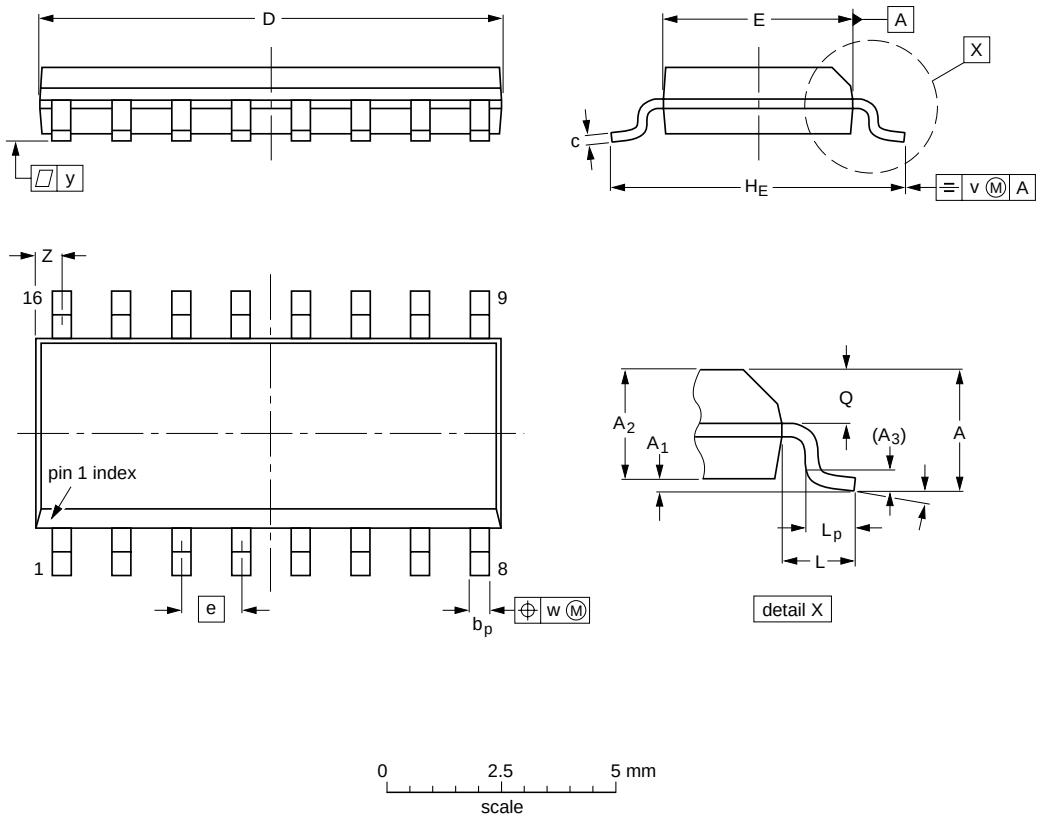
$$T_{ON}(V_{VO}) = T_{ON(max)} - \frac{(T_{ON(max)} - T_{ON(min)})}{\Delta V_{VO}} \times (V_{VO} - V_{VO(low)}) \quad (5)$$

13. Test information

The *General Quality Specification for Integrated Circuits SNW-FQ-611-E* is applicable.

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT109-1 (SO16)

15.1 State diagram and state transitions

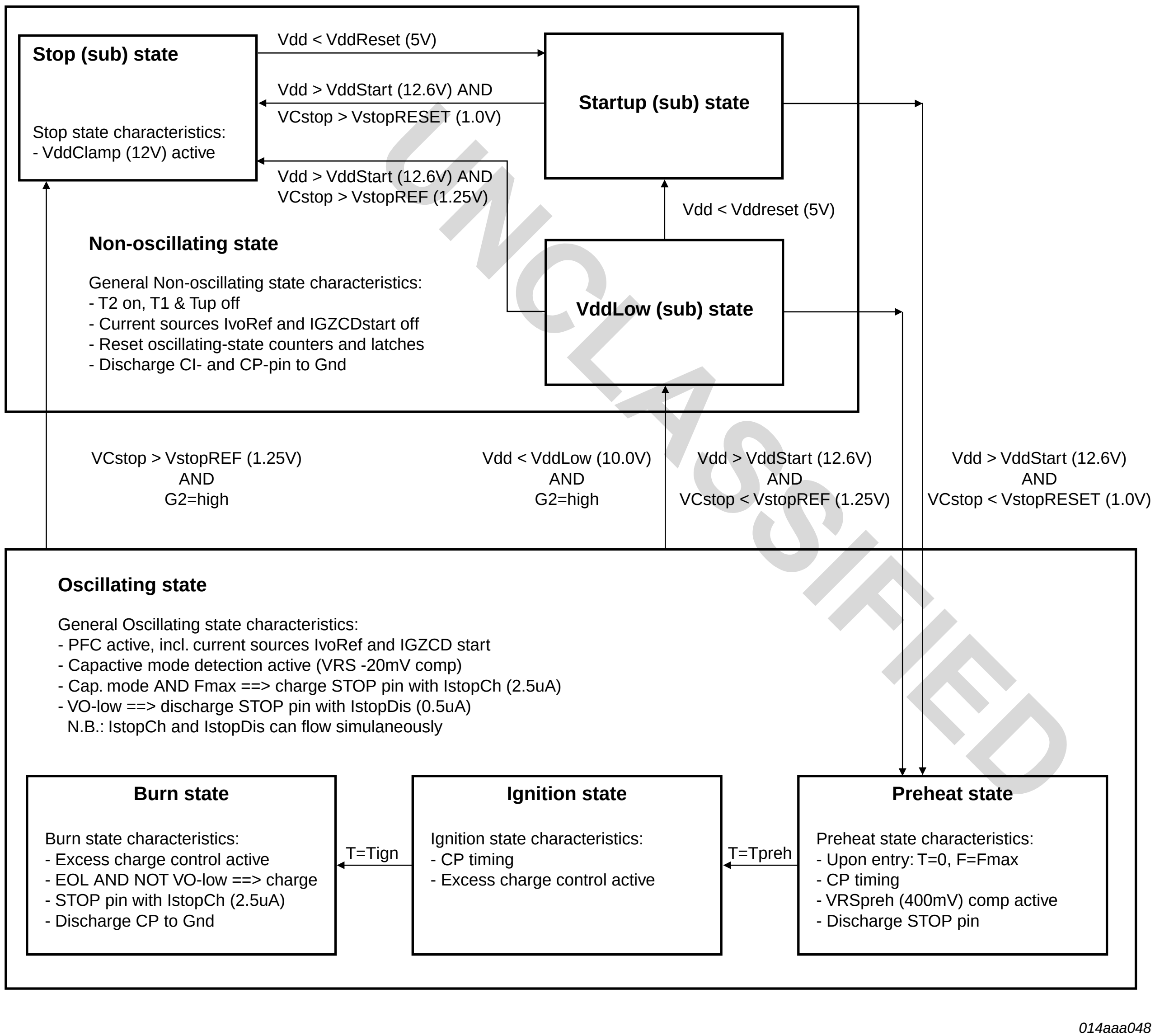


Fig 8. State diagram and state transitions

16. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2013L_1	<yyyymmdd>	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Tables

continued >>

20. Figures

continued >>

21. Contents

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