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MTP12N08L
MTP12N10L

Designer's Data Sheet

Power Field Effect Transistor

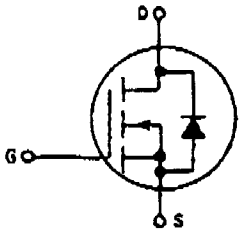
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
LOGIC LEVEL
AMPERES
$r_{DS(on)}$ = 0.18 OHM
80 and 100 VOLTS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

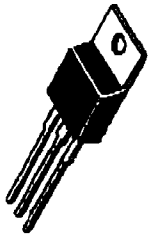
- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



MAXIMUM RATINGS

Rating	Symbol	MTP12N08L	MTP12N10L	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage	V_{GS}	±15		Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C



TO-220AB

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	MTP12N08L MTP12N10L	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	1 50	μAdc

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)				
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)	$V_{GS(th)}$	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 100°C)	$V_{DS(on)}$	— —	2.4 1.6	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 6 A)	g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	800	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	2600	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	350	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	1600	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{oss}	—	100	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	130	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 11 and 12.	Q_g	15 (typ)	25	nC
Gate-Source Charge		Q_{gs}	3.7 (typ)	—	
Gate-Drain Charge		Q_{gd}	11.3 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 14 and 15.	V_{SD}	1 (typ)	1.25	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (typ) 4.5 (typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.