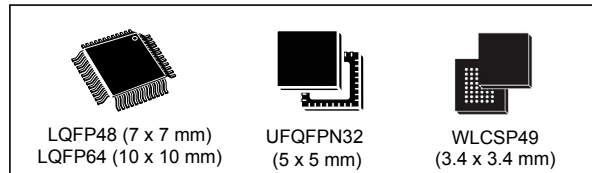


## ARM<sup>®</sup>-Cortex<sup>®</sup>-M4 32-bit MCU+FPU, up to 64 KB Flash, 16 KB SRAM, ADC, DAC, COMP, Op-Amp, 2.0 – 3.6 V

Datasheet - production data

### Features

- Core: ARM<sup>®</sup> 32-bit Cortex<sup>®</sup>-M4 CPU with FPU (72 MHz max.), single-cycle multiplication and HW division, DSP instruction
- Memories
  - 32 to 64 Kbyte of Flash memory
  - 16 Kbyte of SRAM on data bus
- CRC calculation unit
- Reset and power management
  - WDD, VDDA voltage range: 2.0 to 3.6
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low-power: Sleep, Stop, and Standby
  - V<sub>BAT</sub> supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 51 fast I/O ports, all mappable on external interrupt vectors, several 5 V-tolerant
- 7-channel DMA controller supporting timers, ADCs, SPIs, I<sup>2</sup>Cs, USARTs and DAC
- 1 × ADC 0.20 μs (up to 15 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, single ended/differential mode, separate analog supply from 2.0 to 3.6
- Temperature sensor
- 1 × 12-bit DAC channel with analog supply from 2.4 to 3.6 V
- Three fast rail-to-rail analog comparators with analog supply from 2.0 to 3.6 V
- 1 × operational amplifier that can be used in PGA mode, all terminal accessible with analog supply from 2.4 to 3.6 V



- Up to 18 capacitive sensing channels supporting touchkey, linear and rotary sensors
- Up to 9 timers
  - One 32-bit timer with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - One 16-bit 6-channel advanced-control timer, with up to 6 PWM channels, deadtime generation and emergency stop
  - Three 16-bit timers with IC/OC/OCN or PWM, deadtime gen. and emergency stop
  - One 16-bit basic timer to drive the DAC
  - 2 watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
- Calendar RTC with alarm, periodic wakeup from Stop/Standby
- Communication interfaces
  - Three I2Cs with 20 mA current sink to support Fast mode plus
  - Up to 3 USARTs, 1 with ISO 7816 I/F, autobaudrate detect and Dual clock domain
  - Up to two SPIs with multiplexed full duplex I2S
  - Infrared transmitter
- Serial wire debug (SWD), JTAG
- 96-bit unique ID

**Table 1. Device summary**

Reference	Part number
STM32F301x6	STM32F301R6, STM32F301C6, STM32F301K6
STM32F301x8	STM32F301R8, STM32F301C8, STM32F301K8

# Contents

<b>1</b>	<b>Introduction</b>	<b>8</b>
<b>2</b>	<b>Description</b>	<b>9</b>
<b>3</b>	<b>Functional overview</b>	<b>12</b>
3.1	ARM <sup>®</sup> Cortex <sup>®</sup> -M4 core with FPU, embedded Flash and SRAM	12
3.2	Memories	12
3.2.1	Embedded Flash memory	12
3.2.2	Embedded SRAM	12
3.3	Boot modes	12
3.4	Cyclic redundancy check calculation unit (CRC)	13
3.5	Power management	13
3.5.1	Power supply schemes	13
3.5.2	Power supply supervisor	13
3.5.3	Voltage regulator	14
3.5.4	Low-power modes	14
3.6	Interconnect matrix	14
3.7	Clocks and startup	15
3.8	General-purpose inputs/outputs (GPIOs)	17
3.9	Direct memory access (DMA)	17
3.10	Interrupts and events	17
3.10.1	Nested vectored interrupt controller (NVIC)	17
3.11	Fast analog-to-digital converter (ADC)	18
3.11.1	Temperature sensor	18
3.11.2	Internal voltage reference ( $V_{REFINT}$ )	18
3.11.3	$V_{BAT}$ battery voltage monitoring	19
3.12	Digital-to-analog converter (DAC)	19
3.13	Operational amplifier (OPAMP)	19
3.14	Ultra-fast comparators (COMP)	19
3.15	Timers and watchdogs	20
3.15.1	Advanced timer (TIM1)	20
3.15.2	General-purpose timers (TIM2, TIM15, TIM16, TIM17)	21
3.15.3	Basic timer (TIM6)	21

3.15.4	Independent watchdog (IWDG)	21
3.15.5	Window watchdog (WWDG)	22
3.15.6	SysTick timer	22
3.16	Real-time clock (RTC) and backup registers	22
3.17	Inter-integrated circuit interfaces (I <sup>2</sup> C)	23
3.18	Universal synchronous/asynchronous receiver transmitter (USART)	24
3.19	Serial peripheral interfaces (SPI)/Inter-integrated sound interfaces (I2S)	24
3.20	Touch sensing controller (TSC)	25
3.21	Infrared transmitter	27
3.22	Development support	28
3.22.1	Serial wire JTAG debug port (SWJ-DP)	28
<b>4</b>	<b>Pinouts and pin description</b>	<b>29</b>
<b>5</b>	<b>Memory mapping</b>	<b>46</b>
<b>6</b>	<b>Electrical characteristics</b>	<b>49</b>
6.1	Parameter conditions	49
6.1.1	Minimum and maximum values	49
6.1.2	Typical values	49
6.1.3	Typical curves	49
6.1.4	Loading capacitor	49
6.1.5	Pin input voltage	49
6.1.6	Power supply scheme	50
6.1.7	Current consumption measurement	51
6.2	Absolute maximum ratings	52
6.3	Operating conditions	54
6.3.1	General operating conditions	54
6.3.2	Operating conditions at power-up / power-down	55
6.3.3	Embedded reset and power control block characteristics	55
6.3.4	Embedded reference voltage	57
6.3.5	Supply current characteristics	57
6.3.6	Wakeup time from low-power mode	69
6.3.7	External clock source characteristics	70
6.3.8	Internal clock source characteristics	76

6.3.9	PLL characteristics	77
6.3.10	Memory characteristics	78
6.3.11	EMC characteristics	79
6.3.12	Electrical sensitivity characteristics	80
6.3.13	I/O current injection characteristics	81
6.3.14	I/O port characteristics	82
6.3.15	NRST pin characteristics	87
6.3.16	Timer characteristics	88
6.3.17	Communications interfaces	90
6.3.18	ADC characteristics	96
6.3.19	DAC electrical specifications	104
6.3.20	Comparator characteristics	105
6.3.21	Operational amplifier characteristics	107
6.3.22	Temperature sensor characteristics	110
6.3.23	V <sub>BAT</sub> monitoring characteristics	110
<b>7</b>	<b>Package characteristics</b>	<b>111</b>
7.1	Package mechanical data	111
7.2	Thermal characteristics	125
7.2.1	Reference document	125
7.2.2	Selecting the product temperature range	126
<b>8</b>	<b>Part numbering</b>	<b>128</b>
<b>9</b>	<b>Revision history</b>	<b>129</b>

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	STM32F301x6/x8 device features and peripheral counts. . . . .	10
Table 3.	STM32F301x6/x8 peripheral interconnect matrix. . . . .	15
Table 4.	Timer feature comparison. . . . .	20
Table 5.	Comparison of I2C analog and digital filters. . . . .	23
Table 6.	STM32F301x6/x8 I <sup>2</sup> C implementation . . . . .	23
Table 7.	USART features . . . . .	24
Table 8.	STM32F301x6/x8 SPI/I2S implementation . . . . .	25
Table 9.	Capacitive sensing GPIOs available on STM32F301x6/x8 devices. . . . .	26
Table 10.	No. of capacitive sensing channels available on STM32F301x6/x8 devices . . . . .	27
Table 11.	Legend/abbreviations used in the pinout table . . . . .	32
Table 12.	STM32F301x6/x8 pin definitions. . . . .	33
Table 13.	Alternate functions for Port A . . . . .	40
Table 14.	Alternate functions for Port B . . . . .	42
Table 15.	Alternate functions for Port C . . . . .	44
Table 16.	Alternate functions for Port D . . . . .	45
Table 17.	Alternate functions for Port F . . . . .	45
Table 18.	STM32F301x6/x8 peripheral register boundary addresses . . . . .	47
Table 19.	Voltage characteristics . . . . .	52
Table 20.	Current characteristics . . . . .	53
Table 21.	Thermal characteristics. . . . .	53
Table 22.	General operating conditions . . . . .	54
Table 23.	Operating conditions at power-up / power-down . . . . .	55
Table 24.	Embedded reset and power control block characteristics. . . . .	55
Table 25.	Programmable voltage detector characteristics . . . . .	56
Table 26.	Embedded internal reference voltage . . . . .	57
Table 27.	Internal reference voltage calibration values . . . . .	57
Table 28.	Typical and maximum current consumption from VDD supply at VDD = 3.6V . . . . .	58
Table 29.	Typical and maximum current consumption from the V <sub>DDA</sub> supply . . . . .	60
Table 30.	Typical and maximum V <sub>DD</sub> consumption in Stop and Standby modes. . . . .	60
Table 31.	Typical and maximum V <sub>DDA</sub> consumption in Stop and Standby modes. . . . .	61
Table 32.	Typical and maximum current consumption from V <sub>BAT</sub> supply. . . . .	61
Table 33.	Typical current consumption in Run mode, code with data processing running from Flash . . . . .	63
Table 34.	Typical current consumption in Sleep mode, code running from Flash or RAM. . . . .	64
Table 35.	Switching output I/O current consumption . . . . .	66
Table 36.	Peripheral current consumption . . . . .	68
Table 37.	Low-power mode wakeup timings. . . . .	69
Table 38.	High-speed external user clock characteristics. . . . .	70
Table 39.	Low-speed external user clock characteristics . . . . .	71
Table 40.	HSE oscillator characteristics . . . . .	72
Table 41.	LSE oscillator characteristics (f <sub>LSE</sub> = 32.768 kHz) . . . . .	74
Table 42.	HSI oscillator characteristics. . . . .	76
Table 43.	LSI oscillator characteristics . . . . .	77
Table 44.	PLL characteristics . . . . .	77
Table 45.	Flash memory characteristics . . . . .	78
Table 46.	Flash memory endurance and data retention. . . . .	78
Table 47.	EMS characteristics . . . . .	79

Table 48.	EMI characteristics	80
Table 49.	ESD absolute maximum ratings	80
Table 50.	Electrical sensitivities	81
Table 51.	I/O current injection susceptibility	81
Table 52.	I/O static characteristics	82
Table 53.	Output voltage characteristics	85
Table 54.	I/O AC characteristics	86
Table 55.	NRST pin characteristics	87
Table 56.	TIMx characteristics	88
Table 57.	IWDG min/max timeout period at 40 kHz (LSI)	89
Table 58.	WWDG min-max timeout value @72 MHz (PCLK)	89
Table 59.	I2C analog filter characteristics	90
Table 60.	SPI characteristics	91
Table 61.	I2S characteristics	93
Table 62.	ADC characteristics	96
Table 63.	Maximum ADC RAIN	97
Table 64.	ADC accuracy - limited test conditions	99
Table 65.	ADC accuracy	101
Table 66.	ADC accuracy	102
Table 67.	DAC characteristics	104
Table 68.	Comparator characteristics	105
Table 69.	Operational amplifier characteristics	107
Table 70.	TS characteristics	110
Table 71.	Temperature sensor calibration values	110
Table 72.	V <sub>BAT</sub> monitoring characteristics	110
Table 73.	WLCSP49 wafer level chip size package mechanical data	113
Table 74.	LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data	116
Table 75.	LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package mechanical data	119
Table 76.	32-lead, ultra thin, fine pitch quad flat no-lead package mechanical data	122
Table 77.	Package thermal characteristics	125
Table 78.	Ordering information scheme	128
Table 79.	Document revision history	129

## List of figures

Figure 1.	STM32F301x6/x8 block diagram	11
Figure 2.	Clock tree	16
Figure 3.	Infrared transmitter	27
Figure 4.	STM32F301x6/x8 UFQFN32 pinout	29
Figure 5.	STM32F301x6/x8 LQFP48 pinout	29
Figure 6.	STM32F301x6/x8 LQFP64 pinout	30
Figure 7.	STM32F301x6/x8 WLCSP49 ballout	31
Figure 8.	STM32F301x6/x8 memory mapping	46
Figure 9.	Pin loading conditions	49
Figure 10.	Pin input voltage	49
Figure 11.	Power supply scheme	50
Figure 12.	Current consumption measurement scheme	51
Figure 13.	Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')	62
Figure 14.	High-speed external clock source AC timing diagram	70
Figure 15.	Low-speed external clock source AC timing diagram	71
Figure 16.	Typical application with an 8 MHz crystal	73
Figure 17.	Typical application with a 32.768 kHz crystal	75
Figure 18.	HSI oscillator accuracy characterization results	76
Figure 19.	TC and TTA I/O input characteristics - CMOS port	83
Figure 20.	TC and TTA I/O input characteristics - TTL port	83
Figure 21.	Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port	84
Figure 22.	Five volt tolerant (FT and FTf) I/O input characteristics - TTL port	84
Figure 23.	I/O AC characteristics definition	87
Figure 24.	Recommended NRST pin protection	88
Figure 25.	SPI timing diagram - slave mode and CPHA = 0	92
Figure 26.	SPI timing diagram - slave mode and CPHA = 1 <sup>(1)</sup>	92
Figure 27.	SPI timing diagram - master mode <sup>(1)</sup>	93
Figure 28.	I <sup>2</sup> S slave timing diagram (Philips protocol) <sup>(1)</sup>	95
Figure 29.	I <sup>2</sup> S master timing diagram (Philips protocol) <sup>(1)</sup>	95
Figure 30.	ADC accuracy characteristics	103
Figure 31.	Typical connection diagram using the ADC	103
Figure 32.	12-bit buffered /non-buffered DAC	105
Figure 33.	OPAMP Voltage Noise versus Frequency	109
Figure 34.	WLCSP49 wafer level chip size package	112
Figure 35.	WLCSP49 package top view	114
Figure 36.	LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline	115
Figure 37.	LQFP64 recommended footprint	116
Figure 38.	LQFP64 package top view	117
Figure 39.	LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline	118
Figure 40.	LQFP48 recommended footprint	120
Figure 41.	LQFP48 package top view	121
Figure 42.	32-lead, ultra thin, fine pitch quad flat no-lead package (5 x 5)	122
Figure 43.	UFQFPN32 recommended footprint	123
Figure 44.	UFQFPN32 package top view	124

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F301x6/x8 microcontrollers.

This datasheet should be read in conjunction with the STM32F302xx advanced ARM-based 32-bit MCUs reference manual (RM0366). The reference manual is available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the ARM<sup>®</sup> Cortex<sup>®</sup>-M4 core, please refer to the Cortex<sup>®</sup>-M4 Technical Reference Manual, available from ARM website [www.arm.com](http://www.arm.com).





## 2 Description

The STM32F301x6/x8 family is based on the high-performance ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit RISC core operating at a frequency of up to 72 MHz and embedding a floating point unit (FPU). The family incorporates high-speed embedded memories (up to 64 Kbyte of Flash memory, 16 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer a fast 12-bit ADC (5 Msps), three comparators, an operational amplifier, up to 18 capacitive sensing channels, one DAC channel, a low-power RTC, one general-purpose 32-bit timer, one timer dedicated to motor control, and up to three general-purpose 16-bit timers, and one timer to drive the DAC. They also feature standard and advanced communication interfaces: three I<sup>2</sup>Cs, up to three USARTs, up to two SPIs with multiplexed full-duplex I2Ss, and an infrared transmitter.

The STM32F301x6/x8 family operates in the –40 to +85°C and –40 to +105°C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

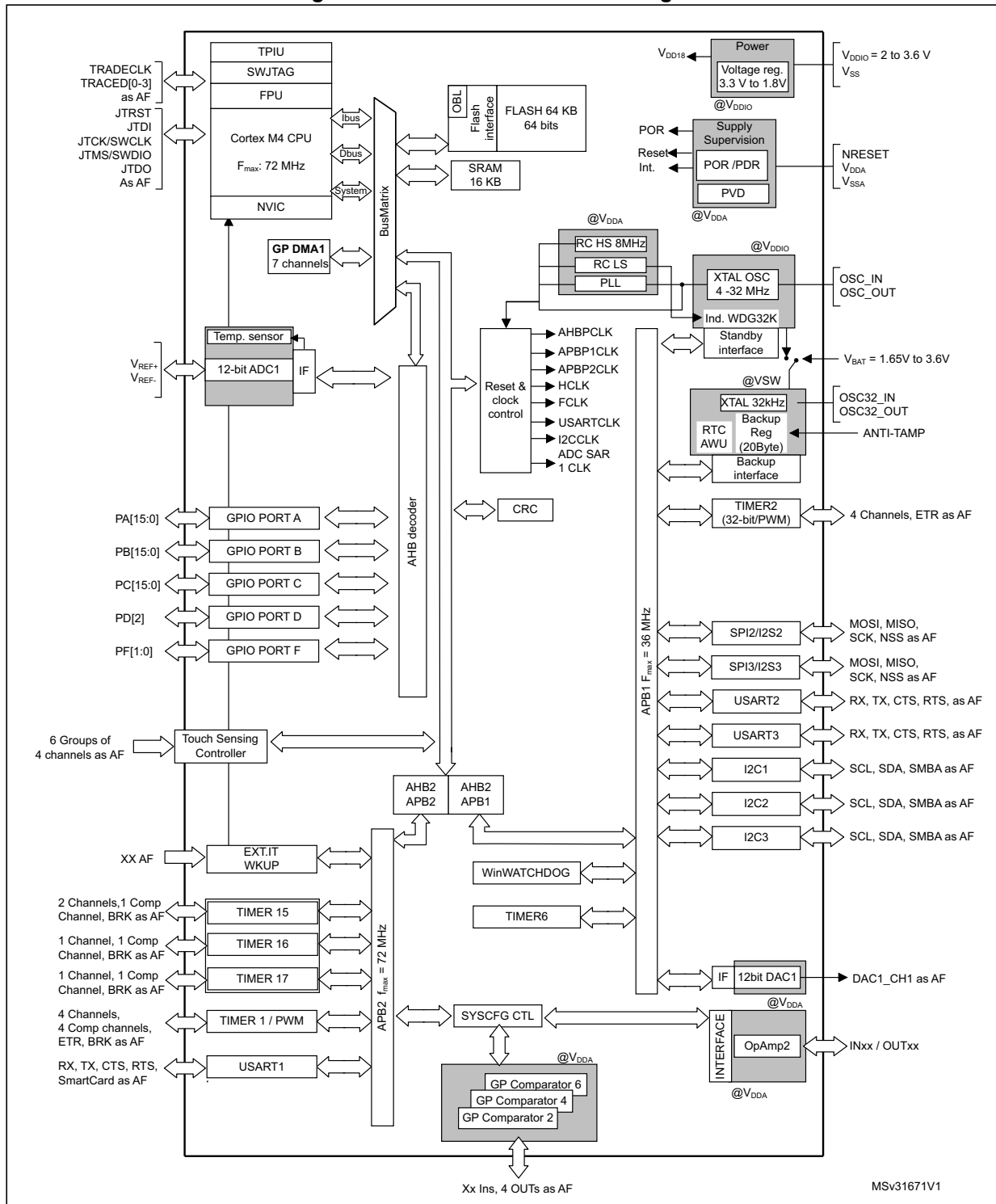
The STM32F301x6/x8 family offers devices in 32-, 48-, 49- and 64-pin packages.

The set of included peripherals changes with the device chosen.

Table 2. STM32F301x6/x8 device features and peripheral counts

Peripheral		STM32F301Kx		STM32F301Cx		STM32F301Rx	
Flash (Kbytes)		32	64	32	64	32	64
SRAM (Kbytes)		16					
Timers	Advanced control	1 (16-bit)					
	General purpose	3 (16-bit) 1 (32 bit)					
	Basic	1					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Comm. interfaces	SPI/I2S	2					
	I <sup>2</sup> C3						
	USART	2		3			
DMA channels		7					
Capacitive sensing channels		18					
12-bit ADC Number of channels		1 8		1 11		1 15	
12-bit DAC channels		1					
Analog comparator		3					
Operational amplifier		1					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85°C / - 40 to 105°C Junction temperature: - 40 to 125°C					
Packages		UFQFPN32		LQFP48, WLCSP49		LQFP64	

Figure 1. STM32F301x6/x8 block diagram



1. AF: alternate function on I/O pins.

## 3 Functional overview

### 3.1 ARM<sup>®</sup> Cortex<sup>®</sup>-M4 core with FPU, embedded Flash and SRAM

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single-precision FPU speeds up software development by using metalanguage development tools while avoiding saturation.

With its embedded ARM core, the STM32F301x6/x8 family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32F301x6/x8 family devices.

### 3.2 Memories

#### 3.2.1 Embedded Flash memory

All STM32F301x6/x8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

#### 3.2.2 Embedded SRAM

STM32F301x6/x8 devices feature 16 Kbytes of embedded SRAM.

### 3.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10) and USART2 (PA2/PA3).

## 3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.5 Power management

### 3.5.1 Power supply schemes

- $V_{SS}$ ,  $V_{DD} = 2.0$  to  $3.6$  V: external power supply for I/Os and the internal regulator. It is provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 2.0$  to  $3.6$  V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL (minimum voltage to be applied to  $V_{DDA}$  is  $2.4$  V when the DAC and operational amplifier are used). The  $V_{DDA}$  voltage level must be always greater or equal to the  $V_{DD}$  voltage level and must be provided first.
- $V_{BAT} = 1.65$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

### 3.5.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of  $2$  V. The device remains in reset mode when the monitored supply voltage is below a specified threshold,  $VPOR/PDR$ , without the need for an external reset circuit.

- The POR monitors only the  $V_{DD}$  supply voltage. During the startup phase it is required that  $V_{DDA}$  should arrive first and be greater than or equal to  $V_{DD}$ .
- The PDR monitors both the  $V_{DD}$  and  $V_{DDA}$  supply voltages, however the  $V_{DDA}$  power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that  $V_{DDA}$  is higher than or equal to  $V_{DD}$ .

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $VPVD$  threshold. An interrupt can be generated when  $V_{DD}$  drops below the  $VPVD$  threshold and/or when  $V_{DD}$  is higher than the  $VPVD$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.5.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

### 3.5.4 Low-power modes

The STM32F301x6/x8 supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode  
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode  
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.  
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, COMPx, I2C or USARTx.
- Standby mode  
The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.  
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.6 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 3. STM32F301x6/x8 peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADC1 DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Comp <sub>x</sub>	Comparator output blanking
COMP <sub>x</sub>	TIMx	Timer input: ocrefclear input, input capture
ADC1	TIM1	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMP <sub>x</sub> PVD GPIO	TIM1 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADC1 DAC1	Conversion external trigger
DAC1	COMP <sub>x</sub>	Comparator inverting input

*Note:* For more details about the interconnect actions, please refer to the corresponding sections in the F301xx reference manual RM0366.

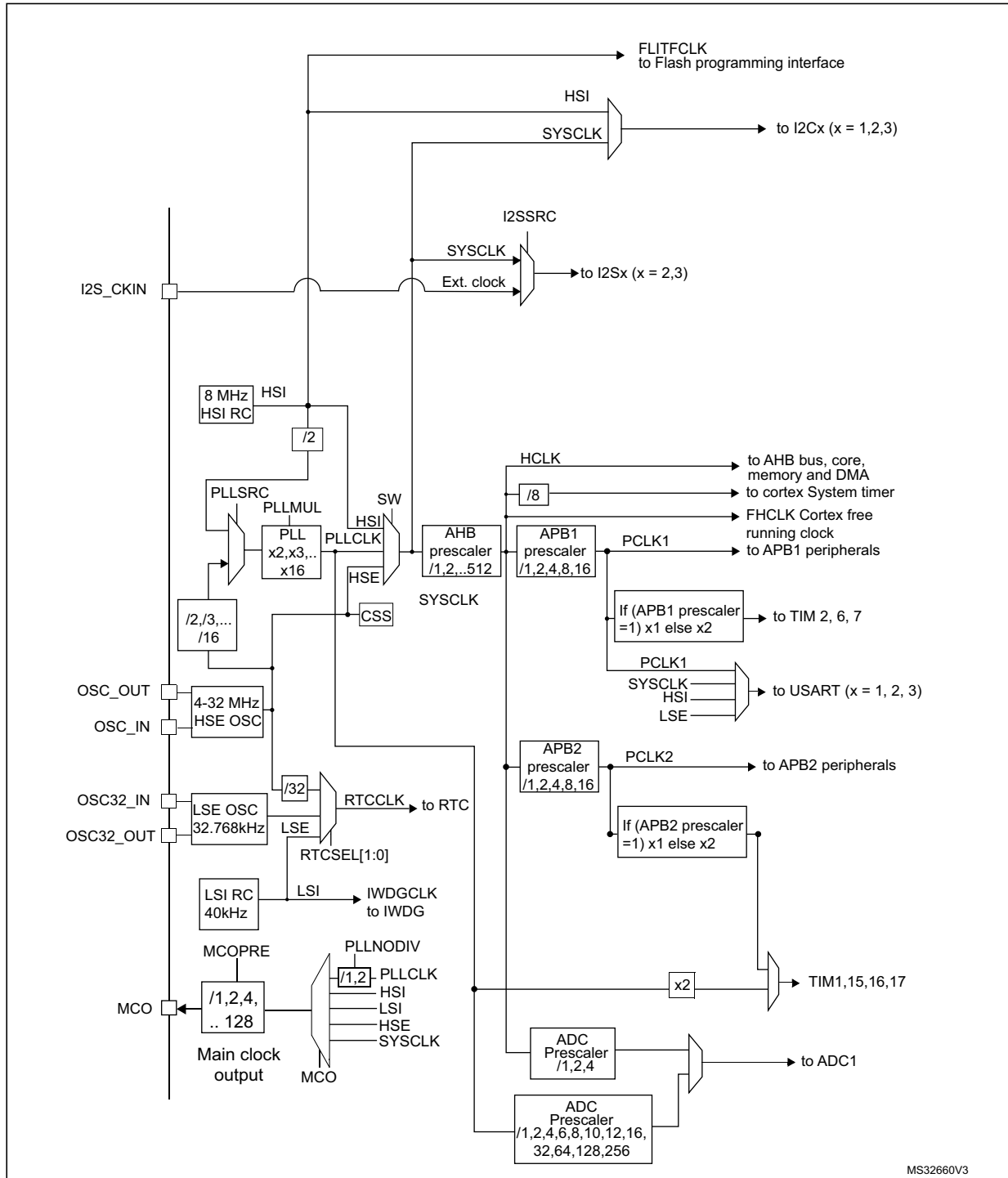
### 3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. To achieve audio class performance, an audio crystal can be used.

Figure 2. Clock tree





## 3.8 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

## 3.9 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I<sup>2</sup>C, USART, timers, DAC and ADC.

## 3.10 Interrupts and events

### 3.10.1 Nested vectored interrupt controller (NVIC)

The STM32F301x6/x8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.11 Fast analog-to-digital converter (ADC)

An analog-to-digital converter, with selectable resolution between 12 and 6 bit, is embedded in the STM32F301x6/x8 family devices. The ADC has up to 15 external channels performing conversions in single-shot or scan modes. Channels can be configured to be either single-ended input or differential input. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available. The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 3.11.1 Temperature sensor

The temperature sensor (TS) generates a voltage  $V_{\text{SENSE}}$  that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

### 3.11.2 Internal voltage reference ( $V_{\text{REFINT}}$ )

The internal voltage reference ( $V_{\text{REFINT}}$ ) provides a stable (bandgap) voltage output for the ADC and Comparators.  $V_{\text{REFINT}}$  is internally connected to the ADC1\_IN18 input channel. The precise voltage of  $V_{\text{REFINT}}$  is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

### 3.11.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the  $V_{BAT}$  battery voltage using the internal ADC channel ADC1\_IN17. As the  $V_{BAT}$  voltage may be higher than  $V_{DDA}$ , and thus outside the ADC input range, the  $V_{BAT}$  pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the  $V_{BAT}$  voltage.

## 3.12 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1\_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

## 3.13 Operational amplifier (OPAMP)

The STM32F301x6/x8 embeds one operational amplifier with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When the operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

## 3.14 Ultra-fast comparators (COMP)

The STM32F301x6/x8 devices embed three ultra-fast rail-to-rail comparators which offer the features below:

- Programmable internal or external reference voltage
- Selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 26: Embedded internal reference voltage](#) for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, and also generate interrupts and breaks for the timers.

### 3.15 Timers and watchdogs

The STM32F301x6/x8 includes advanced control timer, up to general-purpose timers, basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare Channels	Complementary outputs
Advanced control	TIM1 <sup>(1)</sup>	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
	TIM15 <sup>(1)</sup>	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TIM16 <sup>(1)</sup> , TIM17 <sup>(1)</sup>	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. TIM1/15/16/17 can be clocked from the PLL running at 144 MHz when the system clock source is the PLL and AHB or APB2 subsystem clocks are not divided by more than 2 cumulatively.

#### 3.15.1 Advanced timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in [Section 3.15.2](#) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### 3.15.2 General-purpose timers (TIM2, TIM15, TIM16, TIM17)

There are up to four synchronizable general-purpose timers embedded in the STM32F301x6/x8 (see [Table 4](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

#### TIM2

TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

It features 4 independent channels for input capture/output compare, PWM or one-pulse mode output. It can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

It has independent DMA request generation and supports quadrature encoders.

#### TIM15, TIM16 and TIM 17

These three timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM15 has 2 channels and 1 complementary channel
- TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

### 3.15.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

### 3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.15.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 3.16 Real-time clock (RTC) and backup registers

The RTC and the 20 backup registers are supplied through a switch that takes power from either the  $V_{DD}$  supply when present or the VBAT pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when  $V_{DD}$  power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

### 3.17 Inter-integrated circuit interfaces (I<sup>2</sup>C)

The devices feature three I<sup>2</sup>C bus interfaces which can operate in multimaster and slave mode. Each I2C interface can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

All I<sup>2</sup>C interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 5. Comparison of I2C analog and digital filters**

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2Cx (x=1,3) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to [Table 6](#) for the features available in I2C1, I2C2 and I2C3.

**Table 6. STM32F301x6/x8 I<sup>2</sup>C implementation**

I2C features <sup>(1)</sup>	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
SMBus	X	X	X
Wakeup from STOP	X	X	X

1. X = supported.

### 3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F301x6/x8 devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

All USARTs support hardware management of the CTS and RTS signals, multiprocessor communication mode, single-wire half-duplex communication mode and synchronous mode.

USART1 supports Smartcard mode, IrDA SIR ENDEC, LIN Master capability and autobaudrate detection.

All USART interfaces can be served by the DMA controller.

Refer to [Table 7](#) for the features available in all USARTs interfaces.

**Table 7. USART features**

USART modes/features <sup>(1)</sup>	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X		
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X		
LIN mode	X		
Dual clock domain and wakeup from Stop mode	X		
Receiver timeout interrupt	X		
Modbus communication	X		
Auto baud rate detection	X		
Driver Enable	X	X	X

1. X = supported.

### 3.19 Serial peripheral interfaces (SPI)/Inter-integrated sound interfaces (I2S)

Two SPI interfaces (SPI2 and SPI3) allow communication up to 18 Mbits/s in slave and master modes in full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master



mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to [Table 8](#) for the features available in SPI2 and SPI3.

**Table 8. STM32F301x6/x8 SPI/I2S implementation**

SPI features <sup>(1)</sup>	SPI2	SPI3
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	X
TI mode	X	X

1. X = supported.

### 3.20 Touch sensing controller (TSC)

The STM32F301x6/x8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Table 9. Capacitive sensing GPIOs available on STM32F301x6/x8 devices

Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0
	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO1	PC5
	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
4	TSC_G4_IO1	PA9
	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA13
	TSC_G4_IO4	PA14
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
6	TSC_G6_IO1	PB11
	TSC_G6_IO2	PB12
	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14

**Table 10. No. of capacitive sensing channels available on STM32F301x6/x8 devices**

Analog I/O group	Number of capacitive sensing channels		
	STM32F301Rx	STM32F301Cx	STM32F301Kx
G1	3	3	3
G2	3	3	3
G3	3	2	1
G4	3	3	3
G5	3	3	3
G6	3	3	0
Number of capacitive sensing channels	18	17	13

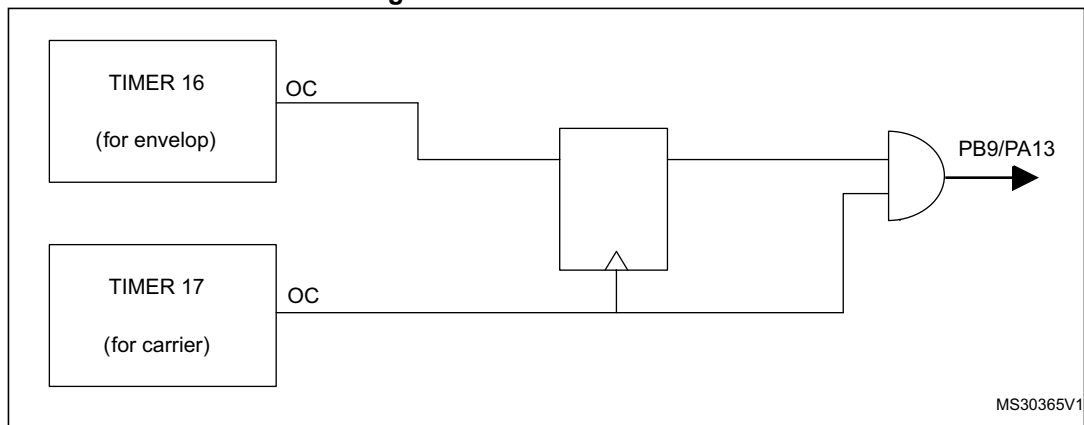
### 3.21 Infrared transmitter

The STM32F301x6/x8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

**Figure 3. Infrared transmitter**



## 3.22 Development support

### 3.22.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## 4 Pinouts and pin description

Figure 4. STM32F301x6/x8 UFQFN32 pinout

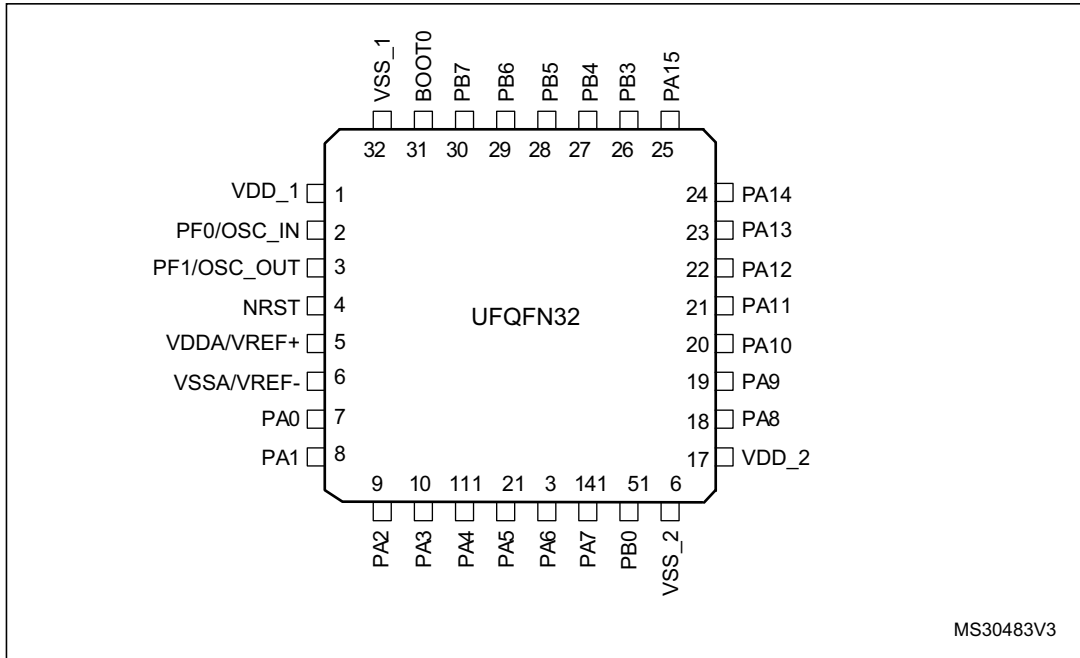


Figure 5. STM32F301x6/x8 LQFP48 pinout

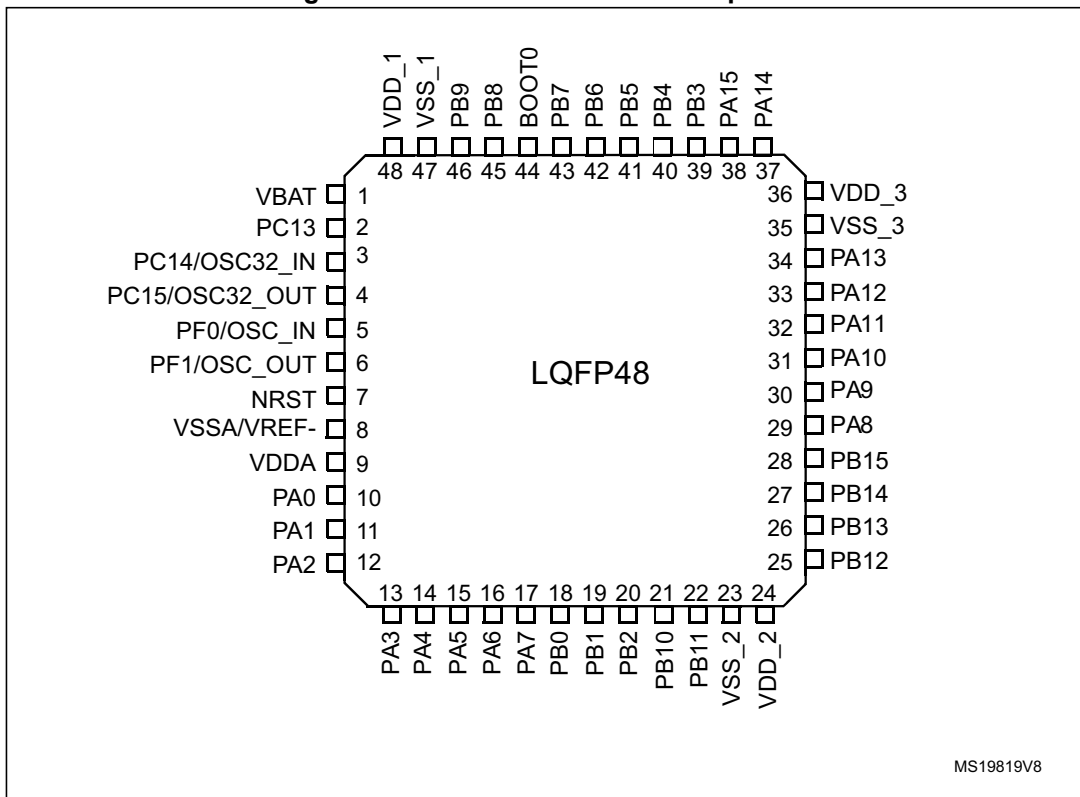
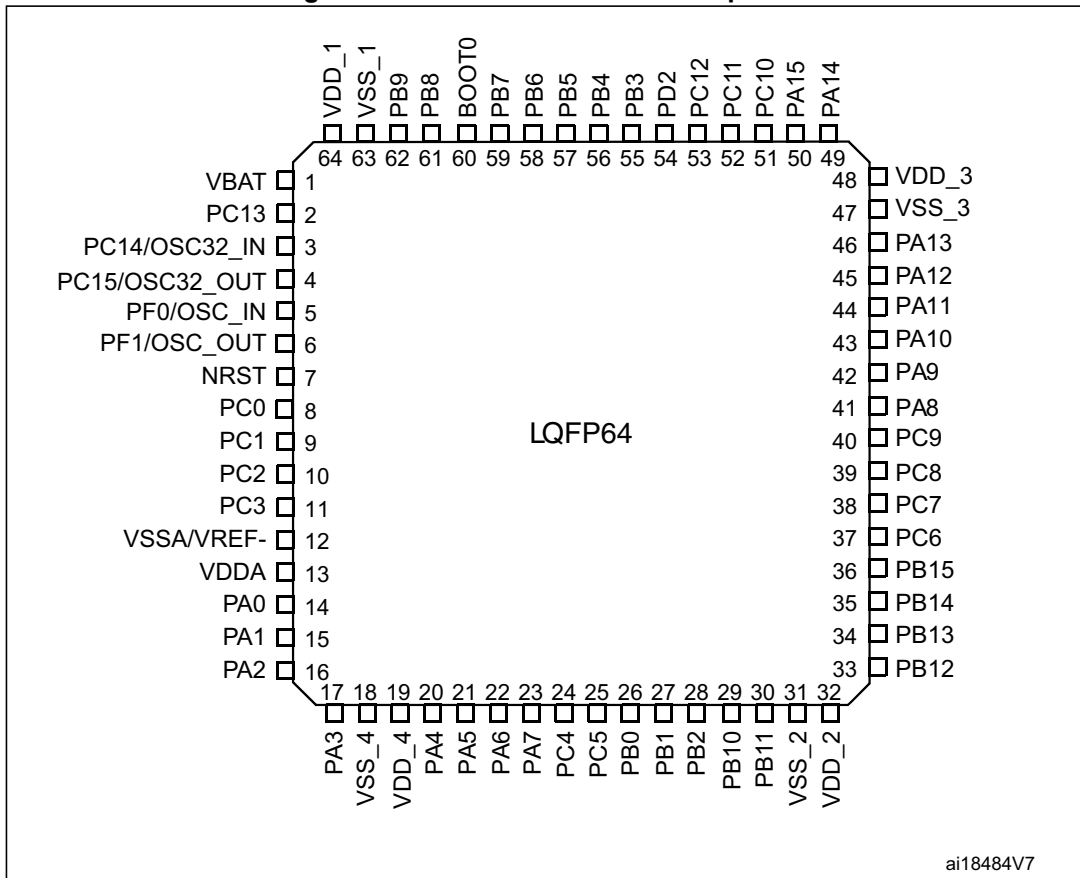


Figure 6. STM32F301x6/x8 LQFP64 pinout



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Figure 7. STM32F301x6/x8 WLCSP49 ballout

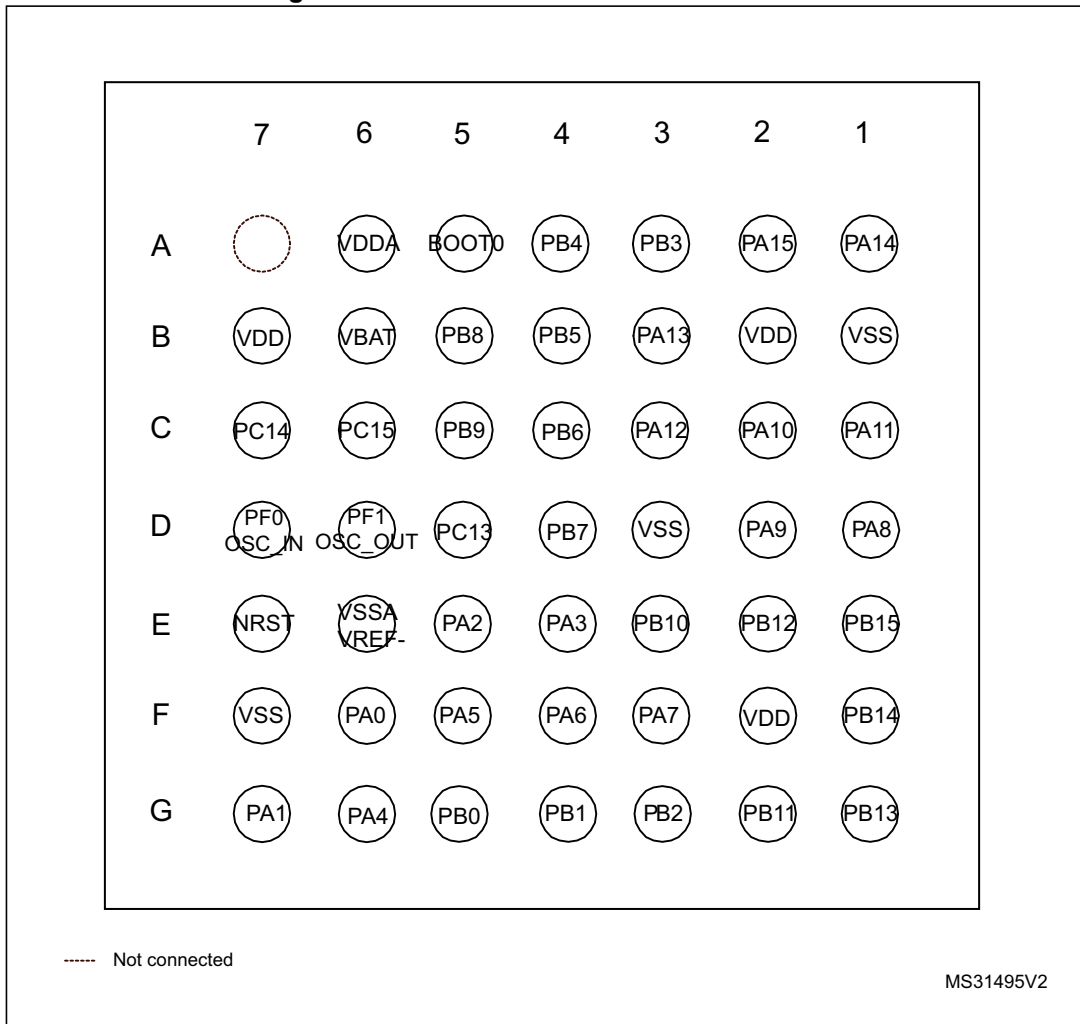


Table 11. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, I2C FM+ option
	TTa	3.3 V tolerant I/O
	TT	3.3 V tolerant I/O
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers



Table 12. STM32F301x6/x8 pin definitions

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	B6	1	1	VBAT	S	-		Backup power supply	
-D	5	2	2	PC13 <sup>(1)</sup> TAMPER1 WKUP2 (PC13)	I/O	TC	(1)	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
-C	7	3	3	PC14 <sup>(1)</sup> OSC32_IN (PC14)	I/O	TC	(1)		OSC32_IN
-C	6	4	4	PC15 <sup>(1)</sup> OSC32_OUT (PC14)	I/O	TC	(1)		OSC32_OUT
2	D7	5	5	PF0 OSC_IN (PF0)	I/O	FTf		I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N	OSC_IN
3	D6	6	6	PF1 OSC_OUT (PF1)	O	FTf		I2C2_SCL, SPI2_SCK/I2S2_CK	OSC_OUT
4	E7	7	7	NRST	I/O	RST		Device reset input/internal reset output (active low)	
-	-	-	8	PC0	I/O	TTa		EVENTOUT, TIM1_CH1	ADC1_IN6
-	-	-	9	PC1	I/O	TTa		EVENTOUT, TIM1_CH2	ADC1_IN7
-	-	-	10	PC2	I/O	TTa		EVENTOUT, TIM1_CH3	ADC1_IN8
-	-	-	11	PC3	I/O	TTa		EVENTOUT, TIM1_CH4, TIM1_BKIN2	ADC1_IN9
6	B7	8	12	VSSA/VREF-	S	-		Analog ground/Negative reference voltage	
5	A6	9	13	VDDA/VREF+	S	-		Analog power supply/Positive reference voltage	



Table 12. STM32F301x6/x8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
7	F6	10	14	PA0 -TAMPER2-WKUP1	I/O	TTa		TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, EVENTOUT	ADC1_IN1, RTC_TAMP2, WKUP1
8	G7	11	15	PA1	I/O	TTa		RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS, TIM15_CH1N, EVENTOUT	ADC1_IN2
9	E5	12	16	PA2	I/O	TTa		TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3, COMP2_INM
10	E4	13	17	PA3	I/O	TTa		TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4
-	-	-	18	VSS	S	-			
-	-	-	19	VDD	S	-			
11	G6	14	20	PA4	I/O	TTa		TSC_G2_IO1, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN5, DAC1_OUT1, COMP2_INM, COMP4_INM, COMP6_INM
12	F5	15	21	PA5	I/O	TTa		TIM2_CH1/TIM2_ETR, TSC_G2_IO2, EVENTOUT	OPAMP2_VINM
13	F4	16	22	PA6	I/O	TTa		TIM16_CH1, TSC_G2_IO3, TIM1_BKIN, EVENTOUT	ADC1_IN10, OPAMP2_VOUT
14	F3	17	23	PA7	I/O	TTa		TIM17_CH1, TSC_G2_IO4, TIM1_CH1N, EVENTOUT	ADC1_IN15, COMP2_INP, OPAMP2_VINP

**Table 12. STM32F301x6/x8 pin definitions (continued)**

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	24	PC4	I/O	TT		EVENTOUT, TIM1_ETR, USART1_TX	
-	-	-	25	PC5	I/O	TTa		EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	OPAMP2_VINM
15	G5	18	26	PB0	I/O	TTa		TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	G4	19	27	PB1	I/O	TTa		TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC1_IN12
-	G3	20	28	PB2	I/O	TTa		TSC_G3_IO4, EVENTOUT	COMP4_INM
-	E3	21	29	PB10	I/O	TT		TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	
-	G2	22	30	PB11	I/O	TTa		TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC1_IN14, COMP6_INP
16	D3	23	31	VSS	S	-		Digital ground	
17	F2	24	32	VDD	S	-		Digital power supply	
-	E2	25	33	PB12	I/O	TT		TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	
-	G1	26	34	PB13	I/O	TTa		TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC1_IN13



Table 12. STM32F301x6/x8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	F1	27	35	PB14	I/O	TTa		TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS, EVENTOUT	OPAMP2_VINP
-	E1	28	36	PB15	I/O	TTa		RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	COMP6_INM
-	-	-	37	PC6	I/O	FT		EVENTOUT, I2S2_MCK, COMP6_OUT	
-	-	-	38	PC7	I/O	FT		EVENTOUT, I2S3_MCK	
-	-	-	39	PC8	I/O	FT		EVENTOUT	
-	-	-	40	PC9	I/O	FTf		EVENTOUT, I2C3_SDA, I2SCKIN	
18	D1	29	41	PA8	I/O	FT		MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, EVENTOUT	
19	D2	30	42	PA9	I/O	FTf		I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT	

**Table 12. STM32F301x6/x8 pin definitions (continued)**

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
20	C2	31	43	PA10	I/O	FTf		TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, EVENTOUT	
21	C1	32	44	PA11	I/O	FT		SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, TIM1_CH4, TIM1_BKIN2, EVENTOUT	
22	C3	33	45	PA12	I/O	FT		TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS, COMP2_OUT, TIM1_ETR, EVENTOUT	
23	B3	34	46	PA13	I/O	FT		SWDIO, TIM16_CH1N, TSC_G4_IO3, IR-OUT, USART3_CTS, EVENTOUT	
-	B1	35	47	VSS_3	S	-		Digital ground	
-	B2	36	48	VDD_3	S	-		Digital power supply	
24	A1	37	49	PA14	I/O	FTf		SWCLK-JTCK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT	
25	A2	38	50	PA15	I/O	FTf		JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI3_NSS/I2S3_WS, USART2_RX, TIM1_BKIN, EVENTOUT	



Table 12. STM32F301x6/x8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	51	PC10	I/O	FT		EVENTOUT, SPI3_SCK/I2S3_CK, USART3_TX	
-	-	-	52	PC11	I/O	FT		EVENTOUT, SPI3_MISO/I2S3ext_SD, USART3_RX	
-	-	-	53	PC12	I/O	FT		EVENTOUT, SPI3_MOSI/I2S3_SD, USART3_CK	
-	-	-	54	PD2	I/O	FT		EVENTOUT	
26	A3	39	55	PB3	I/O	FT		JTDO-TRACESWO, TIM2_CH2, TSC_G5_IO1, SPI3_SCK/I2S3_CK, USART2_TX, EVENTOUT	
27	A4	40	56	PB4	I/O	FT		JTRST, TIM16_CH1, TSC_G5_IO2, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT	
28	B4	41	57	PB5	I/O	FT		TIM16_BKIN, I2C1_SMBAL, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT	
29	C4	42	58	PB6	I/O	FTf		TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, EVENTOUT	
30	D4	43	59	PB7	I/O	FTf		TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, EVENTOUT	

**Table 12. STM32F301x6/x8 pin definitions (continued)**

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
31	A5	44	60	BOOT0	I	B		Boot memory selection	
-	B5	45	61	PB8	I/O	FTf		TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, TIM1_BKIN, EVENTOUT	
-	C5	46	62	PB9	I/O	FTf		TIM17_CH1, I2C1_SDA, IR-OUT, USART3_TX, COMP2_OUT, EVENTOUT	
32	E6	47	63	VSS_1	S	-		Digital ground	
"1"	F7	48	64	VDD_1	S	-		Digital power supply	

- PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF
  - These GPIOs must not be used as current sources (e.g. to drive an LED).

After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0366 reference manual.



Table 13. Alternate functions for Port A

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16/TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/TIM16/TIM17	SPI2/I2S2/SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/I2S3/Infrared	USART1/USART2/USART3/GPCOMP6	I2C3/GPCOMP2/GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			
PA0		TIM2_C H1/TIM2_ETR		TSC_G 1_IO1				USART 2_CTS								EVENT OUT
PA1	RTC_REFIN	TIM2_C H2		TSC_G 1_IO2				USART 2_RTS		TIM15_CH1N						EVENT OUT
PA2		TIM2_C H3		TSC_G 1_IO3				USART 2_TX	COMP2_OUT	TIM15_CH1						EVENT OUT
PA3		TIM2_C H4		TSC_G 1_IO4				USART 2_RX		TIM15_CH2						EVENT OUT
PA4				TSC_G 2_IO1			SPI3_NSS/I2S3_WS	USART 2_CK								EVENT OUT
PA5		TIM2_C H1/TIM2_ETR		TSC_G 2_IO2												EVENT OUT
PA6		TIM16_CH1		TSC_G 2_IO3			TIM1_BKIN									EVENT OUT
PA7		TIM17_CH1		TSC_G 2_IO4			TIM1_CH1N									EVENT OUT
PA8	MCO			I2C3_SCL	I2C2_SMBAL	I2S2_MCK	TIM1_CH1	USART 1_CK								EVENT OUT



**Table 13. Alternate functions for Port A (continued)**

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16/TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/TIM16/TIM17	SPI2/I2S2/SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/Infrared	USART1/USART2/USART3/GPCOMP6	I2C3/GPCOMP2/GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			
PA9			I2C3_SMBAL	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX		TIM15_BKIN	TIM2_CH3					EVENT OUT
PA10		TIM17_BKIN		TSC_G4_IO2	I2C2_SDA	SPI2_MISO/I2S2ext_SD	TIM1_CH3	USART1_RX	COMP6_OUT		TIM2_CH4					EVENT OUT
PA11						SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS				TIM1_CH4	TIM1_BKIN2			EVENT OUT
PA12		TIM16_CH1				I2SCKIN	TIM1_CH2N	USART1_RTS	COMP2_OUT			TIM1_ETR				EVENT OUT
PA13	SWDATJTMS	TIM16_CH1N		TSC_G4_IO3		IR-OUT		USART3_CTS								EVENT OUT
PA14	SWCLKJTCK			TSC_G4_IO4	I2C1_SDA		TIM1_BKIN	USART2_TX								EVENT OUT
PA15	JTDI	TIM2_CH1/TIM2_ETR		TSC_SYNC	I2C1_SCL		SPI3_NSS/I2S3_WS	USART2_RX		TIM1_BKIN						EVENT OUT



Table 14. Alternate functions for Port B

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16/TIM17/EVENT	I2C3/TIM11/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/TIM16/TIM17	SPI2/I2S2/SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/Infrared	USART1/USART2/USART3/GPCOMP6	I2C3/GPCOMP2/GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			
PB0				TSC_G3_IO2			TIM1_C H2N									EVENT OUT
PB1				TSC_G3_IO3			TIM1_C H3N		COMP4_OUT							EVENT OUT
PB2				TSC_G3_IO4												EVENT OUT
PB3	JTDO-TRACE SWO	TIM2_C H2		TSC_G5_IO1			SPI3_S CK/I2S3_CK	USART 2_TX								EVENT OUT
PB4	JTRST	TIM16_CH1		TSC_G5_IO2			SPI3_MISO/I2S3_SD	USART 2_RX			TIM17_BKIN					EVENT OUT
PB5		TIM16_BKIN			I2C1_S MBAI		SPI3_MOSI/I2S3ext_SD	USART 2_CK	I2C3_S DA		TIM17_CH1					EVENT OUT
PB6		TIM16_CH1N		TSC_G5_IO3	I2C1_S CL			USART 1_TX								EVENT OUT
PB7		TIM17_CH1N		TSC_G5_IO4	I2C1_S DA			USART 1_RX								EVENT OUT
PB8		TIM16_CH1		TSC_S YNC	I2C1_S CL			USART 3_RX					TIM1_BKIN			EVENT OUT
PB9		TIM17_CH1			I2C1_S DA		IR-OUT	USART 3_TX	COMP2_OUT							EVENT OUT

Table 14. Alternate functions for Port B (continued)

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS_AF	TIM2/TIM15/TIM16/TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/TIM16/TIM17	SPI2/I2S2/SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/Infrared	USART1/USART2/USART3/GPCOMP6	I2C3/GPCOMP2/GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1				EVENT
PB10		TIM2_C H3		TSC_S YNC				USART 3_TX									EVENT OUT
PB11		TIM2_C H4		TSC_G 6_IO1				USART 3_RX									EVENT OUT
PB12				TSC_G 6_IO2	I2C2_S MBAL	SPI2_N SS/I2S2 _WS	TIM1_B KIN	USART 3_CK									EVENT OUT
PB13				TSC_G 6_IO3		SPI2_S CK/ I2S2_C K	TIM1_C H1N	USART 3_CTS									EVENT OUT
PB14		TIM15_ CH1		TSC_G 6_IO4		SPI2_MI SO/I2S2 ext_SD	TIM1_C H2N	USART 3_RTS									EVENT OUT
PB15	RTC_R EFIN	TIM15_ CH2	TIM15_ CH1N		TIM1_C H3N	SPI2_M OSI/ I2S2_S D											EVENT OUT



Table 15. Alternate functions for Port C

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2 /TIM15	I2C3/TIM15/ TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3 Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/ USART2/ USART3/ GPCOMP6
PC0		EVENTOUT	TIM1_CH1					
PC1		EVENTOUT	TIM1_CH2					
PC2		EVENTOUT	TIM1_CH3					
PC3		EVENTOUT	TIM1_CH4				TIM1_BKIN2	
PC4		EVENTOUT	TIM1_ETR					USART1_TX
PC5		EVENTOUT	TIM15_BKIN	TSC_G3_IO1				USART1_RX
PC6		EVENTOUT					I2S2_MCK	COMP6_OUT
PC7		EVENTOUT					I2S3_MCK	
PC8		EVENTOUT						
PC9		EVENTOUT		I2C3_SDA		I2SCKIN		
PC10		EVENTOUT					SPI3_SCK/ I2S3_CK	USART3_TX
PC11		EVENTOUT					SPI3_MISO/I2S3e xt_SD	USART3_RX
PC12		EVENTOUT					SPI3_MOSI/I2S3_ SD	USART3_CK
PC13					TIM1_CH1N			
PC14								
PC15								

**Table 16. Alternate functions for Port D**

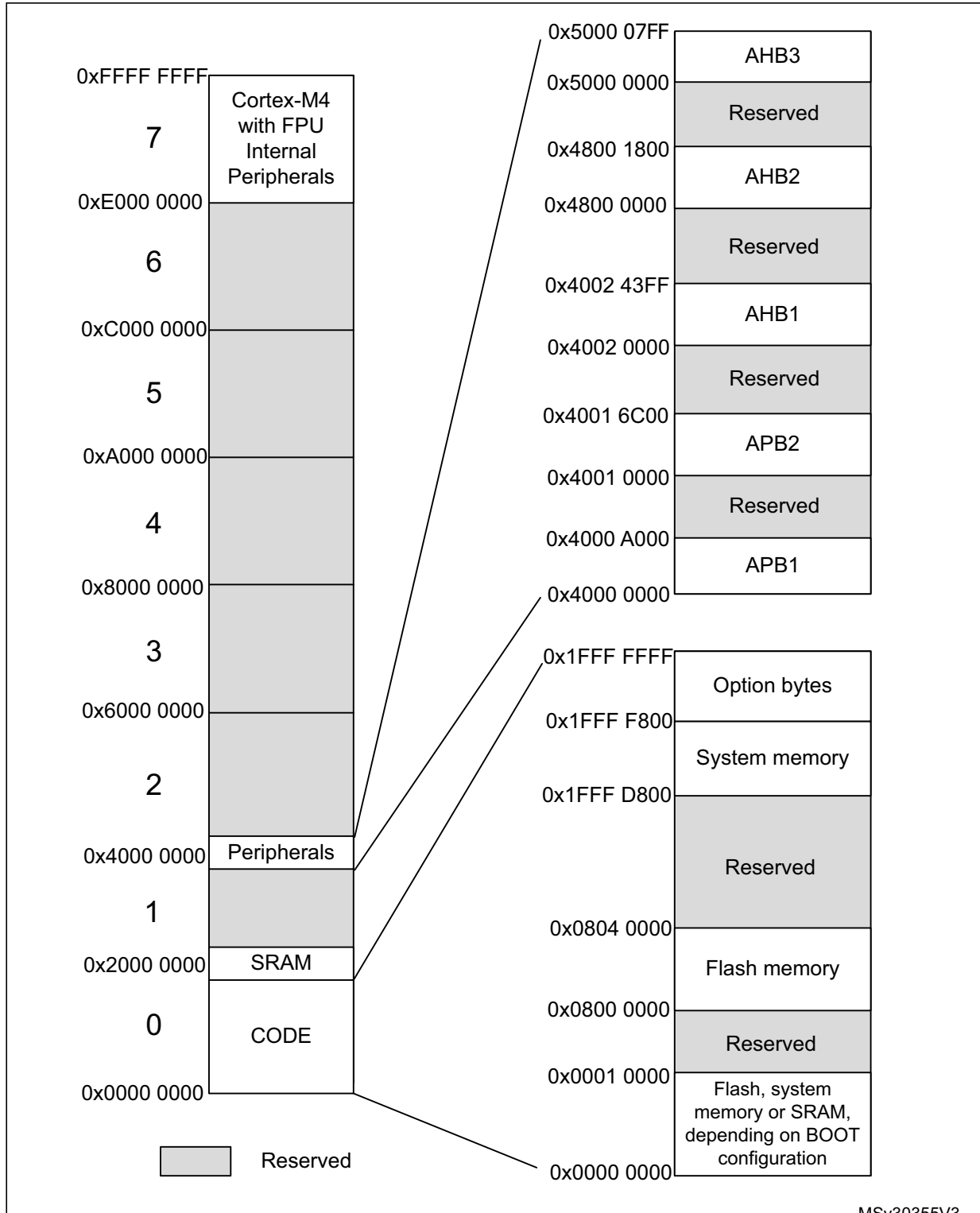
Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2/ TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/ Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/ USART2/ USART3/ GPCOMP6
PD2		EVENTOUT						

**Table 17. Alternate functions for Port F**

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2/ TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/ Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/USAR T2/USART3/ GPCOMP6
PF0					I2C2_SDA	SPI2_NSS/ I2S2_WS	TIM1_CH3N	
PF1					I2C2_SCL	SPI2_SCK/ I2S2_CK		

# 5 Memory mapping

Figure 8. STM32F301x6/x8 memory mapping



**Table 18. STM32F301x6/x8 peripheral register boundary addresses**

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0400 - 0x4002 0FFF	3 K	Reserved
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3000 - 0x4001 37FF	2 K	Reserved
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	8 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
	0x4000 9C00 - 0x4000 FFFF	25 K	Reserved

Table 18. STM32F301x6/x8 peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 7C00 - 0x4000 9BFF	8 K	Reserved
	0x4000 7800 - 0x4000 7BFF	1 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC1
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 5C00 - 0x4000 6FFF	5 K	Reserved
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 4C00 - 0x4000 53FF	2 K	Reserved
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1400 - 0x4000 27FF	5 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0400 - 0x4000 0FFF	3 K	Reserved
0x4000 0000 - 0x4000 03FF	1 K	TIM2	
	0x2000 4000 - 3FFF FFFF	~512 M	Reserved
	0x2000 0000 - 0x2000 3FFF	16 K	SRAM
	0x1FFF F800 - 0x1FFF FFFF	2 K	Option bytes
	0x1FFF D800 - 0x1FFF F7FF	8 K	System memory
	0x0801 0000 - 0x1FFF D7FF	~384 M	Reserved
	0x0800 0000 - 0x0800 FFFF	64 K	Main Flash memory
	0x0001 0000 - 0x07FF FFFF	~128 M	Reserved
	0x0000 000 - 0x0000 FFFF	64 K	Main Flash memory, system memory or SRAM depending on BOOT configuration



## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ }^\circ\text{C}$  and  $T_A = T_{A\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_{DDA} = 3.3\text{ V}$ . They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\sigma$ ).

#### 6.1.3 Typical curves

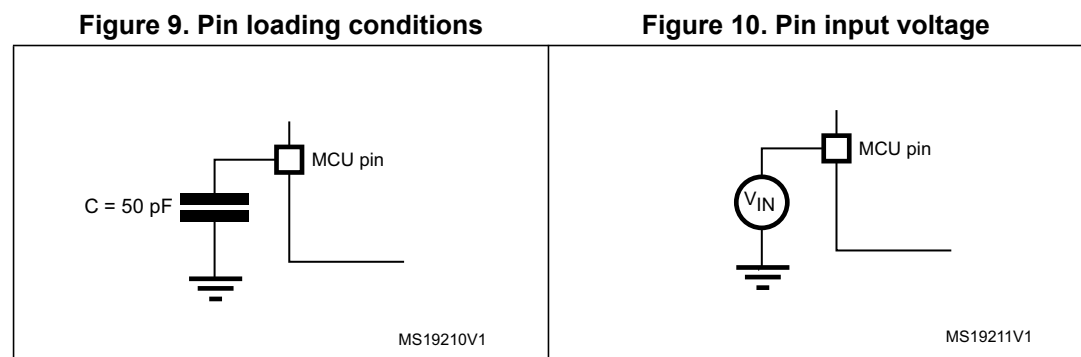
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

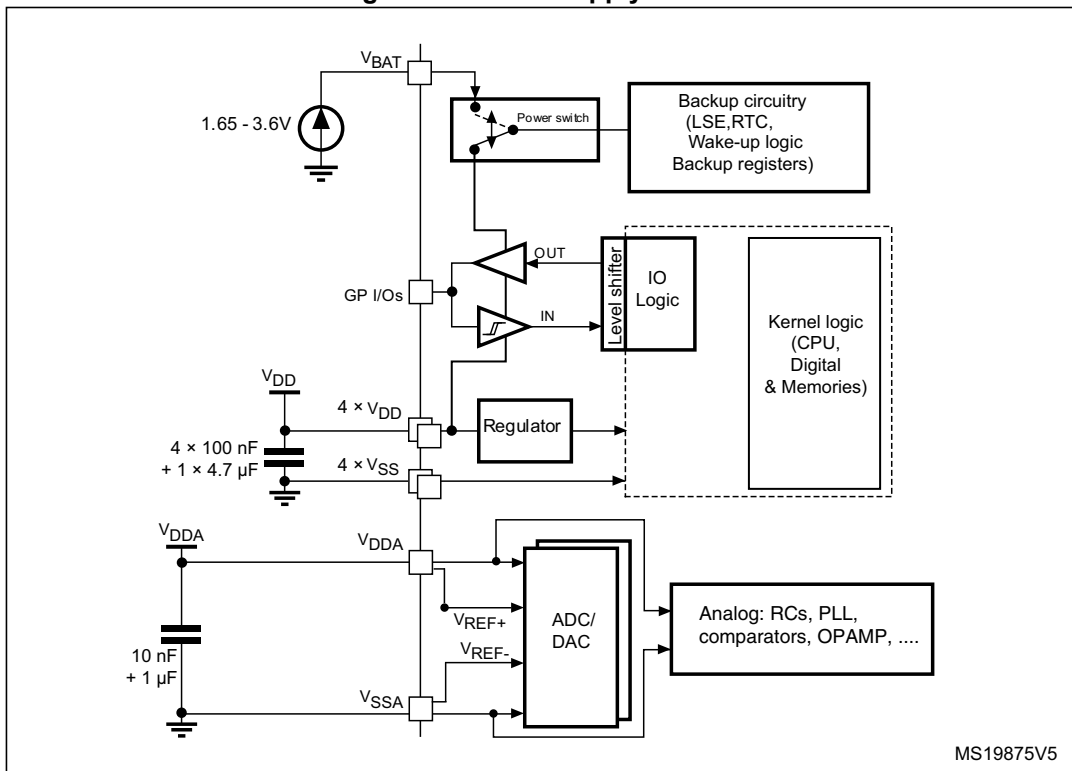
#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 10](#).



6.1.6 Power supply scheme

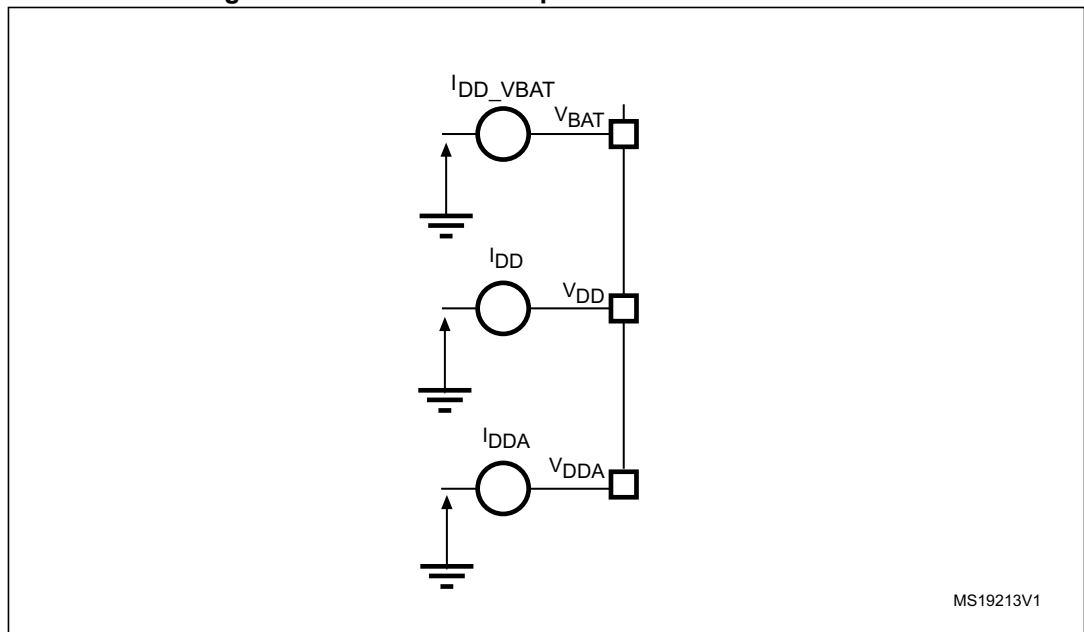
Figure 11. Power supply scheme



**Caution:** Each power supply pair (V<sub>DD</sub>/V<sub>SS</sub>, V<sub>DDA</sub>/V<sub>SSA</sub> etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### 6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 19: Voltage characteristics](#), [Table 20: Current characteristics](#), and [Table 21: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 19. Voltage characteristics<sup>(1)</sup>**

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including $V_{DDA}$ , $V_{BAT}$ and $V_{DD}$ )	-0.3	4.0	V
$V_{DD}-V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$ -		0.4	
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on TTa and TT pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section Electrical sensitivity characteristics</a>		V

- All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between  $V_{DDA}$  and  $V_{DD}$ :  
 $V_{DDA}$  must power on before or at the same time as  $V_{DD}$  in the power up sequence.  
 $V_{DDA}$  must be greater than or equal to  $V_{DD}$ .
- $V_{IN}$  maximum must always be respected. Refer to [Table 20: Current characteristics](#) for the maximum allowed injected current values.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
$\Sigma I_{VDD}$	Total current into sum of all VDD_x power lines (source)	130	mA
$\Sigma I_{VSS}$	Total current out of sum of all VSS_x ground lines (sink)	-130	
$I_{VDD}$	Maximum current into each VDD_x power line (source) <sup>(1)</sup>	100	
$I_{VSS}$	Maximum current out of each VSS_x ground line (sink) <sup>(1)</sup>	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins <sup>(2)</sup>	80	
	Total output current sourced by sum of all IOs and control pins <sup>(2)</sup>	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins <sup>(3)</sup>	-5/+0	
	Injected current on TC and RST pin <sup>(4)</sup>	+/-5	
	Injected current on TTa pins <sup>(5)</sup>	+/-5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) <sup>(6)</sup>	+/-25	

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$  and  $V_{SSA}$ ) pins must always be connected to the external power supply in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 19: Voltage characteristics](#) for the maximum allowed input voltage values.
5. A positive injection is induced by  $V_{IN} > V_{DDA}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer also to [Table Voltage characteristics](#) for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note <sup>(2)</sup> below [Table](#).
6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	150	°C

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency		0	72	MHz
$f_{PCLK1}$	Internal APB1 clock frequency		0	36	
$f_{PCLK2}$	Internal APB2 clock frequency		0	72	
$V_{DD}$	Standard operating voltage		2	3.6	V
$V_{DDA}$	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than $V_{DD}$	2	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
$V_{BAT}$	Backup operating voltage		1.65	3.6	V
$V_{IN}$	I/O input voltage	TC I/O	-0.3	$V_{DD}+0.3$	V
		TT I/O <sup>(1)</sup>	-0.3	3.6	
		TTa I/O	-0.3	$V_{DDA}+0.3$	
		FT and FTf I/O <sup>(1)</sup>	-0.3	5.5	
		BOOT0	0	5.5	
$P_D$	Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 <sup>(2)</sup>	LQFP64	-	444	mW
		LQFP48	-	364	
		WLCSP49	-	408	
		UFQFN32	-	540	
$T_A$	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation <sup>(3)</sup>	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation <sup>(3)</sup>	-40	125	
$T_J$	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. To sustain a voltage higher than  $V_{DD}+0.3\text{ V}$ , the internal pull-up/pull-down resistors must be disabled.
2. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$ . See [Table Package thermal characteristics](#).
3. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$ . See [Table 77: Package thermal characteristics](#)

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 23](#) are derived from tests performed under the ambient temperature condition summarized in [Table 22](#).

**Table 23. Operating conditions at power-up / power-down**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate		0	$\infty$	$\mu\text{s/V}$
	$V_{DD}$ fall time rate		20	$\infty$	
$t_{VDDA}$	$V_{DDA}$ rise time rate		0	$\infty$	
	$V_{DDA}$ fall time rate		20	$\infty$	

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 24](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 22](#).

**Table 24. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}^{(1)}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(2)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}^{(1)}$	PDR hysteresis		-	40	-	mV
$t_{RSTTEMPO}^{(3)}$	POR reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors  $V_{DD}$  and also  $V_{DDA}$  (if kept enabled in the option bytes). The POR detector monitors only  $V_{DD}$ .
2. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.
3. Based on characterization, not tested in production.

Table 25. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
V <sub>PVD0</sub>	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V <sub>PVD1</sub>	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V <sub>PVD2</sub>	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V <sub>PVD3</sub>	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V <sub>PVD4</sub>	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V <sub>PVD5</sub>	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V <sub>PVD6</sub>	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V <sub>PVD7</sub>	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
V <sub>PVDhyst</sub> <sup>(2)</sup>	PVD hysteresis		-	100	-	mV
IDD(PVD)	PVD current consumption		-	0.15	0.26	μA

1. Data based on characterization results only, not tested in production.

2. Guaranteed by design, not tested in production.



### 6.3.4 Embedded reference voltage

The parameters given in [Table 26](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 22](#).

**Table 26. Embedded internal reference voltage**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT}$	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.16	1.2	1.25	V
		$-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$	1.16	1.2	1.24 <sup>(1)</sup>	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage		2.2	-	-	$\mu\text{s}$
$V_{RERINT}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V} \pm 10\text{ mV}$	-	-	10 <sup>(2)</sup>	mV
$T_{Ccoeff}$	Temperature coefficient		-	-	100 <sup>(2)</sup>	ppm/ <sup>o</sup> C

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

**Table 27. Internal reference voltage calibration values**

Calibration value name	Description	Memory address
$V_{REFINT\_CAL}$	Raw data acquired at temperature of 30 °C $V_{DDA} \approx 3.3$	0x1FFF F7BA - 0x1FFF F7BB

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 12: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

**Typical and maximum current consumption**

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f<sub>HCLK</sub> frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled f<sub>PCLK2</sub> = f<sub>HCLK</sub> and f<sub>PCLK1</sub> = f<sub>HCLK</sub>/2
- When f<sub>HCLK</sub> > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in [Table 28](#) to [Table 34](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22](#).

**Table 28. Typical and maximum current consumption from VDD supply at VDD = 3.6V**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T <sub>A</sub> <sup>(1)</sup>			Typ	Max @ T <sub>A</sub> <sup>(1)</sup>			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I <sub>DD</sub>	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	45.7	48.6	50.0	52.0	25.5	27.5	28.1	28.8	mA
			64 MHz	40.6	43.6	44.5	46.4	22.7	24.6	25.2	25.9	
			48 MHz	30.8	33.6	34.1	35.5	17.3	19.0	19.5	20.0	
			32 MHz	21.0	22.9	23.5	25.6	11.7	13.2	13.7	14.1	
			24 MHz	16.0	16.8	18.0	18.9	9.0	10.4	10.8	11.4	
			8 MHz	5.4	5.6	6.1	7.2	3.3	3.3	3.8	4.2	
			1 MHz	1.1	1.2	1.7	2.7	0.8	0.9	1.3	1.6	
		Internal clock (HSI)	64 MHz	37.6	41.3	42.9	44.7	22.5	24.7	25.0	25.8	
			48 MHz	28.7	32.3	33.1	34.0	17.2	19.1	19.4	19.6	
			32 MHz	19.5	22.0	23.4	24.6	11.5	12.9	13.5	13.7	
			24 MHz	14.9	16.6	17.9	18.4	6.0	7.0	7.4	7.9	
			8 MHz	5.2	5.5	6.4	7.0	3.2	3.8	4.3	4.7	

Table 28. Typical and maximum current consumption from VDD supply at VDD = 3.6V (continued)

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T <sub>A</sub> <sup>(1)</sup>			Typ	Max @ T <sub>A</sub> <sup>(1)</sup>			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I <sub>DD</sub>	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	45.8	49.1 <sup>(2)</sup>	50.1	51.4 <sup>(2)</sup>	25.1	27.3 <sup>(2)</sup>	28.0	28.6 <sup>(2)</sup>	mA
			64 MHz	40.8	43.6	44.9	46.9	22.3	24.1	25.0	25.5	
			48 MHz	25.5	27.5	28.4	29.7	14.0	15.6	16.2	16.8	
			32 MHz	20.5	23.1	24.1	25.4	11.1	12.2	13.2	13.3	
			24 MHz	15.4	17.1	18.3	19.5	8.5	9.7	10.1	10.2	
			8 MHz	5.0	5.9	6.3	6.9	3.1	3.7	4.1	4.7	
		1 MHz	0.8	1.1	1.9	2.6	0.5	0.8	1.2	1.4		
		Internal clock (HSI)	64 MHz	37.3	41.1	41.8	43.3	22.0	23.8	24.4	24.9	
			48 MHz	28.0	31.1	31.6	33.2	16.4	18.0	18.3	18.6	
			32 MHz	18.8	21.3	22.1	23.1	10.9	11.9	12.8	13.1	
			24 MHz	14.2	15.9	16.8	17.9	5.5	6.4	6.7	7.3	
			8 MHz	4.8	5.1	6.0	6.5	2.9	3.5	4.1	4.2	
	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	30.0	32.8 <sup>(2)</sup>	33.1	34.1 <sup>(2)</sup>	5.9	6.8 <sup>(2)</sup>	6.9	7.4 <sup>(2)</sup>	
			64 MHz	26.7	29.2	29.6	30.5	5.3	5.9	6.2	6.7	
			48 MHz	16.7	18.5	19.0	19.7	3.6	4.5	4.5	5.3	
			32 MHz	13.3	14.9	15.3	15.4	2.9	3.7	3.8	4.3	
			24 MHz	10.2	11.4	12.0	12.3	2.2	2.7	2.9	3.2	
			8 MHz	3.6	4.4	4.8	5.3	0.9	1.2	1.5	2.1	
1 MHz			0.5	0.8	1.1	1.3	0.1	0.4	0.8	0.8		
I <sub>DD</sub>	Supply current in Sleep mode, executing from Flash or RAM	Internal clock (HSI)	64 MHz	23.2	25.3	25.6	26.2	5.0	5.7	6.1	6.2	
			48 MHz	17.5	19.2	19.4	19.9	3.9	4.7	4.8	5.3	
			32 MHz	11.7	12.9	13.2	13.3	2.6	3.4	3.6	4.2	
			24 MHz	8.9	10.2	10.6	10.8	1.4	2.1	2.4	2.7	
			8 MHz	3.4	4.0	4.6	5.1	0.7	1.1	1.4	1.9	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

**Table 29. Typical and maximum current consumption from the V<sub>DDA</sub> supply**

Symbol	Parameter	Conditions (1)	f <sub>HCLK</sub>	V <sub>DDA</sub> = 2.4 V				V <sub>DDA</sub> = 3.6 V				Unit
				Typ	Max @ T <sub>A</sub> (2)			Typ	Max @ T <sub>A</sub> (2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I <sub>DDA</sub>	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	72 MHz	231	254 <sup>(3)</sup>	266	271 <sup>(3)</sup>	251	274 <sup>(3)</sup>	294	300 <sup>(3)</sup>	µA
			64 MHz	203	226	239	243	222	245	261	266	
			48 MHz	153	174	182	186	165	185	198	203	
			32 MHz	105	124	131	133	114	132	141	143	
			24 MHz	82	98	104	105	89	106	111	113	
			8 MHz	3.1	4.1	4.1	5.1	3.6	4.7	5.2	5.5	
		HSI clock	64 MHz	270	294	307	312	296	322	338	343	
			48 MHz	219	242	253	257	240	263	276	281	
			32 MHz	171	192	201	203	188	209	219	222	
			24 MHz	148	169	175	177	163	182	190	193	
			8 MHz	69	84	87	87	79	92	94	96	

1. Current consumption from the V<sub>DDA</sub> supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I<sub>DDA</sub> is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based on characterization results and tested in production.

**Table 30. Typical and maximum V<sub>DD</sub> consumption in Stop and Standby modes**

Symbol	Parameter	Conditions	Typ @V <sub>DD</sub> (V <sub>DD</sub> =V <sub>DDA</sub> )						Max <sup>(1)</sup>			Unit
			V <sub>0</sub>	V <sub>4</sub>	V <sub>7</sub>	3.0 V	3/3	3.6 V	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub>	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	16.92	17.09	17.16	17.27	17.39	17.50	35.50	359.1	564.5	µA
		Regulator in low-power mode, all oscillators OFF	5.29	5.46	5.55	5.70	5.73	5.95	30.30	267.1	407.4	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.93	1.11	1.19	1.31	1.41	-	-	-	
		LSI OFF and IWDG OFF	0.63	0.76	0.84	0.95	1.02	1.10	5.00	6.30	12.60	

1. Data based on characterization results, not tested in production unless otherwise specified.

**Table 31. Typical and maximum  $V_{DDA}$  consumption in Stop and Standby modes**

Symbol	Parameter	Conditions	Typ @ $V_{DD}$ ( $V_{DD} = V_{DDA}$ )						Max <sup>(1)</sup>			Unit	
			2/0	2/4	2/7	3.0 V	3/3	3/6	$T_A = 25^{\circ}\text{C}$	$T_A = 85^{\circ}\text{C}$	$T_A = 105^{\circ}\text{C}$		
$I_{DDA}$	Supply current in Stop mode	$V_{DDA}$ monitoring ON	Regulator in run/low-power mode, all oscillators OFF	1.70	1.83	1.95	2.08	2.22	2.37	3.40	5.30	5.5	$\mu\text{A}$
	Supply current in Standby mode		LSI ON and IWDG ON	2.08	2.25	2.41	2.59	2.79	3.01	-	-	-	
	Supply current in Standby mode	$V_{DDA}$ monitoring OFF	LSI OFF and IWDG OFF	1.59	1.72	1.83	1.96	2.10	2.25	2.80	2.90	3.60	
			Regulator in run/low-power mode, all oscillators OFF	0.99	1.01	1.04	1.09	1.14	1.21	-	-	-	
	Supply current in Standby mode	$V_{DDA}$ monitoring OFF	LSI ON and IWDG ON	1.36	1.43	1.50	1.60	1.72	1.85	-	-	-	
			LSI OFF and IWDG OFF	0.87	0.89	0.92	0.97	1.02	1.09	-	-	-	

1. Data based on characterization results, not tested in production.

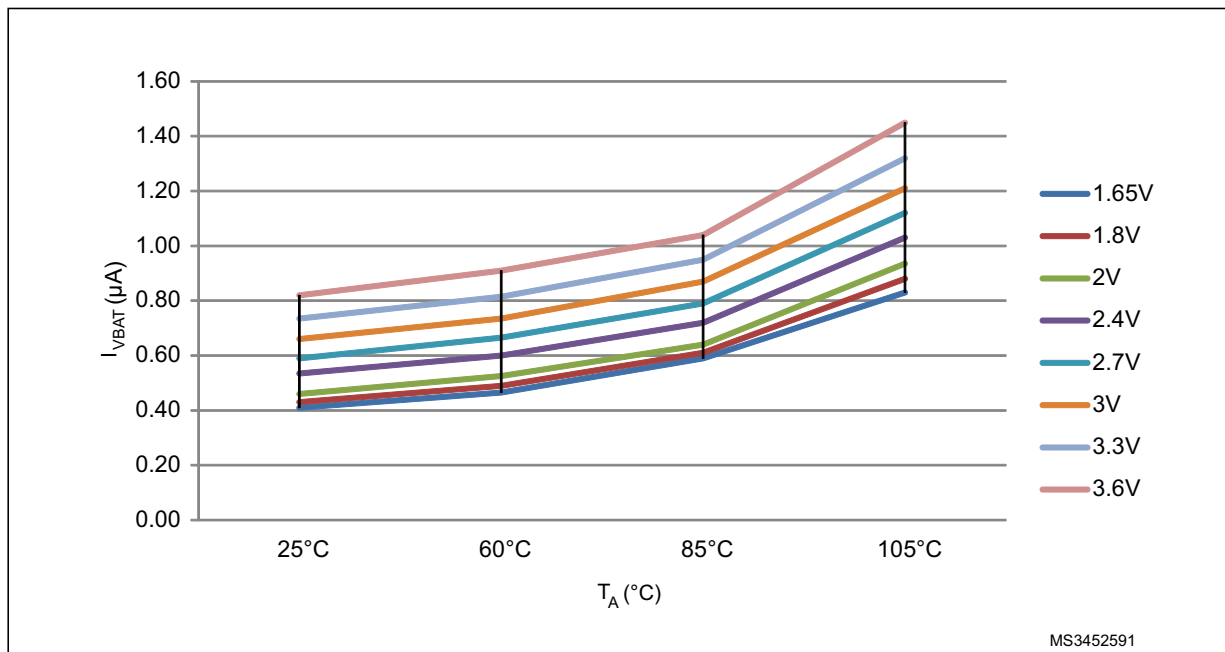
**Table 32. Typical and maximum current consumption from  $V_{BAT}$  supply**

Symbol	Parameter	Conditions <sup>(1)</sup>	Typ.@ $V_{BAT}$								Max. @ $V_{BAT} = 3.6\text{V}^{(2)}$ $T_A$ ( $^{\circ}\text{C}$ )			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	25	85	105	
$I_{DD\_VBAT}$	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.41	0.43	0.46	0.54	0.59	0.66	0.74	0.82	-	-	-	$\mu\text{A}$
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.65	0.68	0.73	0.80	0.87	0.95	1.03	1.14	-	-	-	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.

2. Data based on characterization results, not tested in production.

Figure 13. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



### Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3\text{ V}$
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled,  $f_{APB1} = f_{AHB}/2$ ,  $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

**Table 33. Typical current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I <sub>DD</sub>	Supply current in Run mode from V <sub>DD</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	44.8	24.9	mA
			64 MHz	40.0	22.4	
			48 MHz	30.3	17.1	
			32 MHz	20.7	11.9	
			24 MHz	15.8	9.2	
			16 MHz	10.9	6.5	
			8 MHz	5.7	3.55	
			4 MHz	3.43	3.22	
			2 MHz	2.18	1.53	
			1 MHz	1.56	1.19	
			500 kHz	1.25	0.96	
			125 kHz	0.96	0.84	
I <sub>DDA</sub> <sup>(1) (2)</sup>	Supply current in Run mode from V <sub>DDA</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	237.1		μA
			64 MHz	208.3		
			48 MHz	154.3		
			32 MHz	105.0		
			24 MHz	81.3		
			16 MHz	57.8		
			8 MHz	1.15		
			4 MHz	1.15		
			2 MHz	1.15		
			1 MHz	1.15		
			500 kHz	1.15		
			125 kHz	1.15		

1. V<sub>DDA</sub> monitoring is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

**Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I <sub>DD</sub>	Supply current in Sleep mode from V <sub>DD</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	28.7	6.1	mA
			64 MHz	25.6	5.5	
			48 MHz	19.3	4.26	
			32 MHz	13.1	3.04	
			24 MHz	10.0	2.42	
			16 MHz	6.8	1.81	
			8 MHz	3.54	0.98	
			4 MHz	2.35	0.88	
			2 MHz	1.64	0.80	
			1 MHz	1.28	0.77	
			500 kHz	1.11	0.75	
I <sub>DDA</sub> <sup>(1) (2)</sup>	Supply current in Sleep mode from V <sub>DDA</sub> supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	237.1		μA
			64 MHz	208.3		
			48 MHz	154.3		
			32 MHz	105.0		
			24 MHz	81.3		
			16 MHz	57.8		
			8 MHz	1.15		
			4 MHz	1.15		
			2 MHz	1.15		
			1 MHz	1.15		
			500 kHz	1.15		
125 kHz	1.15					

1. V<sub>DDA</sub> monitoring is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.



### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

#### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 52: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

#### I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 36: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$  is the MCU supply voltage

$f_{SW}$  is the I/O switching frequency

$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions <sup>(1)</sup>	I/O toggling frequency (f <sub>sw</sub> )	Typ	Unit
I <sub>sw</sub>	I/O current consumption	$V_{DD} = 3/3$ $C_{ext} = 0 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		$V_{DD} = 3/3$ $C_{ext} = 10 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		$V_{DD} = 3/3$ $C_{ext} = 22 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
			48 MHz	10.30	
		$V_{DD} = 3/3$ $C_{ext} = 33 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
			48 MHz	15.10	
$V_{DD} = 3/3$ $C_{ext} = 47 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20			
	4 MHz	1.54			
	8 MHz	2.46			
	18 MHz	4.51			
	36 MHz	10.30			
	48 MHz	18.50			

1. C<sub>S</sub> = 5 pF (estimated value).

**On-chip peripheral current consumption**

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and  $V_{DD} = V_{DDA} = 3.3\text{ V}$ .

Table 36. Peripheral current consumption

Peripheral	Typical consumption <sup>(1)</sup>	Unit
	I <sub>DD</sub>	
BusMatrix <sup>(2)</sup>	11.3	μA/MHz
DMA1	6.7	
CRC	2.0	
GPIOA	8.5	
GPIOB	8.3	
GPIOC	8.6	
GIOD	1.5	
GPIOF	1.0	
TSC	4.7	
ADC1	15.9	
APB2-Bridge <sup>(3)</sup>	2.7	
SYSCFG	3.2	
TIM1	27.6	
USART1	21.0	
TIM15	14.3	
TIM16	10.1	
TIM17	10.4	
APB1-Bridge <sup>(3)</sup>	5.8	
TIM2	40.7	
TIM6	7.4	
WWDG	4.6	
SPI2	35.2	
SPI3	34.2	
USART2	13.9	
USART3	13.1	
I2C1	9.4	
I2C2	9.4	
PWR	4.5	
DAC	8.3	
I2C3	10.5	

1. The power consumption of the analog part (I<sub>DDA</sub>) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU or DMA1).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

### 6.3.6 Wakeup time from low-power mode

The wakeup times given in [Table 37](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 22](#).

**Table 37. Low-power mode wakeup timings**

Symbol	Parameter	Conditions	Typ @V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DDA</sub>						Max	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t <sub>WUSTOP</sub>	Wakeup from Stop mode	Regulator in run mode	4.5	4.2	4.1	4.0	3.8	3.8	4.3	μs
		Regulator in low-power mode	8.2	7.0	6.4	6.0	5.7	5.5	8.7	
t <sub>WUSTANDBY</sub> <sup>(1)</sup>	Wakeup from Standby mode	LSI and IWDG OFF	72.8	63.4	59.2	56.1	53.1	51.3	103	
t <sub>WUSLEEP</sub>	Wakeup from Sleep mode		6-							CPU clock cycles

1. Data based on characterization results, not tested in production.

### 6.3.7 External clock source characteristics

#### High-speed external user clock generated from an external source

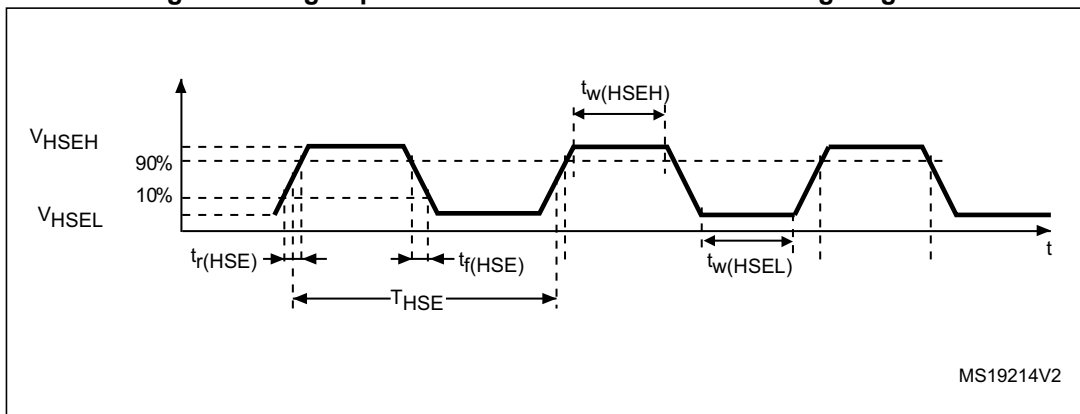
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 14](#).

**Table 38. High-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	User external clock source frequency <sup>(1)</sup>		1	8	32	MHz
$V_{HSEH}$	OSC_IN input pin high level voltage		$0.7V_{DD}$	-V	DD	V
$V_{HSEL}$	OSC_IN input pin low level voltage		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time <sup>(1)</sup>		15	-	-	ns
$t_r(HSE)$ $t_f(HSE)$	OSC_IN rise or fall time <sup>(1)</sup>		--		20	

1. Guaranteed by design, not tested in production.

**Figure 14. High-speed external clock source AC timing diagram**



MS19214V2

**Low-speed external user clock generated from an external source**

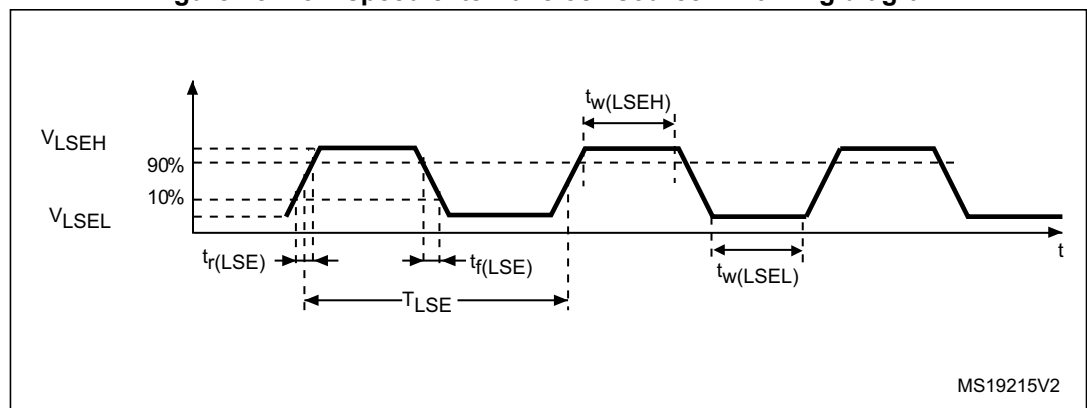
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 15](#)

**Table 39. Low-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User External clock source frequency <sup>(1)</sup>		-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-V	$V_{DD}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time <sup>(1)</sup>		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time <sup>(1)</sup>		--		50	

1. Guaranteed by design, not tested in production.

**Figure 15. Low-speed external clock source AC timing diagram**



MS19215V2

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. HSE oscillator characteristics**

Symbol	Parameter	Conditions <sup>(1)</sup>	Min <sup>(2)</sup>	Typ	Max <sup>(2)</sup>	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	8	32	MHz
$R_F$	Feedback resistor		-	200		k $\Omega$
$I_{DD}$	HSE current consumption	During startup <sup>(3)</sup>	-	-	8.5	mA
		$V_{DD}=3.3$ V, $R_m=30\Omega$ , $CL=10$ pF@8 MHz	-	0.4	-	
		$V_{DD}=3.3$ V, $R_m=45\Omega$ , $CL=10$ pF@8 MHz	-	0.5	-	
		$V_{DD}=3.3$ V, $R_m=30\Omega$ , $CL=10$ pF@32 MHz	-	0.8	-	
		$V_{DD}=3.3$ V, $R_m=30\Omega$ , $CL=10$ pF@32 MHz	-1		-	
		$V_{DD}=3.3$ V, $R_m=30\Omega$ , $CL=10$ pF@32 MHz	-	1.5	-	
$g_m$	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$ <sup>(4)</sup>	Startup time	$V_{DD}$ is stabilized	-	2	-	ms

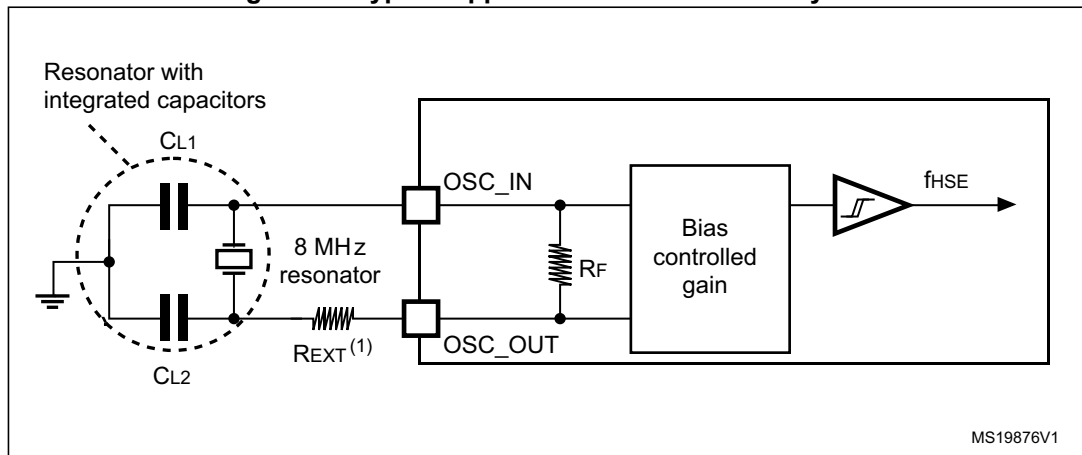
1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the  $t_{SU(HSE)}$  startup time.
4.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.



For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ .

*Note:* For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).

**Figure 16. Typical application with an 8 MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 41](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

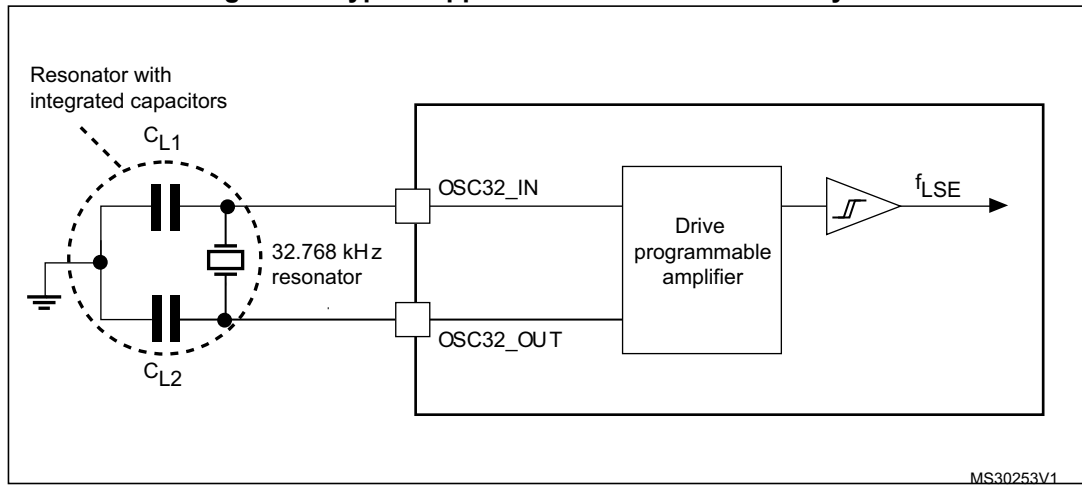
**Table 41. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz)**

Symbol	Parameter	Conditions <sup>(1)</sup>	Min <sup>(2)</sup>	Typ	Max <sup>(2)</sup>	Unit
$I_{DD}$	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	$\mu\text{A}$
		LSEDRV[1:0]=01 medium low driving capability	--	-	1	
		LSEDRV[1:0]=10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
$g_m$	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5-	-	-	$\mu\text{A/V}$
		LSEDRV[1:0]=01 medium low driving capability	8-	-	-	
		LSEDRV[1:0]=10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$ <sup>(3)</sup>	Startup time	$V_{DD}$ is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

Figure 17. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between  $OSC32\_IN$  and  $OSC32\_OUT$  and it is forbidden to add one.

### 6.3.8 Internal clock source characteristics

The parameters given in [Table 42](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22](#).

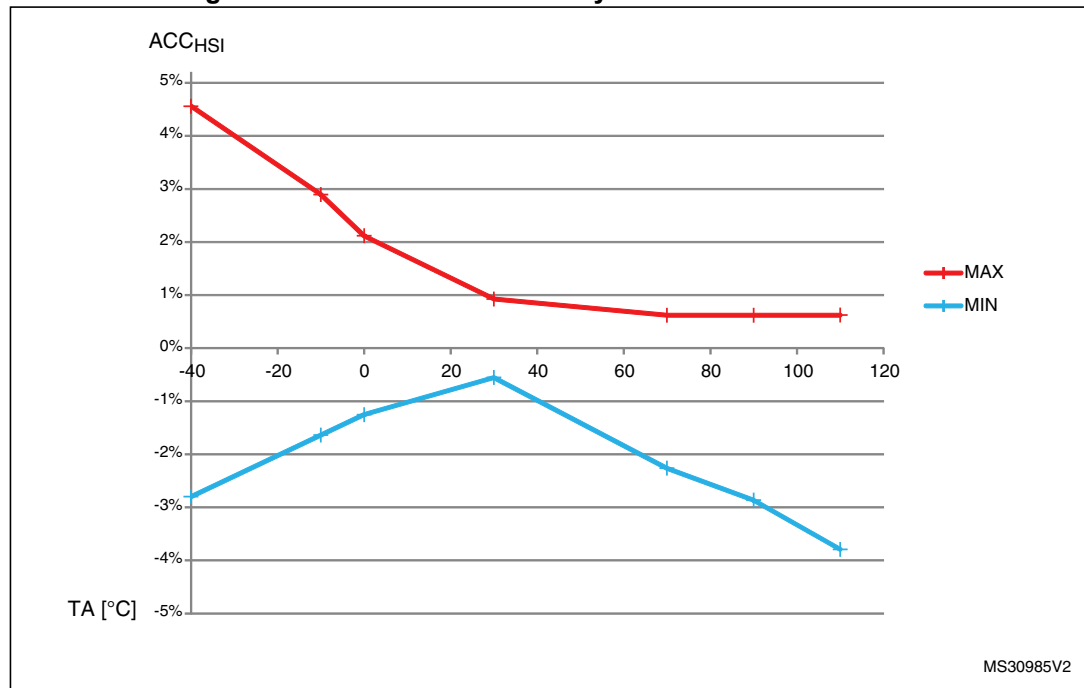
#### High-speed internal (HSI) RC oscillator

**Table 42. HSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>HSI</sub>	Frequency		-	8	-	MHz
TRIM	HSI user trimming step		-	-	1 <sup>(2)</sup>	%
DuCy <sub>(HSI)</sub>	Duty cycle		45 <sup>(2)</sup>	-5	5 <sup>(2)</sup>	%
ACC <sub>HSI</sub>	Accuracy of the HSI oscillator (factory calibrated)	T <sub>A</sub> ≈ C-40 to 105	-3.8 <sup>(3)</sup>	-	4.6 <sup>(3)</sup>	%
		T <sub>A</sub> ≈ C-10 to 85	-2.9 <sup>(3)</sup>	-	2.9 <sup>(3)</sup>	%
		T <sub>A</sub> ≈ 0 to 70 C	---			%
		T <sub>A</sub> ≈ C25	-1	-	1	%
t <sub>su(HSI)</sub>	HSI oscillator startup time		1 <sup>(2)</sup>	-2	(2)	μs
I <sub>DD(HSI)</sub>	HSI oscillator power consumption		-	80	100 <sup>(2)</sup>	μA

1. V<sub>DDA</sub> ≈ 3.3 T<sub>A</sub> = -40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

**Figure 18. HSI oscillator accuracy characterization results**



1. The above curves are based on characterisation results, not tested in production.

### Low-speed internal (LSI) RC oscillator

**Table 43. LSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}$	Frequency 30		40	50	kHz
$t_{su(LSI)}^{(2)}$	LSI oscillator startup time	-	-	85	$\mu$ s
$I_{DD(LSI)}^{(2)}$	LSI oscillator power consumption	-	0.75	1.2	$\mu$ A

1.  $V_{DDA} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

### 6.3.9 PLL characteristics

The parameters given in [Table 44](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22](#).

**Table 44. PLL characteristics**

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
$f_{PLL\_IN}$	PLL input clock <sup>(1)</sup>	1 <sup>(2)</sup>	-2	4 <sup>(2)</sup>	MHz
	PLL input clock duty cycle	40 <sup>(2)</sup>	-6	0 <sup>(2)</sup>	%
$f_{PLL\_OUT}$	PLL multiplier output clock	16 <sup>(2)</sup>	-	72	MHz
$t_{LOCK}$	PLL lock time	-	-	200 <sup>(2)</sup>	$\mu$ s
Jitter	Cycle-to-cycle jitter	-	-	300 <sup>(2)</sup>	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by  $f_{PLL\_OUT}$ .
2. Guaranteed by design, not tested in production.

### 6.3.10 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $105$  °C unless otherwise specified.

**Table 45. Flash memory characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max <sup>(1)</sup>	Unit
$t_{\text{prog}}$	16-bit programming time	$T_A = -40$ to $+105$ °C	20	-	40	µs
$t_{\text{ERASE}}$	Page (2 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
$t_{\text{ME}}$	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
$I_{\text{DD}}$	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

**Table 46. Flash memory endurance and data retention**

Symbol	Parameter	Conditions	Value	Unit
			Min <sup>(1)</sup>	
$N_{\text{END}}$	Endurance	$T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions)	10	kcycles
$t_{\text{RET}}$	Data retention	1 kcycle <sup>(2)</sup> at $T_A = 85$ °C	30	Years
		1 kcycle <sup>(2)</sup> at $T_A = 105$ °C	10	
		10 kcycles <sup>(2)</sup> at $T_A = 55$ °C	20	

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

### 6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 47](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 47. EMS characteristics**

Symbol	Parameter	Conditions	Level/Class
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , LQFP64, $T_A = +25^\circ\text{C}$ , $f_{HCLK} = 72\text{ MHz}$ conforms to IEC 61000-4-2	2B
$V_{EFTB}$	Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , LQFP64, $T_A = +25^\circ\text{C}$ , $f_{HCLK} = 72\text{ MHz}$ conforms to IEC 61000-4-4	4A

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 48. EMI characteristics**

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ]	Unit
				8/72 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.0V, T <sub>A</sub> = 25°C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	5	dBμV
			30 to 130 MHz	6	
			130 MHz to 1GHz	28	
			SAE EMI Level	4	-

**6.3.12 Electrical sensitivity characteristics**

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 49. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (human body model)	T <sub>A</sub> = +25 °C, conforming to JESD22-A114	2	2000	V
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (charge device model)	T <sub>A</sub> = +25 °C, conforming to ANSI/ESD STM5.3.1	II	250	

1. Data based on characterization results, not tested in production.



**Static latch-up**

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 50. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +105 °C conforming to JESD78A	2 level A

**6.3.13 I/O current injection characteristics**

As a general rule, current injection to the I/O pins, due to external voltage below V<sub>SS</sub> or above V<sub>DD</sub> (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

**Functional susceptibility to I/O current injection**

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in [Table 51](#)

**Table 51. I/O current injection susceptibility**

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I <sub>INJ</sub>	Injected current on BOOT0	-0	NA	mA
	Injected current on PC0 pin (TTa pin)	-0	+5	
	Injected current PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA6, PA7, PC4, PB0, PB10, PB11, PB13 with induced leakage current on other pins from this group less than -100 µA or more than +100 µA	-5	+5	
	Injected current on any other TT, FT and FTf pins	-5	NA	
	Injected current on all other TC, TTa and RESET pins	-5	+5	

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*



### 6.3.14 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 52](#) are derived from tests performed under the conditions summarized in [Table 22](#). All I/Os are CMOS and TTL compliant.

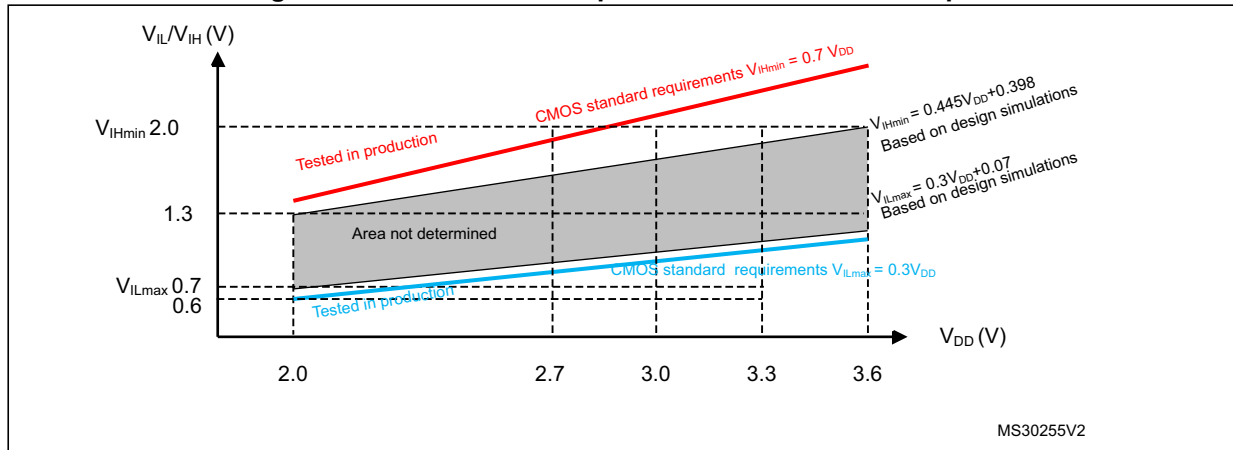
**Table 52. I/O static characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Low level input voltage	TTa and TT I/O	-	-	$0/3 V_{DD} + 0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475 V_{DD} - 0.2^{(1)}$	
		BOOT0 I/O	-	-	$0.3 V_{DD} - 0.3^{(1)}$	
		All I/Os except BOOT0	-	-	$0.3 V_{DD}^{(2)}$	
V <sub>IH</sub>	High level input voltage	TTa and TT I/O	$0.445 V_{DD} + 0.398^{(1)}$	--		V
		FT and FTf I/O	$0.5 V_{DD} + 0.2^{(1)}$	--		
		BOOT0	$0.2 V_{DD} + 0.95^{(1)}$	--		
		All I/Os except BOOT0	$0.7 V_{DD}^{(2)}$	--		
V <sub>hys</sub>	Schmitt trigger hysteresis	TC and TTa I/O	-	200 <sup>(1)</sup>	-	mV
		FT and FTf I/O	-	100 <sup>(1)</sup>	-	
		BOOT0	-	300 <sup>(1)</sup>	-	
I <sub>lkg</sub>	Input leakage current <sup>(3)</sup>	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 0.1$	$\mu A$
		TTa I/O in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	--		1	
		TTa I/O in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	$\pm 0.2$	
		FT and FTf I/O <sup>(4)</sup> $V_{DD} \leq V_{IN} \leq 5V$	--		10	
R <sub>PU</sub>	Weak pull-up equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{SS}$	25	40	55	k $\Omega$
R <sub>PD</sub>	Weak pull-down equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{DD}$	25	40	55	k $\Omega$
C <sub>IO</sub>	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation
2. Tested in production.
3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table I/O current injection susceptibility](#).
4. To sustain a voltage higher than  $V_{DD} + 0.3 V$ , the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 19* and *Figure 20* for standard I/Os.

**Figure 19. TC and TTa I/O input characteristics - CMOS port**



**Figure 20. TC and TTa I/O input characteristics - TTL port**

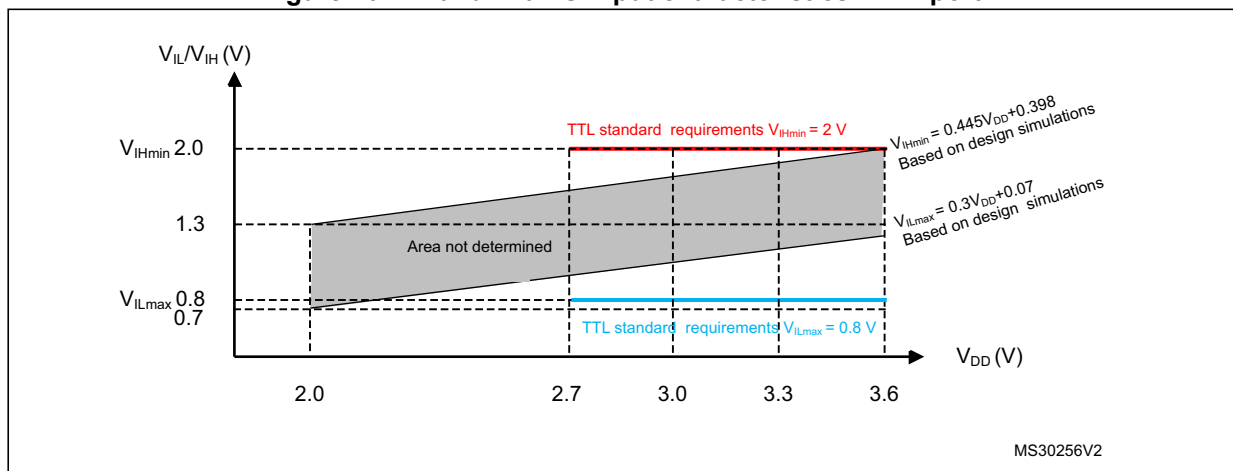


Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

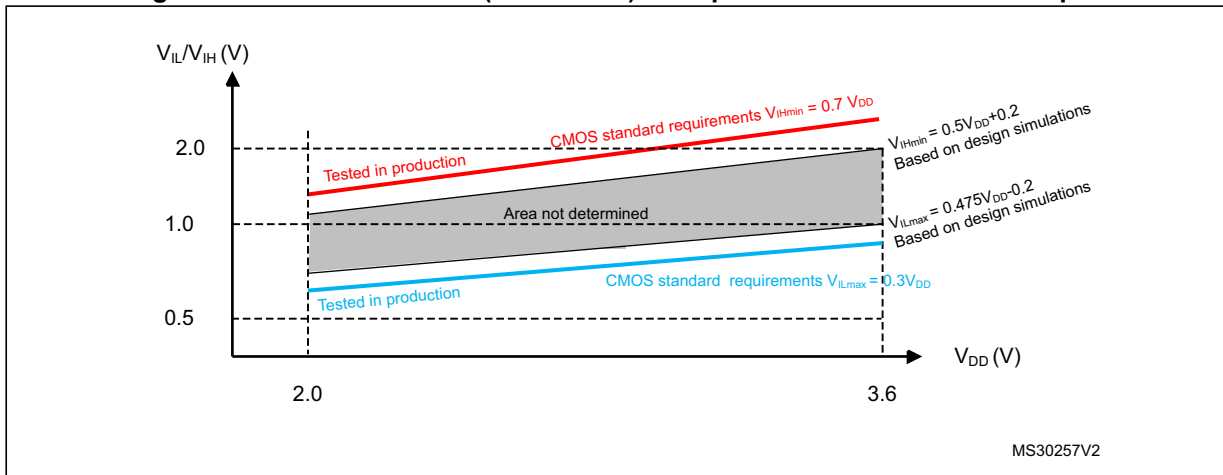
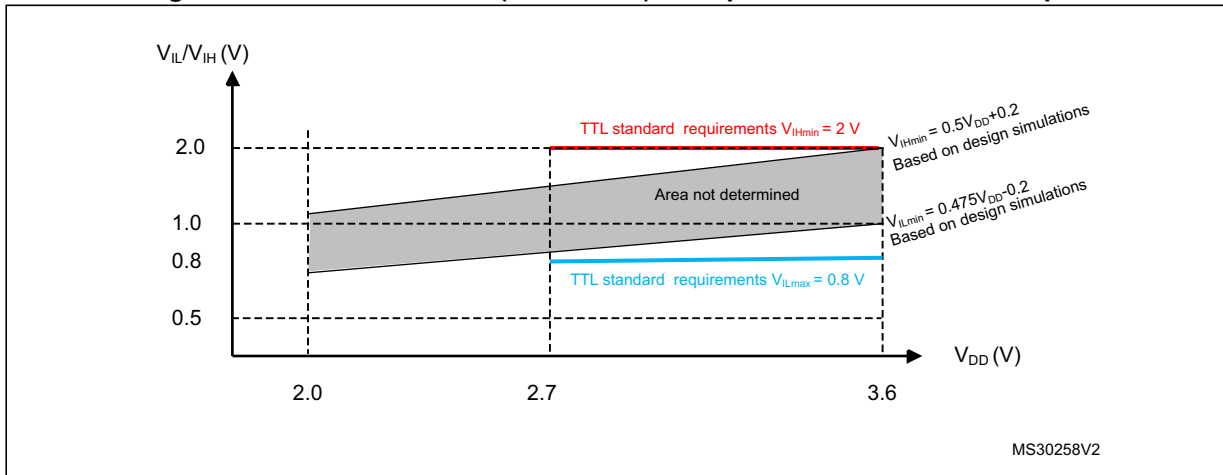


Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed  $V_{OL}/V_{OH}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table](#) ).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table](#) ).

### Output voltage levels

Unless otherwise specified, the parameters given in [Table 53](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 22](#). All I/Os (FT, TTA and TC unless otherwise specified) are CMOS and TTL compliant.

**Table 53. Output voltage characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port <sup>(2)</sup> $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} \leq 3.6$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port <sup>(2)</sup> $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} \leq 3.6$	-	0.4	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} \leq 3.6$	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OLFM+}^{(1)(4)}$	Output low level voltage for an FTf I/O pin in FM+ mode	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $\Sigma I_{IO(PIN)}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $\Sigma I_{IO(PIN)}$ .
4. Data based on design simulation.

**Input/output AC characteristics**

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 54*, respectively.

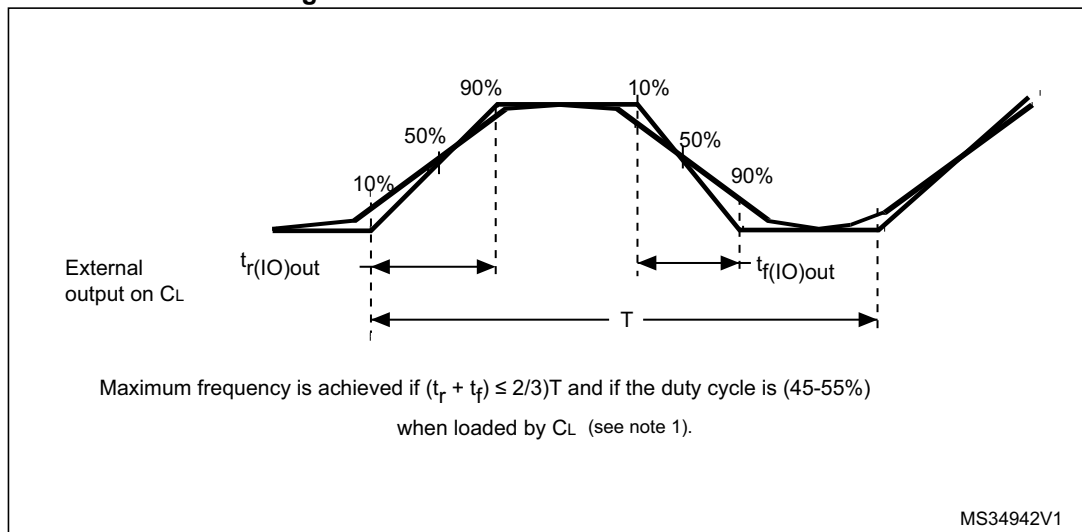
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in *Table 22*.

**Table 54. I/O AC characteristics<sup>(1)</sup>**

OSPEEDRy [1:0] value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 3.6$		$2^{(3)}$	MHz
	$t_{f(IO)out}$	Output high to low level fall time	$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 3.6$	-1	$25^{(3)}$	ns
	$t_{r(IO)out}$	Output low to high level rise time		-1	$25^{(3)}$	
01	$f_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 3.6$		$10^{(3)}$	MHz
	$t_{f(IO)out}$	Output high to low level fall time	$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 3.6$	-2	$5^{(3)}$	ns
	$t_{r(IO)out}$	Output low to high level rise time		-2	$5^{(3)}$	
11	$f_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 30 \text{ pF}, V_{DD} \approx 2.7 \text{ V to } 3.6$		$50^{(3)}$	MHz
			$C_L = 50 \text{ pF}, V_{DD} \approx 2.7 \text{ V to } 3.6$		$30^{(3)}$	MHz
			$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 2.7$		$20^{(3)}$	MHz
	$t_{f(IO)out}$	Output high to low level fall time	$C_L = 30 \text{ pF}, V_{DD} \approx 2.7 \text{ V to } 3.6$		$5^{(3)}$	ns
			$C_L = 50 \text{ pF}, V_{DD} \approx 2.7 \text{ V to } 3.6$		$8^{(3)}$	
			$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 2.7$		$12^{(3)}$	
	$t_{r(IO)out}$	Output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} \approx 2.7 \text{ V to } 3.6$		$5^{(3)}$	
			$C_L = 50 \text{ pF}, V_{DD} \approx 2.7 \text{ V to } 3.6$		$8^{(3)}$	
			$C_L = 50 \text{ pF}, V_{DD} \approx 2 \text{ V to } 2.7$		$12^{(3)}$	
FM+ configuration <sup>(4)</sup>	$f_{max(IO)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-2	$4^{(4)}$	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-1	$2^{(4)}$	ns
	$t_{r(IO)out}$	Output low to high level rise time		-3	$4^{(4)}$	

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0366 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 23*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F301x6/x8 reference manual RM0366 for a description of FM+ I/O mode configuration.

Figure 23. I/O AC characteristics definition



1. See [Table 54: I/O AC characteristics](#).

### 6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 52](#)).

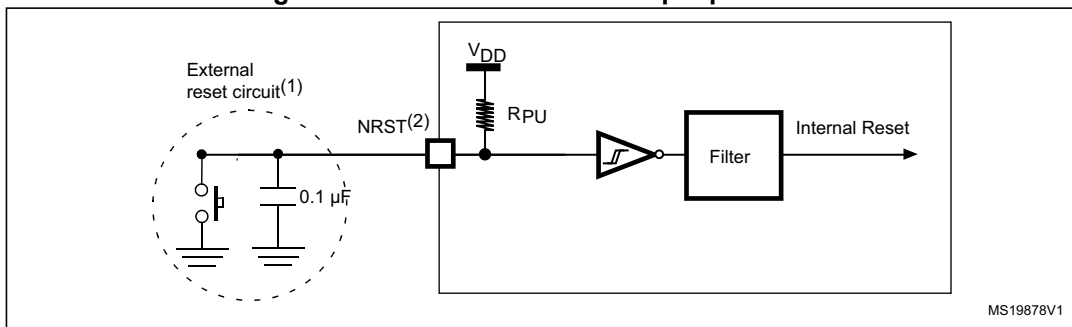
Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 22](#).

Table 55. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage		-	-	$0.3V_{DD} + 0.07^{(1)}$	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage		$0.445V_{DD} + 0.398^{(1)}$	--		
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
$R_{PU}$	Weak pull-up equivalent resistor <sup>(2)</sup>	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse		-	-	$100^{(1)}$	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse		$500^{(1)}$	--		ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 24. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table](#) . Otherwise the reset will not be taken into account by the device.

### 6.3.16 Timer characteristics

The parameters given in [Table 56](#) are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 56. TIMx<sup>(1)(2)</sup> characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1-		$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72\text{ MHz}$	13.9	-	ns
		$f_{TIMxCLK} = 144\text{ MHz}$ , $x = 1, 15, 16, 17$	6.95	-	ns
$f_{EXT}$	Timer external clock frequency on CH1 to CH4	0		$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 72\text{ MHz}$	0	36	MHz
Res <sub>TIM</sub>	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72\text{ MHz}$ (except TIM1/15/16/17)	0.0139	910	$\mu\text{s}$
		$f_{TIMxCLK} = 144\text{ MHz}$ , $x = 1/15/16/17$	0.0069	455	$\mu\text{s}$
$t_{MAX\_COUNT}$	Maximum possible count with 32-bit counter		-	$65536 \times 65536$	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72\text{ MHz}$	-	59.65	s
		$f_{TIMxCLK} = 144\text{ MHz}$ , $x = 1/15/16/17$	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.



Table 57. IWDG min/max timeout period at 40 kHz (LSI) <sup>(1)</sup>

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 58. WWDG min-max timeout value @72 MHz (PCLK)<sup>(1)</sup>

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687 3.6409	
2	1	0.1137 7.2817	
4	2	0.2275 14.564	
8	3	0.4551 29.127	

1. Guaranteed by design, not tested in production.

### 6.3.17 Communications interfaces

#### I<sup>2</sup>C interface characteristics

The I2C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 6.3.14: I/O port characteristics](#) for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics :

**Table 59. I2C analog filter characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{AF}$	Maximum pulse width of spikes that are suppressed by the analog filter	50 <sup>(2)</sup>	260 <sup>(3)</sup>	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below  $t_{AF(min)}$  are filtered.
3. Spikes with widths above  $t_{AF(max)}$  are not filtered

### SPI/I<sup>2</sup>S characteristics

Unless otherwise specified, the parameters given in [Table 60](#) for SPI or in [Table 61](#) for I<sup>2</sup>S are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 22](#).

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I<sup>2</sup>S).

**Table 60. SPI characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{SCK}$ $1/t_c(SCK)$	SPI clock frequency	Master mode	-	-	18	MHz
		Slave mode	-	-	18	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{pclk}$	--		ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{pclk}$	--		
$t_w(SCKH)$ $t_w(SCKL)$	SCK high and low time	Master mode, $f_{PCLK} = 36$ MHz, presc = 4	$T_{pclk} - 2$	$T_{pclk}$	$T_{pclk} + 2$	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	0	-	-	
		Slave mode	1	-	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	6.5	-	-	
		Slave mode	2.5	-	-	
$t_a(SO)$	Data output access time	Slave mode	8	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	14	
$t_v(SO)$ $t_v(MO)$	Data output valid time	Slave mode	-	12	27	
		Master mode	-	1.5	4	
$t_h(SO)$ $t_h(MO)$	Data output hold time	Slave mode	7.5	-	-	
		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.

Figure 25. SPI timing diagram - slave mode and CPHA = 0

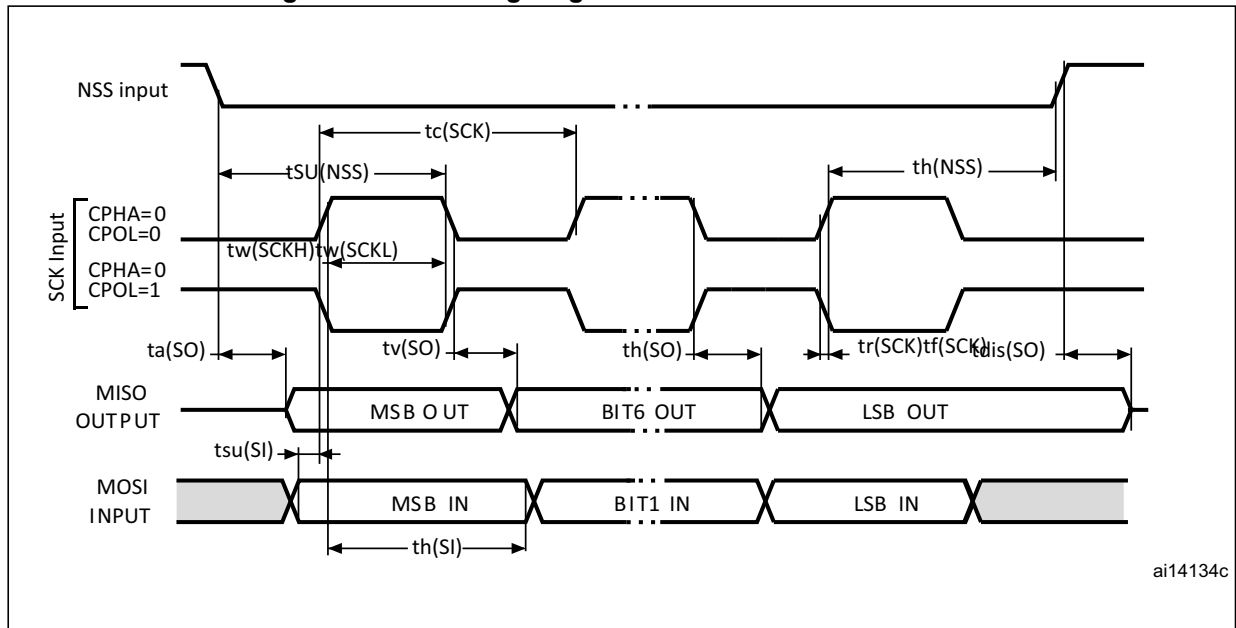
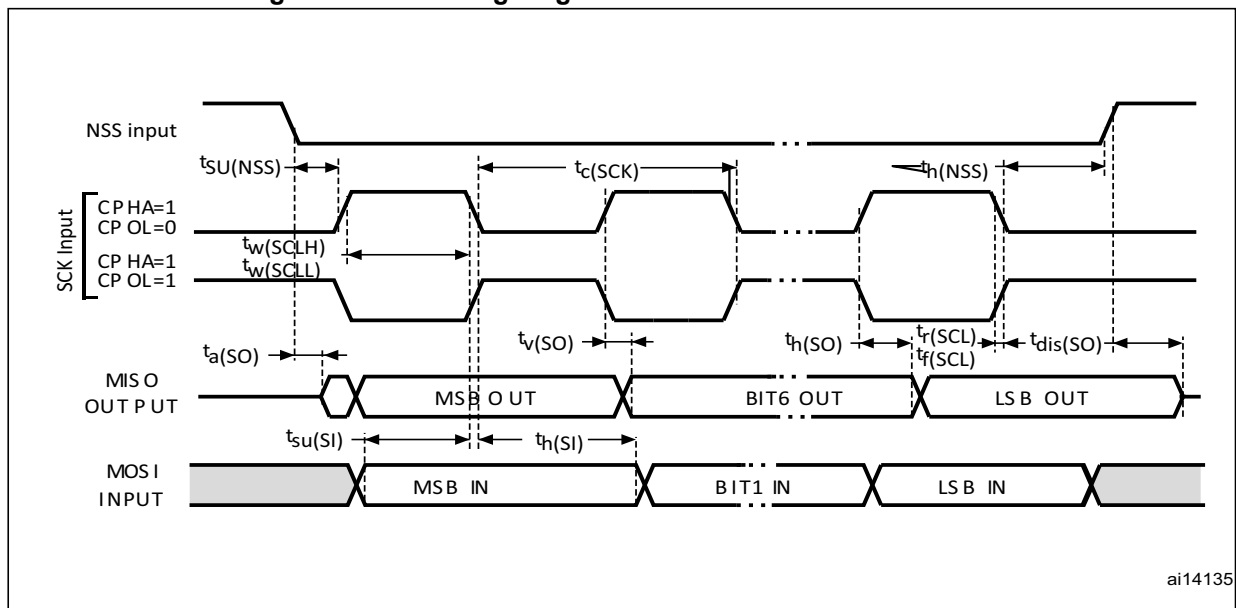
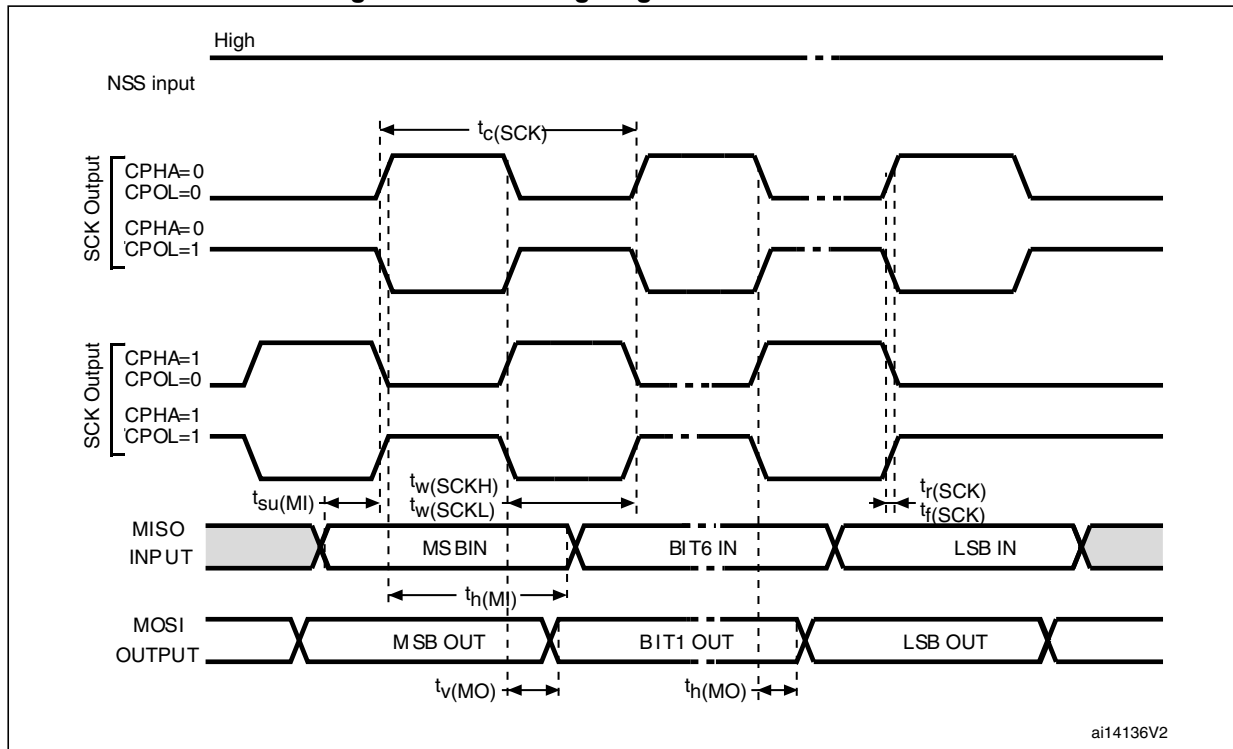


Figure 26. SPI timing diagram - slave mode and CPHA = 1<sup>(1)</sup>



1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30$  pF.

Figure 27. SPI timing diagram - master mode<sup>(1)</sup>



1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub> = 30 pF.

Table 61. I2S characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
f <sub>MCK</sub>	I2S Main clock output	-	256 x 8K	256xFs <sup>(2)</sup>	MHz
f <sub>CK</sub>	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D <sub>CK</sub>	I2S clock frequency duty cycle	Slave receiver	30	70	%

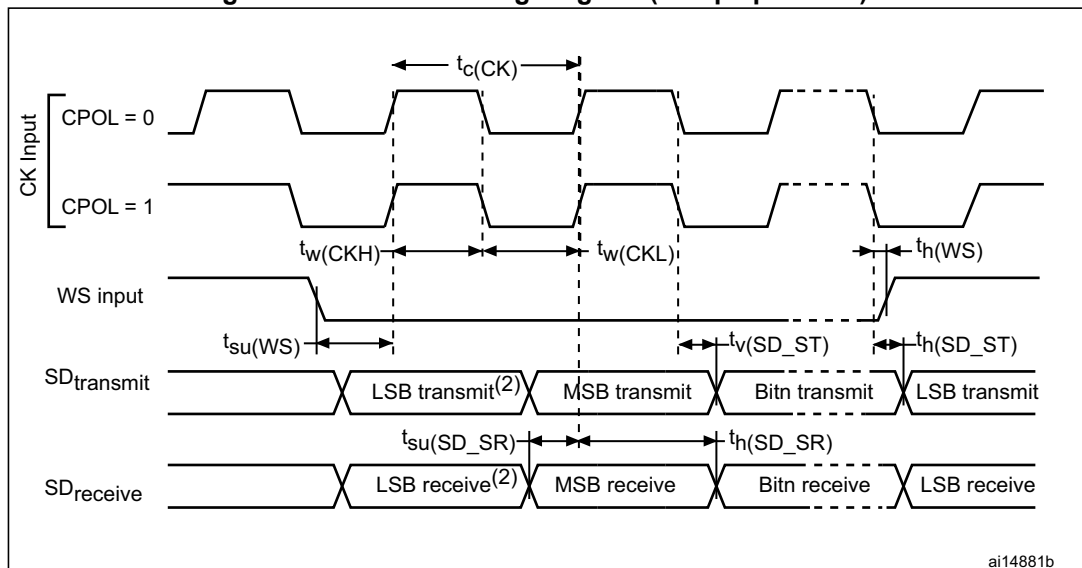
Table 61. I2S characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
t <sub>v(WS)</sub>	WS valid time	Master mode	-	20	ns
t <sub>h(WS)</sub>	WS hold time	Master mode	2	-	
t <sub>su(WS)</sub>	WS setup time	Slave mode	0	-	
t <sub>h(WS)</sub>	WS hold time	Slave mode	4	-	
t <sub>su(SD_MR)</sub>	Data input setup time	Master receiver	1	-	
t <sub>su(SD_SR)</sub>		Slave receiver	1	-	
t <sub>h(SD_MR)</sub>	Data input hold time	Master receiver	8	-	
t <sub>h(SD_SR)</sub>		Slave receiver	2.5	-	
t <sub>v(SD_ST)</sub>	Data output valid time	Slave transmitter (after enable edge)	-	50	
t <sub>v(SD_MT)</sub>		Master transmitter (after enable edge)	-2	2	
t <sub>h(SD_ST)</sub>	Data output hold time	Slave transmitter (after enable edge)	8	-	
t <sub>h(SD_MT)</sub>		Master transmitter (after enable edge)	1-		

1. Data based on characterization results, not tested in production.
2. 256x Fs maximum is 36 MHz (APB1 Maximum frequency)

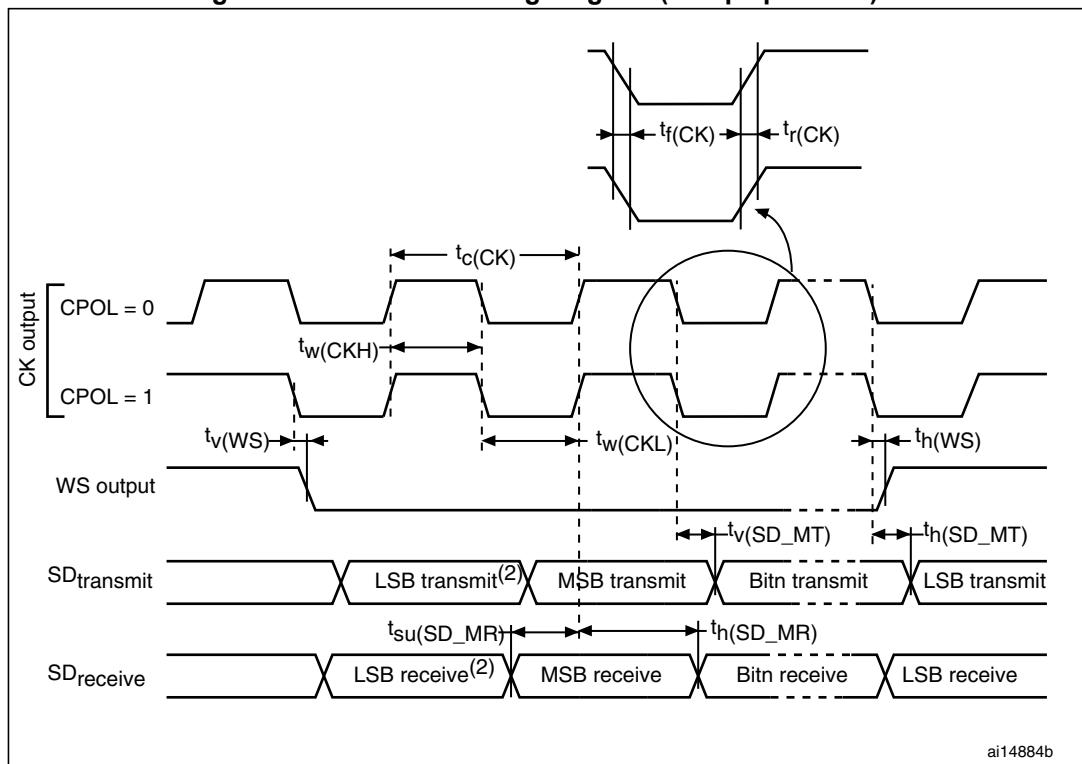
**Note:** Refer to RM0366 Reference Manual I2S Section for more details about the sampling frequency (Fs), fMCK, fCK, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of  $(I2SDIV)/(2*I2SDIV+ODD)$  and a max  $(I2SDIV+ODD)/(2*I2SDIV+ODD)$  and Fs max supported for each mode/condition.

Figure 28. I<sup>2</sup>S slave timing diagram (Philips protocol)<sup>(1)</sup>



1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub>=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 29. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>



1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub>=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### 6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in [Table 62](#) to [Table 64](#) are guaranteed by design, with conditions summarized in [Table 22](#).

**Table 62. ADC characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	Analog supply voltage for ADC		2	-	3.6	V
$I_{DDA}$	ADC current consumption	-	-	TBD	TBD	TBD
$f_{ADC}$	ADC clock frequency		0.14	-	72	MHz
$f_S^{(1)}$	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
$f_{TRIG}^{(1)}$	External trigger frequency	$f_{ADC} = 72$ MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
$V_{AIN}$	Conversion voltage range		0	-	$V_{DDA}$	V
$R_{AIN}^{(1)}$	External input impedance		-	-	100	k $\Omega$
$C_{ADC}^{(1)}$	Internal sample and hold capacitor		-5		-	pF
$t_{CAL}^{(1)}$	Calibration time	$f_{ADC} = 72$ MHz	1.56			$\mu$ s
			112			$1/f_{ADC}$
$t_{latr}^{(1)}$	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}^{(1)}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$
$t_S^{(1)}$	Sampling time	$f_{ADC} = 72$ MHz	0.021	-	8.35	$\mu$ s
			1.5	-	601.5	$1/f_{ADC}$
$TADCVREG\_STUP^{(1)}$	ADC Voltage Regulator Start-up time		--		10	$\mu$ s
$t_{CONV}^{(1)}$	Total conversion time (including sampling time)	$f_{ADC} = 72$ MHz Resolution = 12 bits	0.19	-	8.52	$\mu$ s
		Resolution = 12 bits	14 to 614 ( $t_S$ for sampling + 12.5 for successive approximation)			$1/f_{ADC}$



1. Data guaranteed by design.

**Table 63. Maximum ADC R<sub>AIN</sub> <sup>(1)</sup>**

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R <sub>AIN</sub> max (kΩ)		
			Fast channels <sup>(2)</sup>	Slow channels	Other channels <sup>(3)</sup>
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00

Table 63. Maximum ADC  $R_{AIN}$  <sup>(1)</sup> (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	$R_{AIN}$ max (k $\Omega$ )		
			Fast channels <sup>(2)</sup>	Slow channels	Other channels <sup>(3)</sup>
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channel on PA6.
3. Channel available on PA6.

Table 64. ADC accuracy - limited test conditions<sup>(1)(2)</sup>

Symbol	Parameter	Conditions		Min (3)	Typ	Max (3)	Unit	
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±4	±4.5	LSB
				Slow channel 4.8 Ms	-	±5.5	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
EO	Offset error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±2	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
EG	Gain error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±5	±5.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3.5	
ED	Differential linearity error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±2	±3	
			Differential	Fast channel 5.1 Ms	-	±1.5	±1.5	
				Slow channel 4.8 Ms	-	±1.5	±2	
ENOB <sup>(4)</sup>	Effective number of bits	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	10.8	10.8	-	bit
				Slow channel 4.8 Ms	10.8	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.2	11.3	-	
SINAD <sup>(4)</sup>	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 64. ADC accuracy - limited test conditions<sup>(1)(2)</sup> (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit		
SNR <sup>(4)</sup>	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	66	67	-	dB		
				Slow channel 4.8 Ms	66	67	-			
			Differential	Fast channel 5.1 Ms	69	70	-			
				Slow channel 4.8 Ms	69	70	-			
THD <sup>(4)</sup>	Total harmonic distortion		ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V <sub>DDA</sub> = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	-80		-80	dB
					Slow channel 4.8 Ms	-	-78		-77	
				Differential	Fast channel 5.1 Ms	-	-83		-82	
					Slow channel 4.8 Ms	-	-81		-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 3.10.1](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5dB Full Scale 50kHz sine wave input signal.

Table 65. ADC accuracy <sup>(1)(2)(3)</sup>

Symbol	Parameter	Conditions		Min <sup>(4)</sup>	Max <sup>(4)</sup>	Unit	
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps $2/0 \leq V_{DDA} \leq 3.6\text{ V}$	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB <sup>(5)</sup>	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD <sup>(5)</sup>	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	

**Table 65. ADC accuracy <sup>(1)(2)(3)</sup> (continued)**

Symbol	Parameter	Conditions		Min <sup>(4)</sup>	Max <sup>(4)</sup>	Unit		
SNR <sup>(5)</sup>	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5Msps, 2 V ≤ V <sub>DDA</sub> ≤ 3.6	Single ended	Fast channel 5.1 Ms	64	-	dB	
				Slow channel 4.8 Ms	64	-		
			Differential	Fast channel 5.1 Ms	67	-		
				Slow channel 4.8 Ms	67	-		
THD <sup>(5)</sup>	Total harmonic distortion		ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5Msps, 2 V ≤ V <sub>DDA</sub> ≤ 3.6	Single ended	Fast channel 5.1 Ms	-		-75
					Slow channel 4.8 Ms	-		-75
				Differential	Fast channel 5.1 Ms	-		-79
					Slow channel 4.8 Ms	-		-78

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 6.3.14](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V<sub>DDA</sub>, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5dB Full Scale 50kHz sine wave input signal.

**Table 66. ADC accuracy<sup>(1)(2)</sup>**

Symbol	Parameter	Test conditions	Typ	Max <sup>(3)</sup>	Unit	
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V <sub>DDA</sub> = V <sub>REF+</sub> ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 6.3.14: I/O port characteristics](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 30. ADC accuracy characteristics

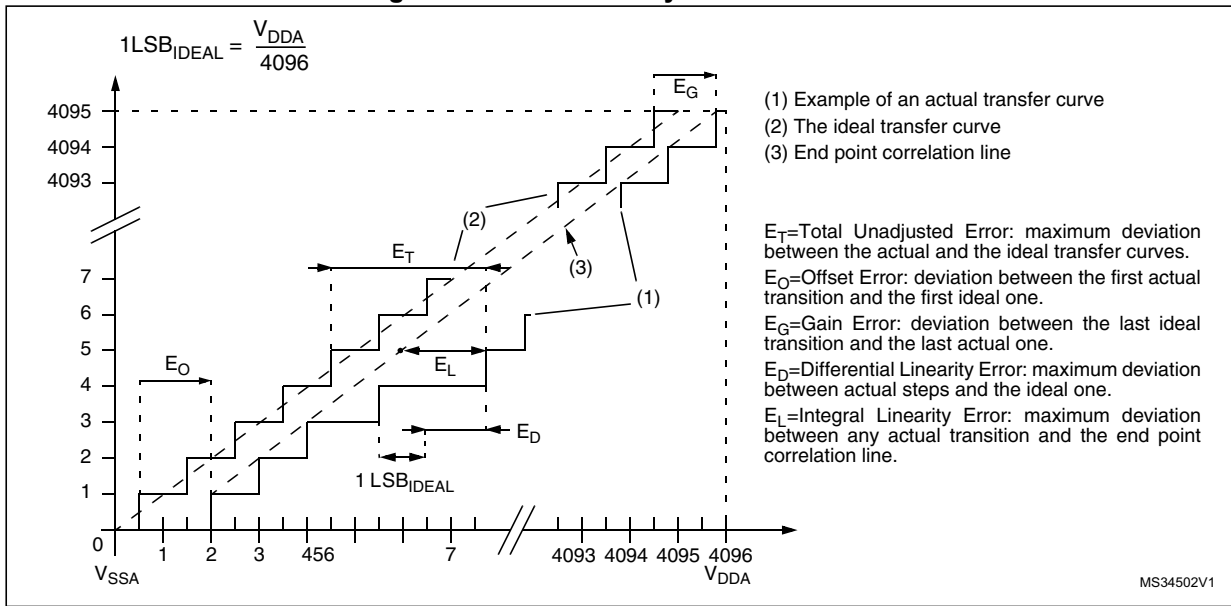
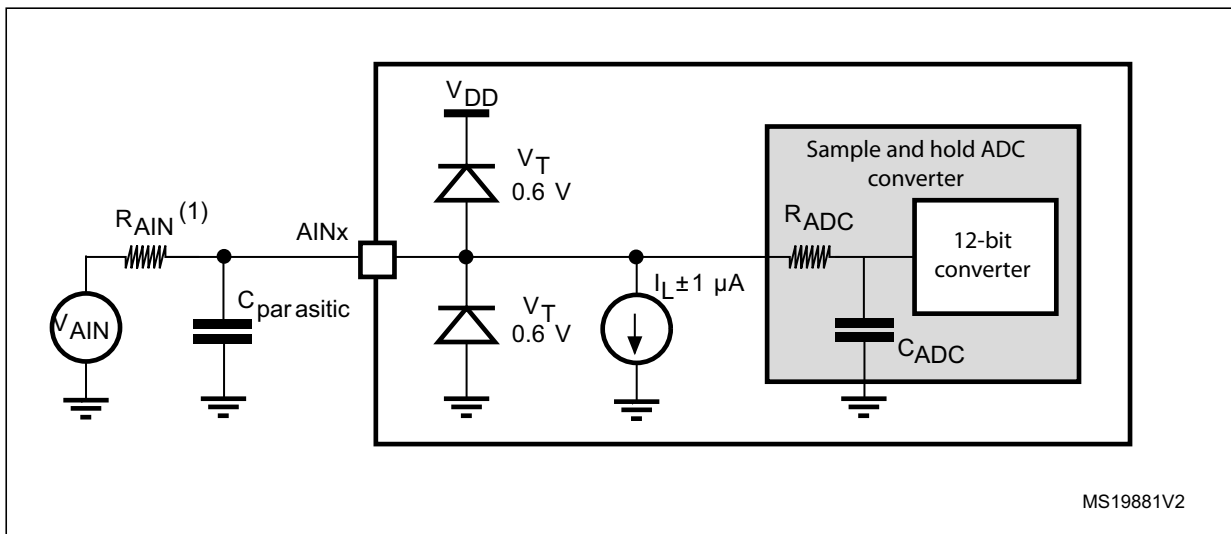


Figure 31. Typical connection diagram using the ADC



1. Refer to [Table](#) for the values of  $R_{\text{AIN}}$ .
2.  $C_{\text{parasitic}}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{\text{parasitic}}$  value will downgrade conversion accuracy. To remedy this,  $f_{\text{ADC}}$  should be reduced.

**General PCB design guidelines**

Power supply decoupling should be performed as shown in [Figure 11](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

## 6.3.19 DAC electrical specifications

Table 67. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	Analog supply voltage	DAC output buffer ON	2.4	-	3.6	V
$R_{LOAD}^{(1)}$	Resistive load	DAC output buffer ON	5	-	-	k $\Omega$
$R_O^{(1)}$	Output impedance	DAC output buffer ON	-	-	15	k $\Omega$
$C_{LOAD}^{(1)}$	Capacitive load	DAC output buffer ON	-	-	50	pF
$V_{DAC\_OUT}^{(1)}$	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA} = 3.6$ V and (0x155) and (0xEAB) at $V_{DDA} = 2.4$ V DAC output buffer ON.	0.2	-	$V_{DDA} - 0.2$	V
		DAC output buffer OFF	-	0.5	$V_{DDA} - 1LSB$	mV
$I_{DDA}^{(3)}$	DAC DC current consumption in quiescent mode (Standby mode) <sup>(2)</sup>	With no load, middle code (0x800) on the input.	-	-	380	$\mu$ A
		With no load, worst code (0xF1C) on the input.	-	-	480	$\mu$ A
$DNL^{(3)}$	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	$\pm 0.5$	LSB
		Given for a 12-bit input code	-	-	$\pm 2$	LSB
$INL^{(3)}$	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	$\pm 1$	LSB
		Given for a 12-bit input code	-	-	$\pm 4$	LSB
Offset <sup>(3)</sup>	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$ )	-	-	-	$\pm 10$	mV
		Given for a 10-bit input code at $V_{DDA} \neq 3.6$	-	-	$\pm 3$	LSB
		Given for a 12-bit input code at $V_{DDA} = 3.6$ V	-	-	$\pm 12$	LSB
Gain error <sup>(3)</sup>	Gain error	Given for a 12-bit input code	-	-	$\pm 0.5$	%
$t_{SETTLING}^{(3)}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1LSB$ )	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ $\Omega$	-3	-	4	$\mu$ s
Update rate <sup>(3)</sup>	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ $\Omega$	-	-	1	MS/s

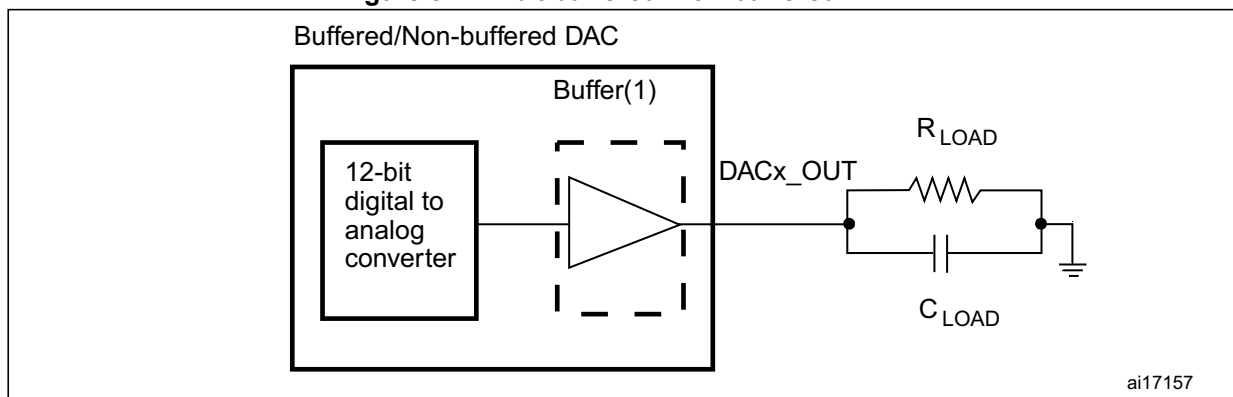


Table 67. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WAKEUP}^{(3)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50 \text{ pF}$ , $R_{LOAD} \geq 5 \text{ } \Omega$	-	6.5	10	$\mu\text{s}$
PSRR+ <sup>(1)</sup>	Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)	$C_{LOAD} = 50 \text{ pF}$ , No $R_{LOAD} \geq 5 \text{ } \Omega$ ,	-	-67	-40	dB

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 32. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

### 6.3.20 Comparator characteristics

Table 68. Comparator characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DDA}$	Analog supply voltage	-	2	-	3.6	V
$V_{IN}$	Comparator input voltage range	-0		-	$V_{DDA}$	
$V_{BG}$	Scaler input voltage	-	-	$V_{REFINIT}$	-	
$V_{SC}$	Scaler offset voltage	-	-	$\pm 5$	$\pm 10$	mV
$t_{S\_SC}$	Scaler startup time from power down	-	-	-	0.1	ms
$t_{START}$	Comparator startup time	$V_{DDA} \geq 2.7$		-	4	$\mu\text{s}$
		$V_{DDA} < 2.7 \text{ V}$	-	-	10	

Table 68. Comparator characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_D$	Propagation delay for 200 mV step with 100 mV overdrive	$V_{DDA} \geq 2.7 \text{ V}$	-	25	28	ns
		$V_{DDA} < 2.7 \text{ V}$	-	28	30	
	Propagation delay for full range step with 100 mV overdrive	$V_{DDA} \geq 2.7 \text{ V}$	-	32	35	
		$V_{DDA} < 2.7 \text{ V}$	-	35	40	
$V_{\text{OFFSET}}$	Comparator offset error	$V_{DDA} \geq 2.7 \text{ V}$	-	$\pm 5$	$\pm 10$	mV
		$V_{DDA} < 2.7 \text{ V}$	-	-	$\pm 25$	
$V_{\text{OFFSET}}$	Total offset variation	Full temperature range	-	-	3	mV
$I_{\text{DD(Comp)}}$	COMP current consumption	-	-	400	600	$\mu\text{A}$

1. Guaranteed by design, not tested in production.

## 6.3.21 Operational amplifier characteristics

Table 69. Operational amplifier characteristics<sup>(1)</sup>

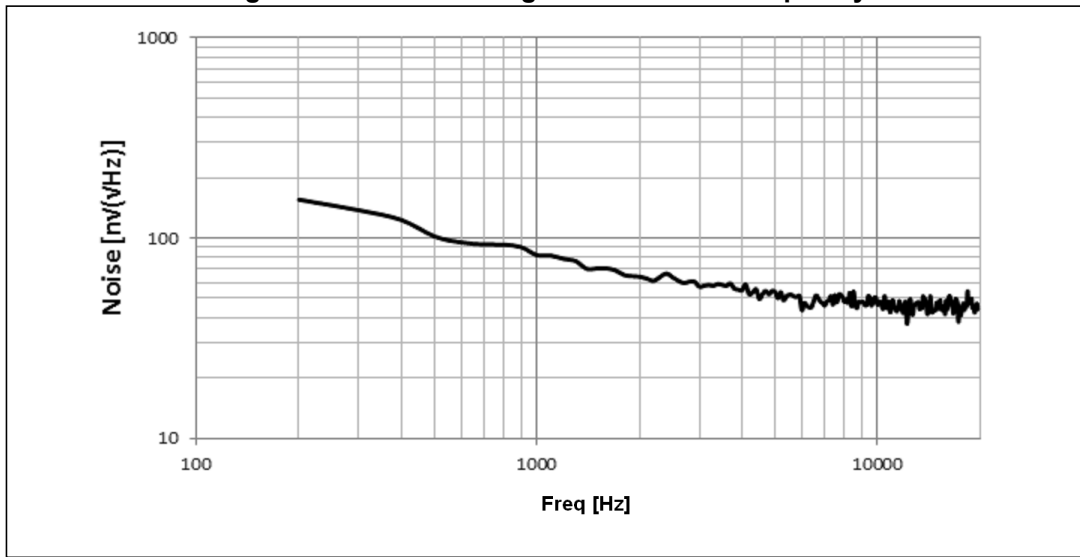
Symbol	Parameter		Condition	Min	Typ	Max	Unit
V <sub>DDA</sub>	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V <sub>DDA</sub>	V
V <sub>OFFSET</sub>	Input offset voltage	Maximum calibration range	25°C, No Load on output.	--		4	mV
			All voltage/Temp.	--		6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	--		3	
ΔV <sub>OFFSET</sub>	Input offset voltage drift		-	-	5	-	μV/°C
I <sub>LOAD</sub>	Drive current		-	-	-	500	μA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	μA
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/μs
R <sub>LOAD</sub>	Resistive load		-	4	-	-	kΩ
C <sub>LOAD</sub>	Capacitive load		-	-	-	50	pF
V <sub>OH</sub> SAT	High saturation voltage		R <sub>load</sub> = min, Input at V <sub>DDA</sub> .	-	-	100	mV
			R <sub>load</sub> = 20K, Input at V <sub>DDA</sub> .	--		20	
V <sub>OL</sub> SAT	Low saturation voltage		R <sub>load</sub> = min, input at 0V	-	-	100	
			R <sub>load</sub> = 20K, input at 0V.	--		20	
φ <sub>m</sub>	Phase margin		-	-	62	-	°
t <sub>OFFTRIM</sub>	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		--		-	2	ms
t <sub>WAKEUP</sub>	Wake up time from OFF state.		C <sub>LOAD</sub> ≤ 50 pf, R <sub>LOAD</sub> ≥ 4 kΩ, Follower configuration	-	2.8	5	μs
t <sub>S_OPAM_VOUT</sub>	ADC sampling time when reading the OPAMP output			400	-	-	ns

Table 69. Operational amplifier characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	
			-	4	-	
			-	8	-	
			-	16	-	
R <sub>network</sub>	R2/R1 internal resistance values in PGA mode <sup>(2)</sup>	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	
I <sub>bias</sub>	OPAMP input bias current	-	-	-	±0.2 <sup>(3)</sup>	μA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cloud = 50pF, Rload = 4 KΩ	-4		-	MHz
		PGA Gain = 4, Cloud = 50pF, Rload = 4 KΩ	-2		-	
		PGA Gain = 8, Cloud = 50pF, Rload = 4 KΩ	-1		-	
		PGA Gain = 16, Cloud = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-4	3	-	

1. Guaranteed by design, not tested in production.
2. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain = 1+R2/R1
3. Mostly TTA I/O leakage, when used in analog mode.

Figure 33. OPAMP Voltage Noise versus Frequency



### 6.3.22 Temperature sensor characteristics

Table 70. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature	-	$\pm 1$	$\pm 2$	$^{\circ}\text{C}$
Avg_Slope <sup>(1)</sup>	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}$	Voltage at 25 $^{\circ}\text{C}$	1.34	1.43	1.52	V
$t_{START}^{(1)}$	Startup time	4	-	10	$\mu\text{s}$
$T_{S\_temp}^{(1)(2)}$	ADC sampling time when reading the temperature	2.2	-	-	$\mu\text{s}$

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 71. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$ , $V_{DDA} \approx 3.3$	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$ $V_{DDA} \approx 3.3$	0x1FFF F7C2 - 0x1FFF F7C3

### 6.3.23 V BAT monitoring characteristics

Table 72.  $V_{BAT}$  monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for $V_{BAT}$	-	50	-	K $\Omega$
Q	Ratio on $V_{BAT}$ measurement	-	2	-	
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S\_vbat}^{(1)(2)}$	ADC sampling time when reading the $V_{BAT}$ 1mV accuracy	2.2	-	-	$\mu\text{s}$

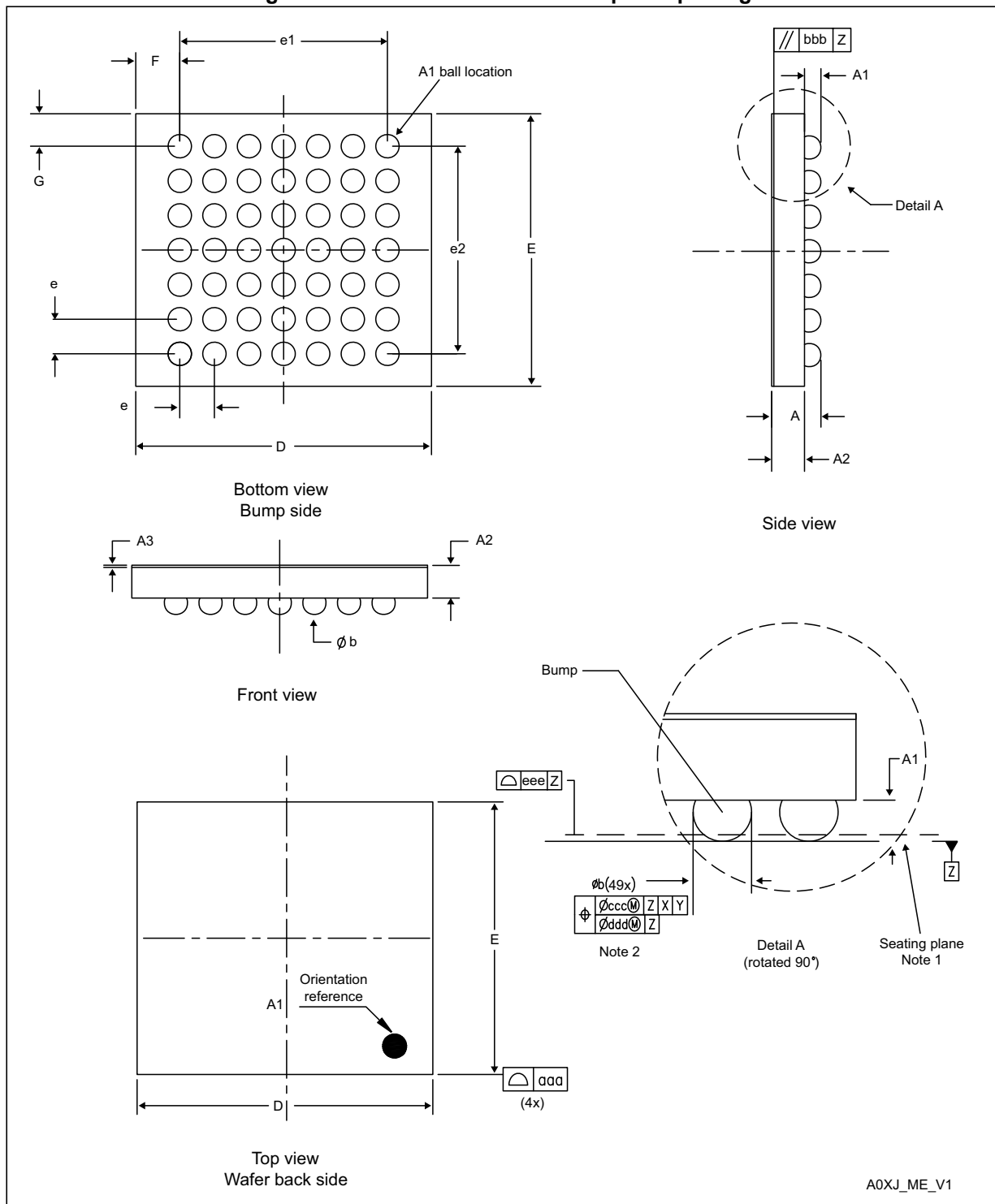
1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

## 7 Package characteristics

### 7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 34. WLCSP49 wafer level chip size package



A0XJ\_ME\_V1

1. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
2. Bump position designation per JESD 95-1, SPP-010.



**Table 73. WLCSP49 wafer level chip size package mechanical data<sup>(1)</sup>**

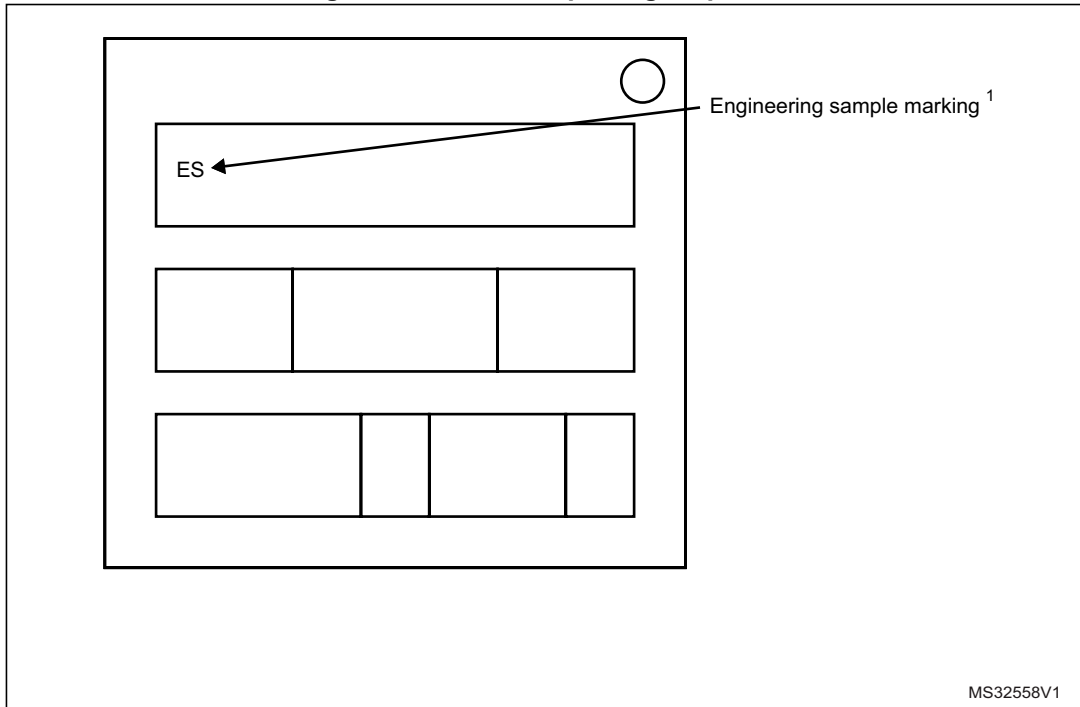
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1		0.175			0.0069	
A2		0.380			0.0150	
A3 <sup>(2)</sup>		0.025			0.0010	
b <sup>(3)</sup>	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.382	3.417	3.452	0.1331	0.1345	0.1359
E	3.116	3.151	3.186	0.1227	0.1241	0.1254
e		0.400			0.0157	
e1		2.400			0.0945	
e2		2.400			0.0945	
F		0.508			0.200	
G		0.375			0.148	
aaa		0.100			1.9291	
bbb		0.100			0.0039	
ccc		0.100			0.0039	
ddd		0.050			0.0020	
eee		0.050			0.0020	
N	Number of pins					
	49					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Marking of engineering samples**

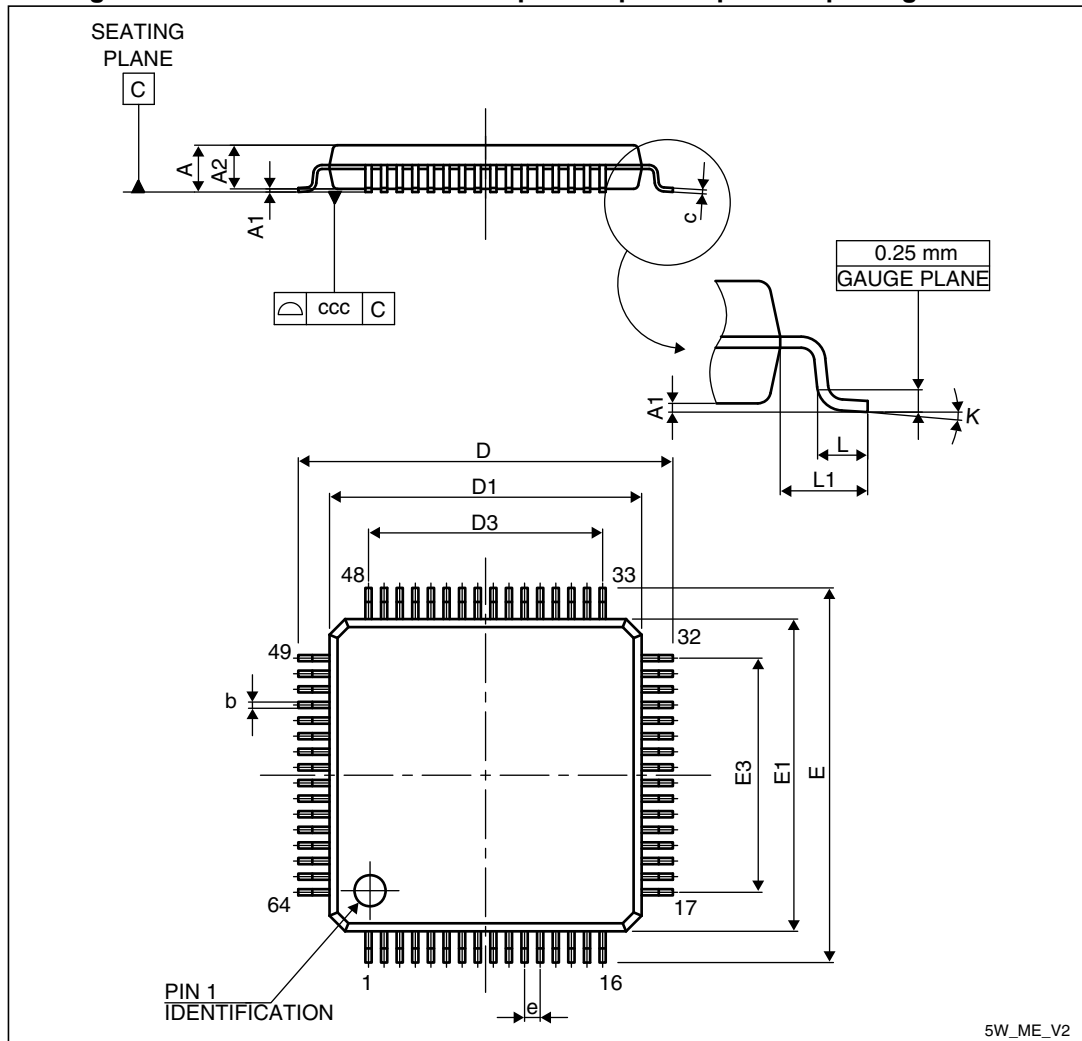
The following figure shows the engineering sample marking for the WLCSP49 package. Only the information field containing the engineering sample marking is shown.

**Figure 35. WLCSP49 package top view**



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 36. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



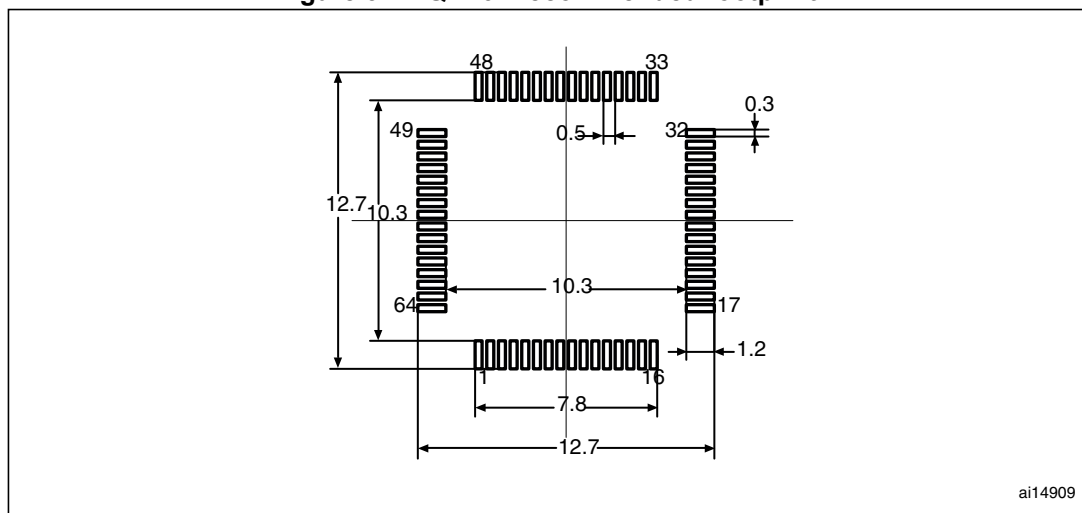
1. Drawing is not to scale.

Table 74. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	0.200		0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D.		7.500				
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.00	10.200	0.3858	0.3937	0.4016
e		0.500			0.0197	
k	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.75	0.0177	0.0236	0.0295
L1	1.000				0.0394	
ccc			0.080			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. LQFP64 recommended footprint

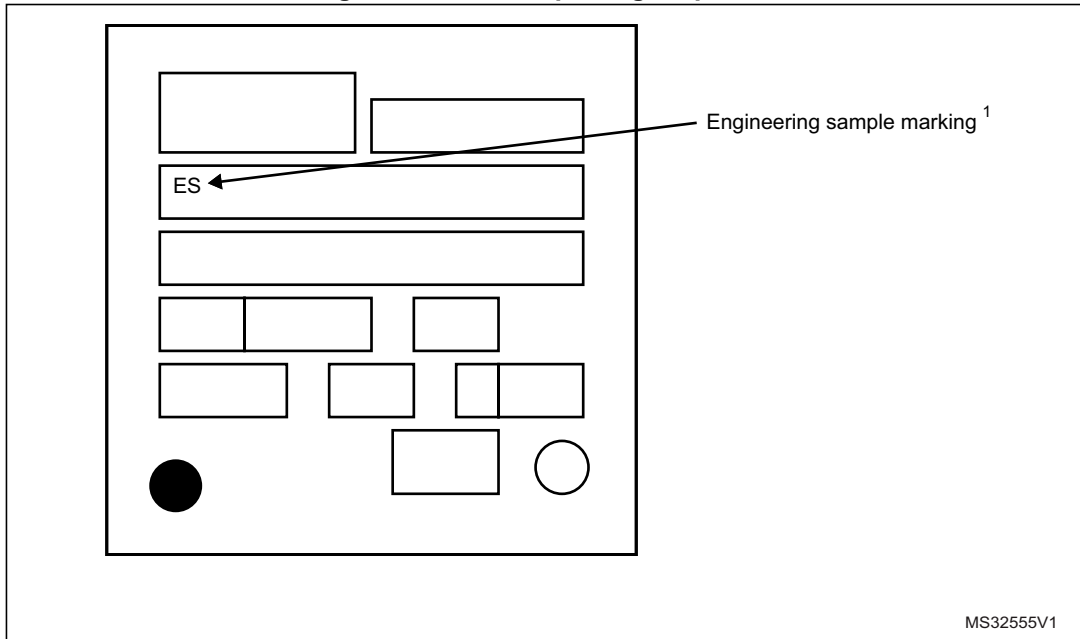


1. Drawing is not to scale.
2. Dimensions are in millimeters.

### Marking of engineering samples

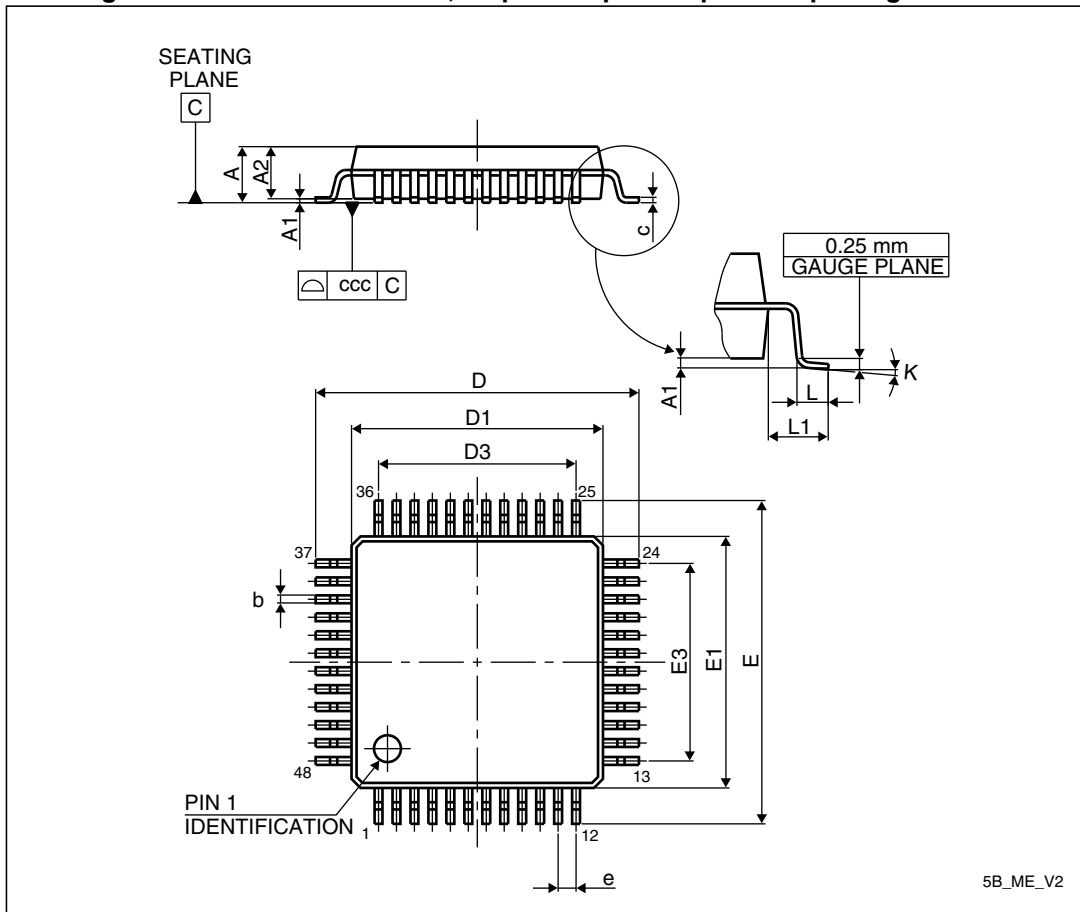
The following figure shows the engineering sample marking for the LQFP64 package. Only the information field containing the engineering sample marking is shown.

Figure 38. LQFP64 package top view



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 39. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline



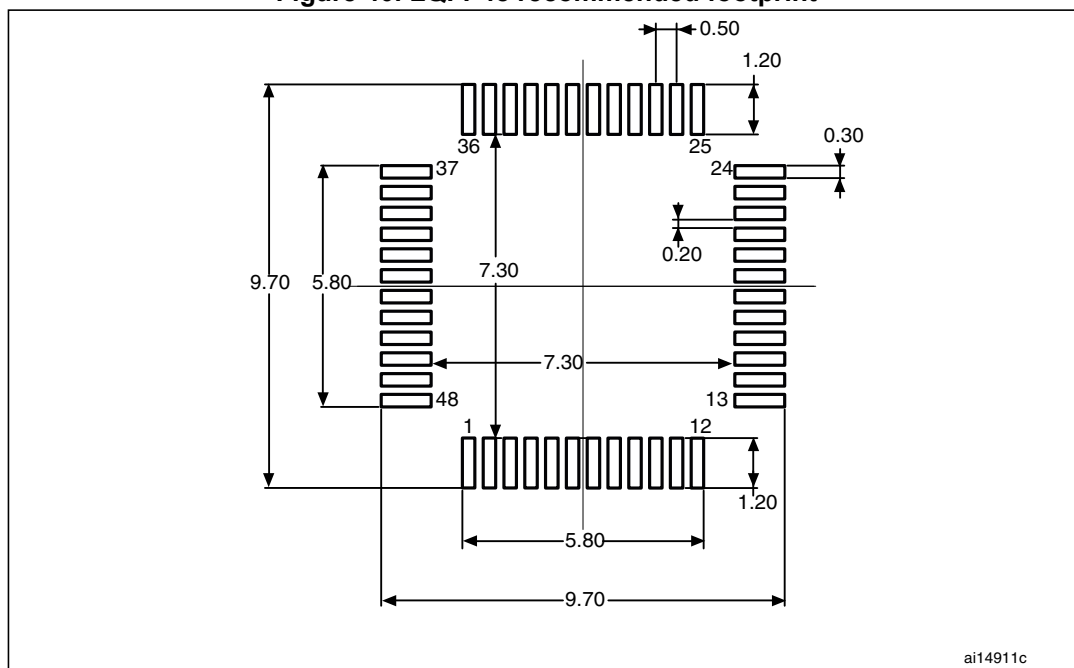
1. Drawing is not to scale.

Table 75. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050	0.150		0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	0.200		0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	5.500				0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	5.500				0.2165	
e	0.500				0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	1.000				0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.080			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP48 recommended footprint



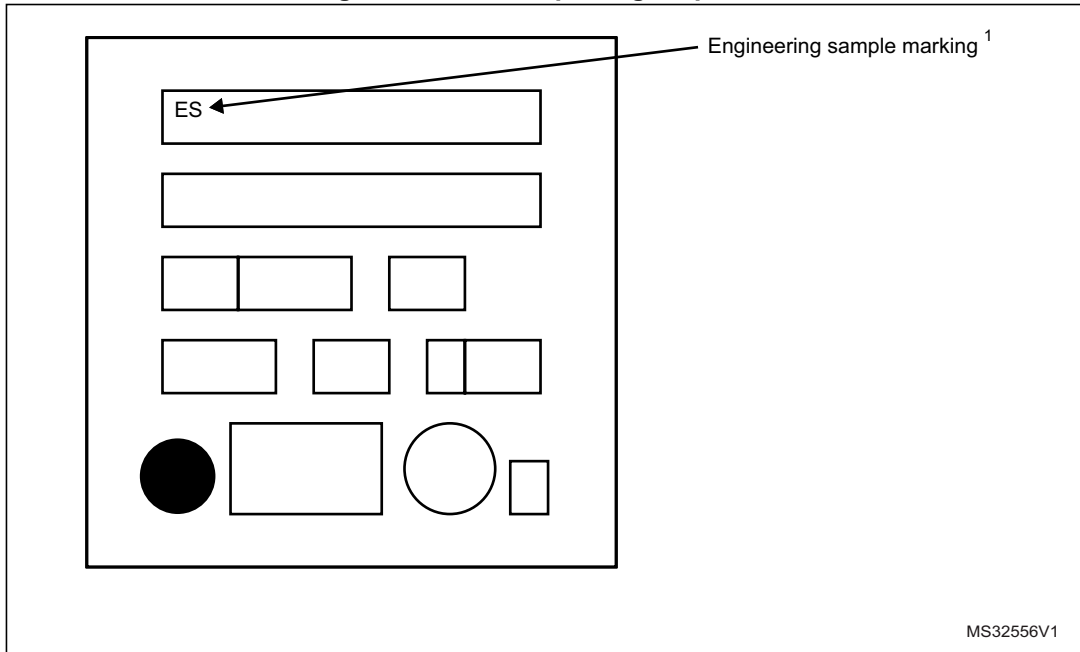
- 1. Drawing is not to scale.
- 2. Dimensions are in millimeters.



### Marking of engineering samples

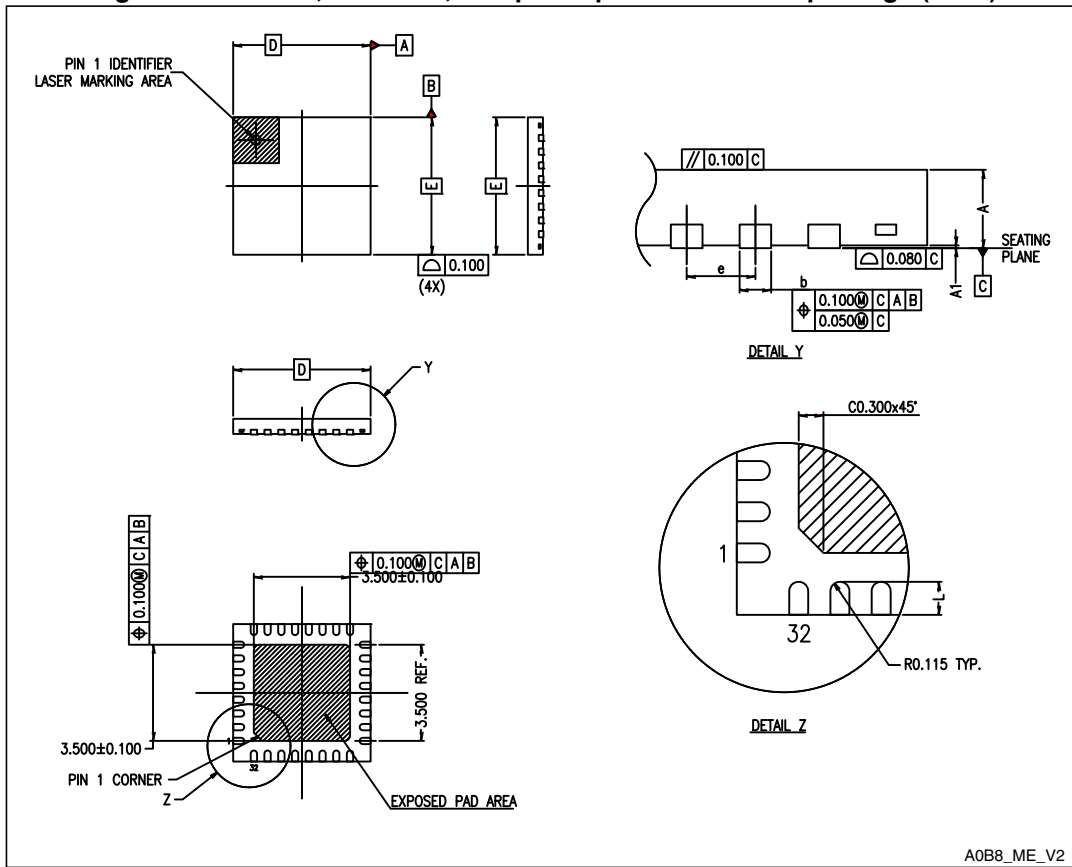
The following figure shows the engineering sample marking for the LQFP48 package. Only the information field containing the engineering sample marking is shown.

Figure 41. LQFP48 package top view



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 42. 32-lead, ultra thin, fine pitch quad flat no-lead package (5 x 5)



A0B8\_ME\_V2

1. Drawing is not to scale.

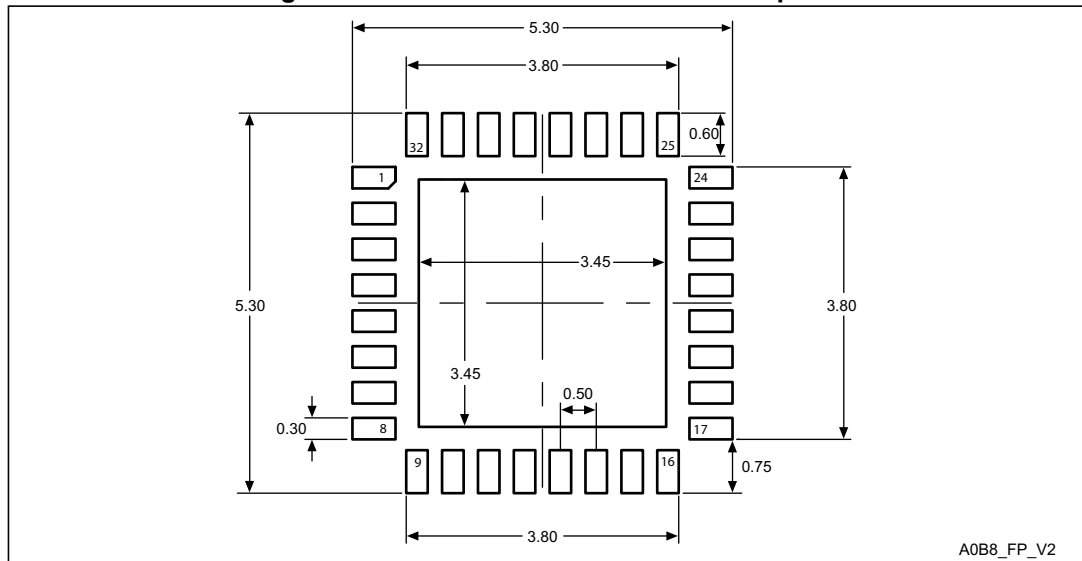
Table 76. 32-lead, ultra thin, fine pitch quad flat no-lead package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.500	0.600	0.0217	0.0197	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
A3	0.200			0.0079		
b	0.250	0.180	0.300	0.0098	0.0071	0.0118
D	5.000	4.850	5.150	0.1969	0.1909	0.2028
D2	3.450	3.200	3.700	0.1358	0.1260	0.1457
E	5.000	4.850	5.150	0.1969	0.1909	0.2028
E2	3.450	3.200	3.700	0.1358	0.1260	0.1457
e	0.500			0.0197		
L	0.400	0.300	0.500	0.0157	0.0118	0.0197
ddd			0.080			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 43. UFQFPN32 recommended footprint

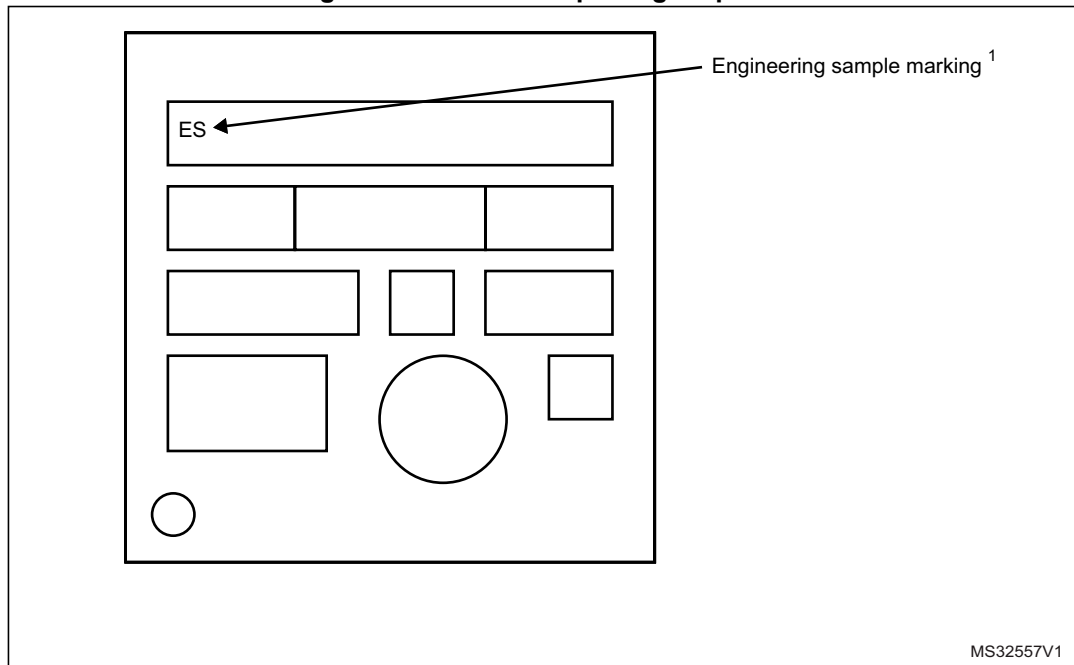


1. Drawing is not to scale.
2. Dimensions are in millimeters.

### Marking of engineering samples

The following figure shows the engineering sample marking for the UFQFPN32 package. Only the information field containing the engineering sample marking is shown.

Figure 44. UFQFPN32 package top view



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

## 7.2 Thermal characteristics

The maximum chip junction temperature ( $T_J$ max) must never exceed the values given in [Table 22: General operating conditions](#).

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D$  max =  $P_{INT}$  max +  $P_{I/O}$ max),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 77. Package thermal characteristics**

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient WCSP49 - 3.4 × 3.4 mm	49	
	Thermal resistance junction-ambient UFQFN32 - 5 × 5 mm	37	

### 7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org)

## 7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Chapter 8: Part numbering](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F301x6/x8 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 3 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 2 I/Os used at the same time in output at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 3 \times 8\text{ mA} \times 0.4\text{ V} + 2 \times 20\text{ mA} \times 1.3\text{ V} = 61.6\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 61.6\text{ mW}$ :

$$P_{Dmax} = 175 + 61.6 = 236.6\text{ mW}$$

Thus:  $P_{Dmax} = 236.6\text{ mW}$

Using the values obtained in [Table 77](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $45\text{ °C/W}$

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 236.6\text{ mW}) = 82\text{ °C} + 10.65\text{ °C} = 92.65\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Chapter 8: Part numbering](#)).

**Example 2: High-temperature application**

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 115\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 9 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 9 \times 8\text{ mA} \times 0.4\text{ V} = 28.8\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 28.8\text{ mW}$ :

$$P_{Dmax} = 70 + 28.8 = 98.8\text{ mW}$$

Thus:  $P_{Dmax} = 98.8\text{ mW}$

Using the values obtained in [Table 77](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP100,  $45\text{ °C/W}$

$$T_{Jmax} = 115\text{ °C} + (45\text{ °C/W} \times 98.8\text{ mW}) = 115\text{ °C} + 4.44\text{ °C} = 119.44\text{ °C}$$

This is within the range of the suffix 7 version parts ( $-40 < T_J < 125\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Chapter 8: Part numbering](#)).

# 8 Part numbering

**Table 78. Ordering information scheme**

Example:	STM32	F	301	R	8	T	6	xxx
<b>Device family</b>								
STM32 = ARM-based 32-bit microcontroller								
<b>Product type</b>								
F = general-purpose								
<b>Device subfamily</b>								
301 = STM32F301xx, 2.0 to 3.6 V operating voltage								
<b>Pin count</b>								
K = 32 pins								
C = 48 or 49 pins								
R = 64 pins								
<b>Flash memory size</b>								
6 = 32 Kbytes of Flash memory								
8 = 64 Kbytes of Flash memory								
<b>Package</b>								
T = LQFP								
Y= WLCSP								
U= UFQFPN								
<b>Temperature range</b>								
6 = Industrial temperature range, -40 to 85 °C								
7 = Industrial temperature range, -40 to 105 °C								
<b>Options</b>								
xxx = programmed parts								
TR = tape and reel								



## 9 Revision history

**Table 79. Document revision history**

Date	Revision	Changes
10-Apr-2014	1	Initial release.

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