

### 16,777,216 WORD X 1 BIT DYNAMIC RAM

#### Description

The TC5116100BSJ is the new generation dynamic RAM organized 16,777,216 word by 1 bit. The TC5116100BSJ utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5116100BSJ to be packaged in a standard 26/24 pin plastic SOJ (300mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

#### Features

- 16,777,216 word by 1 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in  $V_{BB}$  generator
- Low Power
  - 440mW MAX. Operating (TC5116100BSJ-60)
  - 385mW MAX. Operating (TC5116100BSJ-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write,  $\overline{CAS}$  before  $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/64ms
- Package TC5116100BSJ: SOJ26-P-300C

Note: For packaging details see Mechanical Dimensions section.

#### Key Parameters

| ITEM                                   | TC5116100BSJ |       |
|--|--------------|-------|
|  | -60          | -70   |
| $t_{RAC}$ $\overline{RAS}$ Access Time | 60ns         | 70ns  |
| $t_{AA}$ Column Address Access Time    | 30ns         | 35ns  |
| $t_{CAC}$ $\overline{CAS}$ Access Time | 15ns         | 20ns  |
| $t_{RC}$ Cycle Time                    | 110ns        | 130ns |
| $t_{PC}$ Fast Page Mode Cycle Time     | 40ns         | 45ns  |

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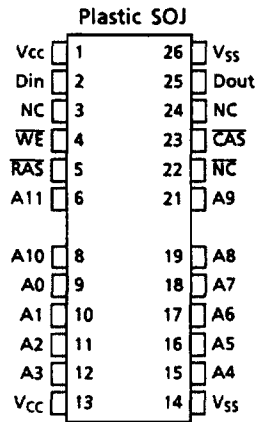
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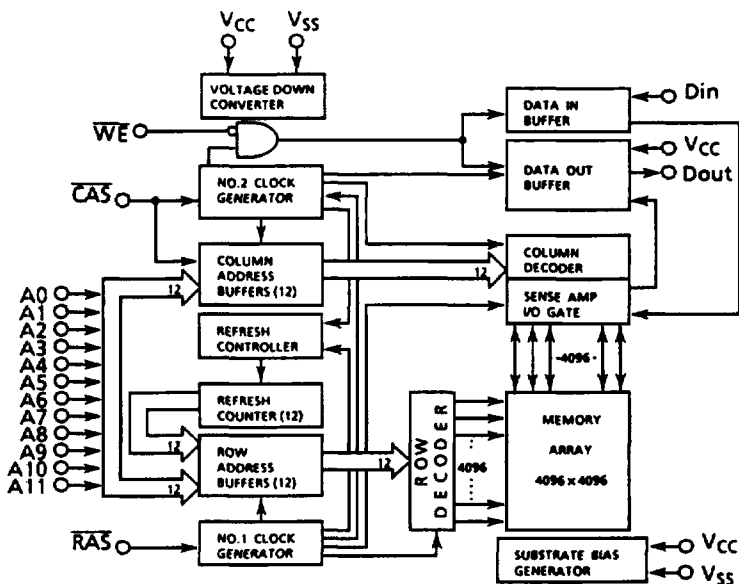
**Pin Name**

|                  |                       |
|------------------|-----------------------|
| A0 - A11         | Address Inputs        |
| $\overline{RAS}$ | Row Address Strobe    |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$  | Write Enable          |
| D <sub>IN</sub>  | Data In               |
| D <sub>OUT</sub> | Data Out              |
| V <sub>CC</sub>  | Power (+5V)           |
| V <sub>SS</sub>  | Ground                |
| N.C.             | No Connection         |

**Pin Connection (Top View)**



Block Diagram



Absolute Maximum Ratings

| ITEM                         | SYMBOL       | RATING                | UNIT | NOTE |
|------------------------------|--------------|-----------------------|------|------|
| Input Voltage                | $V_{IN}$     | $-0.5 - V_{CC} + 0.5$ | V    | 1    |
| Output Voltage               | $V_{OUT}$    | $-0.5 - V_{CC} + 0.5$ | V    | 1    |
| Power Supply Voltage         | $V_{CC}$     | $-0.5 - 7.0$          | V    | 1    |
| Operating Temperature        | $T_{OPR}$    | 0-70                  | °C   | 1    |
| Storage Temperature          | $T_{STG}$    | -55-150               | °C   | 1    |
| Soldering Temperature (10s)  | $T_{SOLDER}$ | 260                   | °C   | 1    |
| Power Dissipation            | $P_D$        | 900                   | mW   | 1    |
| Short Circuit Output Current | $I_{OUT}$    | 50                    | mA   | 1    |

## Recommended DC Operating Conditions (Ta = 0 ~ 70°C)

| SYMBOL          | PARAMETER            | MIN.   | TYP. | MAX.                   | UNIT | NOTE |
|-----------------|----------------------|--------|------|------------------------|------|------|
| V <sub>CC</sub> | Power Supply Voltage | 4.5    | 5.0  | 5.5                    | V    | 2    |
| V <sub>IH</sub> | Input High Voltage   | 2.4    | -    | V <sub>CC</sub> + 0.5* | V    | 2    |
| V <sub>IL</sub> | Input Low Voltage    | -0.5** | -    | 0.8                    | V    | 2    |

\*V<sub>CC</sub> + 2.0V at pulse width ≤ 20ns (pulse width is measured at V<sub>CC</sub>).

\*\* -2.0V at pulse width ≤ 20ns (pulse width is measured at V<sub>SS</sub>).

DC Electrical Characteristics (V<sub>CC</sub> = 5V ± 10%, Ta = 0 ~ 70°C)

| SYMBOL            | PARAMETER   | MIN             | MAX | UNIT | NOTE |          |
|-------------------|---|-----------------|-----|------|------|----------|
| I <sub>CC1</sub>  | OPERATING CURRENT<br>Average Power Supply Operating Current<br>(RAS, CAS, Address Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)                             | TC5116100BSJ-60 | -   | 80   | mA   | 3,4<br>5 |
|                   |   | TC5116100BSJ-70 | -   | 70   |      |          |
| I <sub>CC2</sub>  | STANDBY CURRENT<br>Power Supply Standby Current<br>(RAS=CAS=V <sub>IH</sub> )   | -               | 2   | mA   |      |          |
| I <sub>CC3</sub>  | RAS ONLY REFRESH CURRENT<br>Average Power Supply Current, RAS Only Mode<br>(RAS Cycling, CAS=V <sub>IH</sub> : t <sub>RC</sub> =t <sub>RC</sub> MIN.)         | TC5116100BSJ-60 | -   | 80   | mA   | 3,5      |
|                   |   | TC5116100BSJ-70 | -   | 70   |      |          |
| I <sub>CC4</sub>  | FAST PAGE MODE CURRENT<br>Average Power Supply Current, Fast Page Mode<br>(RAS=V <sub>IL</sub> , CAS, Address Cycling: t <sub>PC</sub> =t <sub>PC</sub> MIN.) | TC5116100BSJ-60 | -   | 70   | mA   | 3,4<br>5 |
|                   |   | TC5116100BSJ-70 | -   | 60   |      |          |
| I <sub>CC5</sub>  | STANDBY CURRENT<br>Power Supply Standby Current<br>(RAS=CAS=V <sub>CC</sub> -0.2V)  | -               | 1   | mA   |      |          |
| I <sub>CC6</sub>  | CAS BEFORE RAS REFRESH CURRENT<br>Average Power Supply Current, CAS Before RAS Mode<br>(RAS, CAS, Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)             | TC5116100BSJ-60 | -   | 80   | mA   | 3,5      |
|                   |   | TC5116100BSJ-70 | -   | 70   |      |          |
| I <sub>I(L)</sub> | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any input<br>(0V < V <sub>IN</sub> < V <sub>CC</sub> , All Other Pins Not Under Test=0V)                      | -10             | 10  | μA   |      |          |
| I <sub>O(L)</sub> | OUTPUT LEAKAGE CURRENT<br>(D <sub>OUT</sub> is disabled, (0V ≤ V <sub>OUT</sub> < V <sub>CC</sub> ))  | -10             | 10  | μA   |      |          |
| V <sub>OH</sub>   | OUTPUT LEVEL<br>Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)   | 2.4             | -   | V    |      |          |
| V <sub>OL</sub>   | OUTPUT LEVEL<br>Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)  | -               | 0.4 | V    |      |          |

Electrical Characteristics and Recommended AC Operating Conditions ( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0\text{--}70^\circ\text{C}$ ) (Notes 6,7,8)

| SYMBOL     | PARAMETER   | TC5116100BSJ |         |     |         | UNIT | NOTES   |
|------------|---|--------------|---------|-----|---------|------|---------|
|            |   | -60          |         | -70 |         |      |         |
|            |   | MIN          | MAX.    | MIN | MAX     |      |         |
| $t_{RC}$   | Random Read or Write Cycle Time   | 110          | -       | 130 | -       | ns   |         |
| $t_{RMW}$  | Read-Modify-Write Cycle   | 130          | -       | 155 | -       | ns   |         |
| $t_{PC}$   | Fast Page Mode Cycle Time   | 40           | -       | 45  | -       | ns   |         |
| $t_{PRMW}$ | Fast Page Mode Read-Modify-Write Cycle Time                                 | 60           | -       | 70  | -       | ns   |         |
| $t_{RAC}$  | Access Time from $\overline{RAS}$   | -            | 60      | -   | 70      | ns   | 9,14,15 |
| $t_{CAC}$  | Access Time from $\overline{CAS}$   | -            | 15      | -   | 20      | ns   | 9,14    |
| $t_{AA}$   | Access Time from Column Address   | -            | 30      | -   | 35      | ns   | 9,15    |
| $t_{CPA}$  | Access Time from $\overline{CAS}$ Precharge                                 | -            | 35      | -   | 40      | -    | 9       |
| $t_{CLZ}$  | $\overline{CAS}$ to Output in Low-Z   | 0            | -       | 0   | -       | ns   | 9       |
| $t_{OFF}$  | Output Buffer Turn-off Delay  | 0            | 15      | 0   | 15      | ns   | 10      |
| $t_T$      | Transition Time (Rise and Fall)   | 3            | 50      | 3   | 50      | ns   | 8       |
| $t_{RP}$   | $\overline{RAS}$ Precharge Time   | 40           | -       | 50  | -       | ns   |         |
| $t_{RAS}$  | $\overline{RAS}$ Pulse Width  | 60           | 10,000  | 70  | 10,000  | ns   |         |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode)                               | 60           | 400,000 | 70  | 400,000 | ns   |         |
| $t_{RSH}$  | $\overline{RAS}$ Hold Time  | 15           | -       | 20  | -       | ns   |         |
| $t_{RHCP}$ | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode) | 35           | -       | 40  | -       | ns   |         |
| $t_{CSH}$  | $\overline{CAS}$ Hold Time  | 60           | -       | 70  | -       | ns   |         |
| $t_{CAS}$  | $\overline{CAS}$ Pulse Width  | 15           | 10,000  | 20  | 10,000  | ns   |         |
| $t_{RCD}$  | $\overline{RAS}$ to $\overline{CAS}$ Delay Time                             | 20           | 45      | 20  | 50      | ns   | 14      |
| $t_{RAD}$  | $\overline{RAS}$ to Column Address Delay Time                               | 15           | 30      | 15  | 35      | ns   | 15      |
| $t_{CRP}$  | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time                         | 5            | -       | 5   | -       | ns   |         |
| $t_{CP}$   | $\overline{CAS}$ Precharge Time   | 10           | -       | 10  | -       | ns   |         |
| $t_{ASR}$  | Row Address Set-Up Time   | 0            | -       | 0   | -       | ns   |         |
| $t_{RAH}$  | Row Address Hold Time   | 10           | -       | 10  | -       | ns   |         |
| $t_{ASC}$  | Column Address Set-Up Time  | 0            | -       | 0   | -       | ns   |         |
| $t_{CAH}$  | Column Address Hold Time  | 10           | -       | 15  | -       | ns   |         |
| $t_{RAL}$  | Column Address to $\overline{RAS}$ Lead Time                                | 30           | -       | 35  | -       | ns   |         |
| $t_{RCS}$  | Read Command Set-Up Time  | 0            | -       | 0   | -       | ns   |         |
| $t_{RCH}$  | Read Command Hold Time  | 0            | -       | 0   | -       | ns   | 11      |
| $t_{RRH}$  | Read Command Hold Time referenced to $\overline{RAS}$                       | 0            | -       | 0   | -       | ns   | 11      |
| $t_{WCH}$  | Write Command Hold Time   | 10           | -       | 15  | -       | ns   |         |

## Electrical Characteristics and Recommended AC Operating Conditions (Cont)

| SYMBOL     | PARAMETER   | TC5116100BSJ |      |     |     | UNIT | NOTES |
|------------|---|--------------|------|-----|-----|------|-------|
|            |   | -60          |      | -70 |     |      |       |
|            |   | MIN          | MAX. | MIN | MAX |      |       |
| $t_{WP}$   | Write Command Pulse Width   | 10           | -    | 15  | -   | ns   |       |
| $t_{RWL}$  | Write Command to $\overline{RAS}$ Lead Time   | 15           | -    | 20  | -   | ns   |       |
| $t_{CWL}$  | Write Command to $\overline{CAS}$ Lead Time   | 15           | -    | 20  | -   | ns   |       |
| $t_{DS}$   | Data Set-Up Time  | 0            | -    | 0   | -   | ns   | 12    |
| $t_{DH}$   | Data Hold Time  | 10           | -    | 15  | -   | ns   | 12    |
| $t_{REF}$  | Refresh Period  | -            | 64   | -   | 64  | ms   |       |
| $t_{WCS}$  | Write Command Set-Up Time   | 0            | -    | 0   | -   | ns   | 13    |
| $t_{CWD}$  | $\overline{CAS}$ to $\overline{WE}$ Delay Time  | 15           | -    | 20  | -   | ns   | 13    |
| $t_{RWD}$  | $\overline{RAS}$ to $\overline{WE}$ Delay Time  | 60           | -    | 70  | -   | ns   | 13    |
| $t_{AWD}$  | Column Address to $\overline{WE}$ Delay Time  | 30           | -    | 35  | -   | ns   | 13    |
| $t_{CPWD}$ | $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time  | 35           | -    | 40  | -   | ns   | 13    |
| $t_{CSR}$  | $\overline{CAS}$ Set-up Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Cycle)                       | 5            | -    | 5   | -   | ns   |       |
| $t_{CHR}$  | $\overline{CAS}$ Hold Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Cycle)                         | 10           | -    | 15  | -   | ns   |       |
| $t_{RPC}$  | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time   | 5            | -    | 5   | -   | ns   |       |
| $t_{CPT}$  | $\overline{CAS}$ Precharge Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)       | 20           | -    | 30  | -   | ns   |       |
| $t_{WTS}$  | Write Command Set-up Time<br>(Test Mode In)   | 10           | -    | 10  | -   | ns   |       |
| $t_{WTH}$  | Write Command Hold Time<br>(Test Mode In)   | 10           | -    | 10  | -   | ns   |       |
| $t_{WRP}$  | $\overline{WE}$ to $\overline{RAS}$ Precharge Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Cycle) | 10           | -    | 10  | -   | ns   |       |
| $t_{WRH}$  | $\overline{WE}$ to $\overline{RAS}$ Hold Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Cycle)      | 10           | -    | 10  | -   | ns   |       |

## Electrical Characteristics and Recommended AC Operating Conditions in the Test Mode

| SYMBOL     | PARAMETER   | TC5116100BSJ |         |     |         | UNIT | NOTES     |
|------------|---|--------------|---------|-----|---------|------|-----------|
|            |   | -60          |         | -70 |         |      |           |
|            |   | MIN          | MAX.    | MIN | MAX     |      |           |
| $t_{RC}$   | Random Read or Write Cycle Time   | 115          | -       | 135 | -       | ns   |           |
| $t_{PC}$   | Fast Page Mode Cycle Time   | 45           | -       | 50  | -       | ns   |           |
| $t_{RAC}$  | Access Time from $\overline{RAS}$   | -            | 65      | -   | 75      | ns   | 9, 14, 15 |
| $t_{CAC}$  | Access Time from $\overline{CAS}$   | -            | 20      | -   | 25      | ns   | 9, 14     |
| $t_{AA}$   | Access Time from Column Address   | -            | 35      | -   | 40      | ns   | 9, 15     |
| $t_{CPA}$  | Access Time from $\overline{CAS}$ Precharge                                 | -            | 40      | -   | 45      | ns   | 9         |
| $t_{RAS}$  | $\overline{RAS}$ Pulse Width  | 65           | 10,000  | 75  | 10,000  | ns   |           |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode)                               | 65           | 400,000 | 75  | 400,000 | ns   |           |
| $t_{RSH}$  | $\overline{RAS}$ Hold Time  | 20           | -       | 25  | -       | ns   |           |
| $t_{CSH}$  | $\overline{CAS}$ Hold Time  | 65           | -       | 75  | -       | ns   |           |
| $t_{RHCP}$ | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode) | 40           | -       | 45  | -       | ns   |           |
| $t_{CAS}$  | $\overline{CAS}$ Pulse Width  | 20           | 10,000  | 25  | 10,000  | ns   |           |
| $t_{RAL}$  | Column Address to $\overline{RAS}$ Lead Time                                | 35           | -       | 40  | -       | ns   |           |

Capacitance ( $V_{CC} = 5V \pm 10\%$ ,  $f = 1MHz$ ,  $T_a = 0 \sim 70^\circ C$ )

| SYMBOL   | PARAMETER   | MIN | MAX | UNIT |
|----------|---|-----|-----|------|
| $C_{I1}$ | Input Capacitance ( $A_0 \sim A_{10}$ , $D_{IN}$ )                          | -   | 5   | pF   |
| $C_{I2}$ | Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ) | -   | 7   |      |
| $C_O$    | Input Capacitance ( $D_{OUT}$ )   | -   | 7   |      |

Note: Please refer to Timing Diagrams Number 3.

**Notes:**

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while  $\overline{RAS}=V_{IL}$ . In case of  $I_{CC4}$ , it can be changed once or less during a fast page mode cycle ( $t_{PC}$ ).
6. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles instead of 8  $\overline{RAS}$  only refresh cycles are required.
7. AC measurements assume  $t_T=5$ ns.
8.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10.  $t_{OFF}$  (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in Read-Modify-Write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}$  (min.),  $t_{CWD} \geq t_{CWD}$  (min.),  $t_{AWD} \geq t_{AWD}$  (min.) and  $t_{CPWD} \geq t_{CPWD}$  (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the  $t_{RCD}$  (max.) limit insures that  $t_{RAC}$  can be met.  $t_{RCD}$  (max.) is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.) limit, then access time is controlled by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}$  (max.) limit insures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, then access time is controlled by  $t_{AA}$ .