DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- **DC triggered from active HIGH or active LOW inputs**
- **Retriggerable for very long pulses up to 100% duty factor**
- **Direct reset terminates output pulse**
- **Schmitt-trigger action on all inputs except for the reset input**
- **Output capability: standard (except for nR_{EXT}/C_{EXT})**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT423 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT423 are dual retriggerable monostable multivibrators with output pulse width control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse periode (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. When $n\overline{R}_D$ is LOW, it forces the nQ output LOW, the $n\overline{Q}$ output HIGH and also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V; R_{EXT} = 5 kΩ; C_{EXT} = 0 pF	25	26	ns
	$n\overline{R}_D$ to nQ, $n\overline{Q}$		20	22	ns
C_I	input capacitance		3.5	3.5	pF
t_W	minimum output pulse width nQ, $n\overline{Q}$	notes 1 and 2	75	75	ns

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
D = duty factor in %
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
C_{EXT} = timing capacitance in pF

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset action (active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

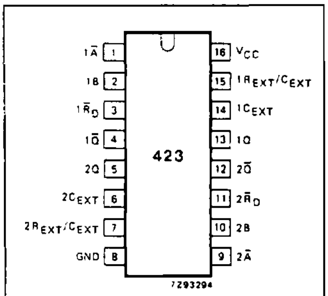
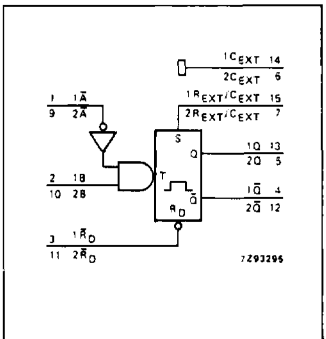


Fig. 1 Pin configuration.



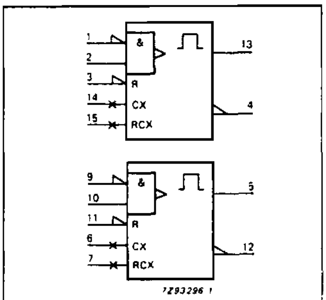


Fig. 3 IEC logic symbol.

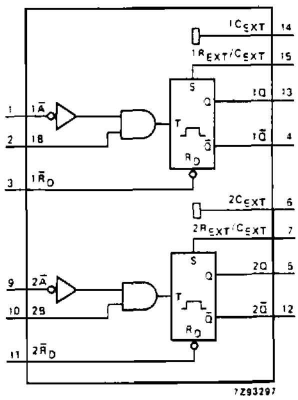


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{R}_D$	nĀ	nB	nQ	nQ̄
L	X	X	L	H
X	H	X	L *	H *
X	X	L	L *	H *
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⊔ = one LOW level output pulse

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.

GENERAL DESCRIPTION (Cont'd)

Figures 7 and 8 illustrate pulse control by reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.
For pulse widths, when $C_{EXT} < 10\,000$ pF, see Fig. 9.
When $C_{EXT} > 10\,000$ pF, the typical output pulse width is defined as:

$t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.),

where, t_W = pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF.

Schmitt-trigger action in the nĀ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The "423" is identical to the "123" but cannot be triggered via the reset input.

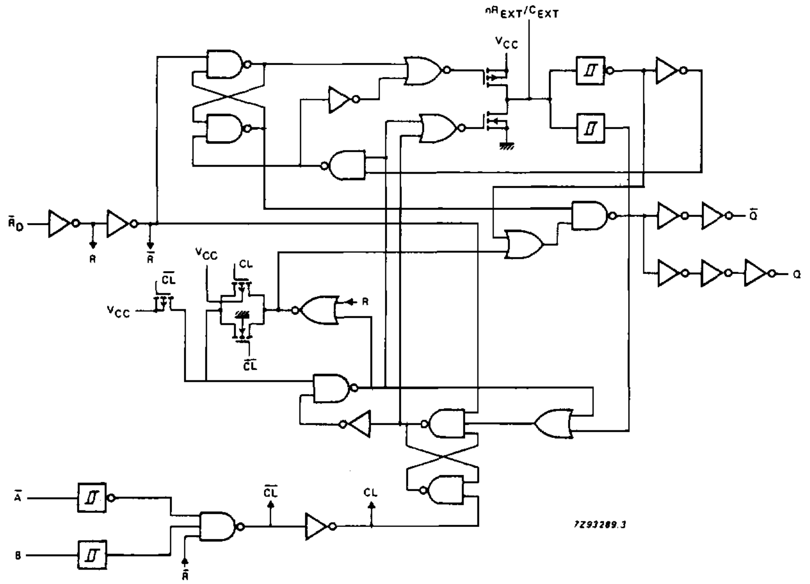


Fig. 5 Logic diagram.

Note to Fig. 5

It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

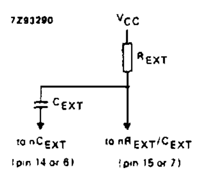


Fig. 6 Timing component connections.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	V_{CC} V	TEST CONDITIONS WAVEFORMS/NOTES
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$, nQ		80 29 23	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
t_W	trigger pulse width $n\overline{A}$ = LOW	100 20 17	11 4 3		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	trigger pulse width nB = HIGH	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	100 20 17	14 5 4		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		450		–		–		μs	5.0	$C_{EXT} = 100$ nF; $R_{EXT} = 10$ kΩ; Figs 7 and 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		75		–		–		ns	5.0	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		110		–		–		ns	5.0	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ; note 2; Fig. 7
R_{EXT}	external timing resistor	10 2		1000 1000	–		–		kΩ	2.0 5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig. 9; note 3

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\overline{A}$, nB	0.35
$n\overline{R}_D$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	TEST CONDITIONS V_{CC} V	WAVEFORMS/NOTES
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to $n\overline{Q}$, nQ		30	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		26	48		60		72	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	
t_W	trigger pulse width $n\overline{A}$ = LOW	20	5		25		30		ns	4.5	Fig. 7
t_W	trigger pulse width nB = HIGH	20	5		25		30		ns	4.5	Fig. 7
t_W	reset pulse width $n\overline{R}_D$ = LOW	20	7		25		30		ns	4.5	Fig. 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		450		–		–		μs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Figs 7 and 8
t_W	output pulse width nQ = HIGH $n\overline{Q}$ = LOW		75		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 1; Figs 7 and 8
t_{rt}	retrigger time $n\overline{A}$, nB		41		–		–		ns	5.0	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; note 2; Fig. 7
R_{EXT}	external timing resistor	2		1000	–		–		kΩ	5.0	Fig. 9
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig 9; note 3

Notes to AC characteristics

1. For other R_{EXT} and C_{EXT} combinations see Fig. 9.
   If $C_{EXT} > 10$ pF, the next formula is valid:
   $t_W = K \times R_{EXT} \times C_{EXT}$ (typ.)
   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for V_{CC} = 5.0 V and 0.55 for V_{CC} = 2.0 V.
   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.
   The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.
   If $C_{EXT} > 10$ pF, the next formula (at V_{CC} = 5.0 V) for the set-up time of a retrigger pulse is valid:
   $t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT})$ (typ.)
   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in kΩ.
   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50$ pF.

AC WAVEFORMS

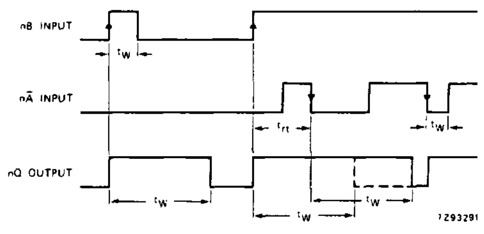


Fig. 7 Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

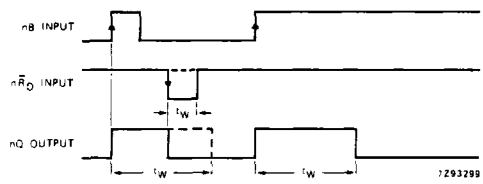


Fig. 8 Output pulse control using reset input $n\overline{R}_D$; $n\overline{A}$ = LOW.

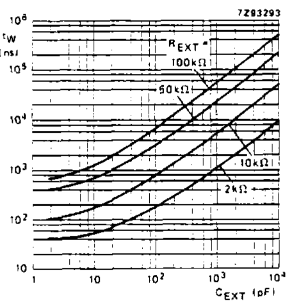


Fig. 9 Typical output pulse width as a function of the external capacitor values at V_{CC} = 5.0 V and T_{amb} = 25 °C.

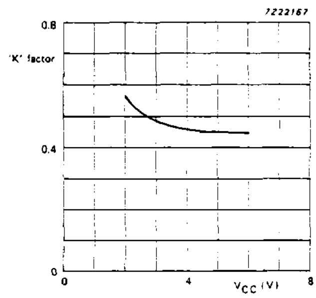


Fig. 10 Typical 'K' factor; external capacitance = 10 nF, external resistance = 10 kΩ to 100 kΩ and T_{amb} = 25 °C.

APPLICATION INFORMATION

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_X and C_X, this output pulse can be eliminated using the circuit shown in Fig. 11.

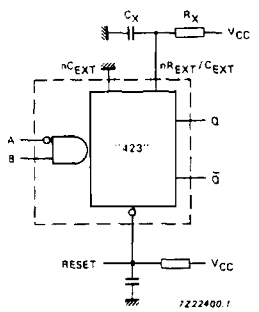


Fig. 11 Power-up output pulse elimination circuit.

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may substain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky-type diode able to withstand large current surges and connect as shown in Fig. 12.

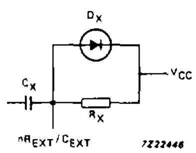


Fig. 12 Power-down protection circuit.