



AP1013CEN

18V 1ch H-Bridge Motor Driver IC

1. General Description

The AP1013CEN realizes four drive mode of forward, reverse, break and standby by 1 channel H-bridge motor driver corresponding to operating voltage 18V. The AP1013CEN layouts N-channel LDMOSFET in high side and low side in output circuit and realizes a small package. Also it has under voltage detection and thermal shut down circuits. It is suitable for driving various small motor.

2. Features

- Control Power Supply Voltage (VC) 2.7V to 5.5V
- Logic Terminal Supply Voltage 1.62V to VC
- Wide Motor Driver Operating Voltage 2V to 18V
(N-channel MOSFET high side and Low side architecture)
- Maximum Output Current (DC) 1.3A
- Maximum Output Current (Peak) 2.2A (Ta=25°C, within 10ms in 200ms)
- Maximum Output Current (Peak) 3.3A (Ta=25°C, within 5ms in 200ms)
- Maximum Output Current (Peak) 5.0A (Ta=25°C, within 2ms in 200ms)
- H-Bridge On Resistance RON(TOP+BOT)=0.38Ω@25°C
- Power-Down Mode Quiescent current is under 1uA (Ta=25°C)
- Built-in Under Voltage Detection Circuit Detect V_{VC} under 2.2V
- Built-in Thermal Shut Down Circuit (Tj) 175°C
- Junction Temperature 150°C
- Package 16-pin QFN Package (3mm × 3mm)

3. Table of Contents

1. General Description	1
2. Features.....	1
3. Table of Contents.....	2
4. Block Diagram.....	3
5. Ordering Guide	3
6. Pin Configurations and Functions.....	4
■ Pin Configurations	4
■ Functions	4
■ Terminal Equivalent Circuit	5
7. Absolute Maximum Ratings	6
8. Recommended Operating Conditions	7
9. Electrical Characteristics	7
10. Descriptions	9
10.1 Control Logic.....	9
10.2 Basic Architecture of the Motor Driver.....	9
10.3 Protection Circuits	10
11. Recommended External Circuits.....	11
■ Recommended External Circuit.....	11
■ Parts List	11
12. Package.....	12
■ Outline Dimensions	12
■ Reference Foot Pattern	12
■ Marking	13
13. Revise History	14
IMPORTANT NOTICE	15

4. Block Diagram

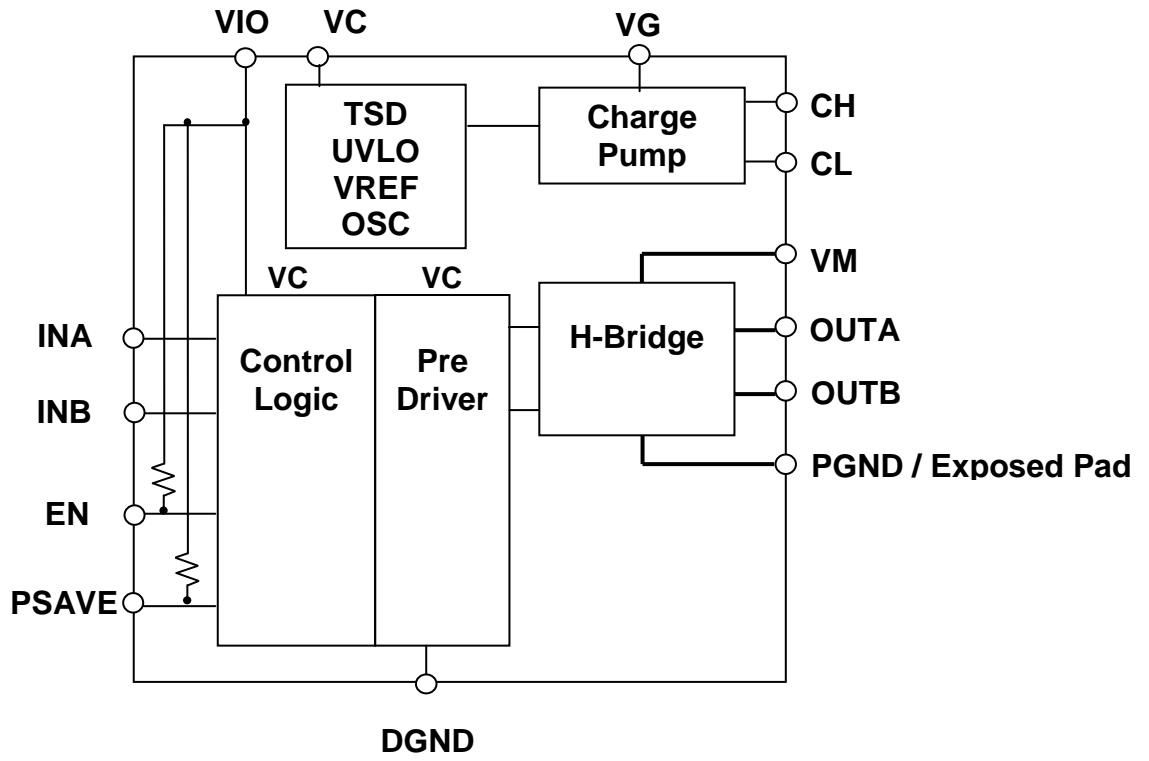


Figure 1. Block Diagram

5. Ordering Guide

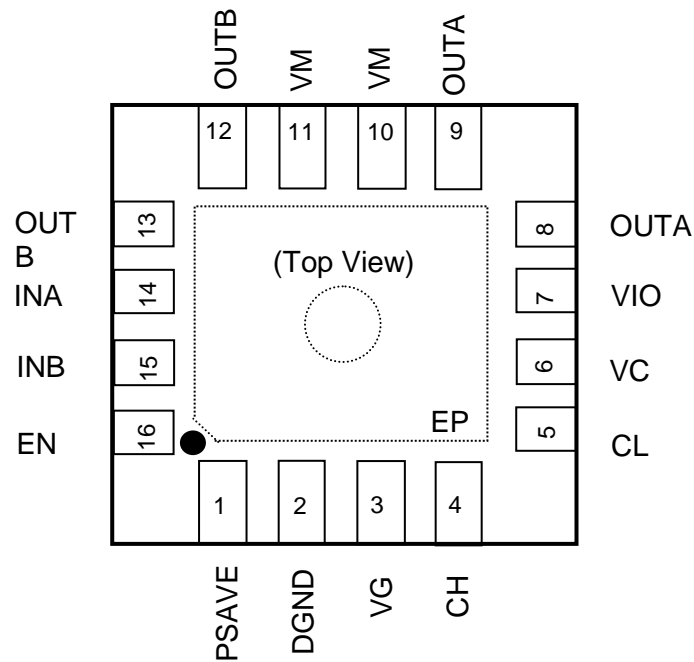
AP1013CEN

-30~85°C

16-pin QFN

6. Pin Configurations and Functions

■ Pin Configurations



Note) EP(Exposed Pad) is Power Ground.
The Exposed Pad is necessary soldered to PCB.

■ Functions

No	Pin Name	I/O	Description	Note
1	PSAVE	I	Power save input terminal	100k Ω Pull-up
2	DGND	P	Ground terminal	
3	VG	O	Connect terminal of charge pump output capacitor	
4	CH	O	Connect terminal of charge pump capacitor	
5	CL	O	Connect terminal of charge pump capacitor	
6	VC	P	Control power supply terminal	
7	VIO	P	Power supply terminal for logic input	
8,9	OUTA	O	Motor driver output terminal	
10,11	VM	P	Motor driver power supply	
12,13	OUTB	O	Motor driver output terminal	
14	INA	I	Control signal input terminal	
15	INB	I	Control signal input terminal	
16	EN	I	Enable signal input terminal	100k Ω Pull-up
EP	PGND	P	Power ground terminal	Exposed Pad

Note 1. I (Input terminal), O(Output terminal) and P (Power terminal)

■ Terminal Equivalent Circuit

Pin name	Name	Functions	Equivalent Circuits
6	VC	Control power supply	
7	VIO	Power supply for logic input	
10,11	VM	Motor driver power supply	
1 16	PSAVE EN	Logic input (Built-in pull-up resistor)	
14 15	INA INB	Control signal input	
8,9 12,13	OUTA OUTB	Motor driver output	
3 4	VG CH	Connect terminal of charge pump output capacitor Connect terminal of charge pump capacitor	
5	CL	Connect terminal of charge pump capacitor	
2 EP	DGND PGND	Ground terminal Power ground terminal	

7. Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Note
Control power supply voltage	VC	-0.5	6	V	
Logic terminal supply voltage	VIO	-0.5	6	V	
Motor driver power supply voltage	VM	-0.5	19	V	
VC, VIO level terminal voltage	Vterminal1	-0.5	5.5	V	
VM level terminal voltage (OUTA, and OUTB)	Vterminal2	-0.5	19	V	
VG, CH terminal voltage	Vterminal3	-0.5	25	V	
Maximum DC output current	IloaddcMD	-	1.3	A	OUTA and OUTB terminal
Maximum peak output current	IloadpeakMD	-	2.2 3.3 5.0	A	OUTA and OUTB terminal Under 10ms in 200ms Under 5ms in 200ms Under 2ms in 200ms
Power dissipation	PD	-	2083	mW	(Note 4) Ta=25°C
		-	1083	mW	(Note 4) Ta=85°C
Operating Temperature range	Ta	-30	85	°C	
Junction temperature	Tj	-	150	°C	
Storage temperature	Tstg	-65	150	°C	

Note 2. All above voltage is defined to VSS (DGND/PGND terminal voltage)

Note 3. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the products on the verge of suffering physical damages, and therefore products must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Note 4. When 2-layer board is used, this is calculated $R_{\theta JA}=60^{\circ}\text{C}/\text{W}$. EP terminal should be connected to ground.

Note 5. Input terminal does not work until input logic terminal power supplies VIO, and is handled as “L” fixation.

Note 6. The each power supply of VM, VC and VIO is sequence-free.

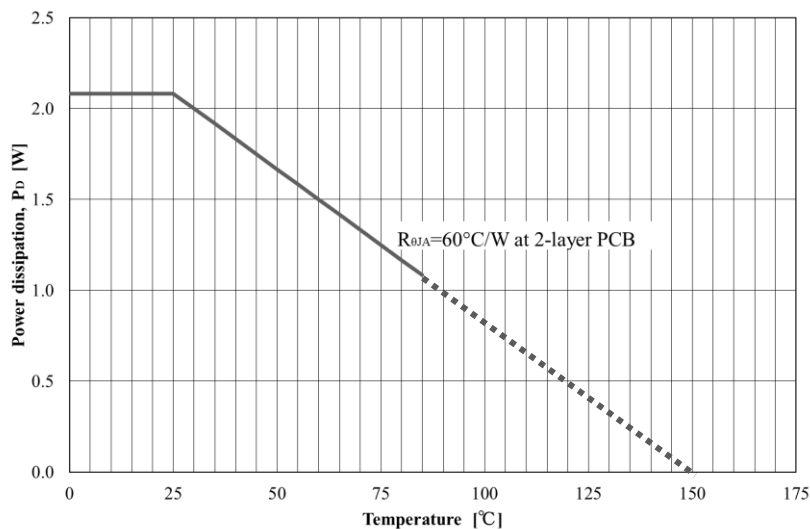


Figure 2. Power Dissipation

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit
Control power supply voltage	VC	2.7	3.3	5.5	V
Logic terminal supply voltage	VIO	1.62	1.8/3.3	VC	V
Motor driver power supply voltage	VM	2.0	-	18	V
Input frequency range	Fin	-	-	200	kHz

9. Electrical Characteristics

(Ta = 25°C, VM=15V, VC = 3.3V and VIO= 3.3V, unless otherwise specified.)

Parameter	Symbol	Test conditions	min	typ	max	Unit
Charge pump						
Charge pump voltage	VG	VG=VC+VM	18.0	18.2	18.3	V
Charge pump wake up time	t _{VG}	VG=VC+VM-0.3V	0.1	0.36	3	ms
VDET1						
VC under voltage detect voltage	VC _{DETLV}		1.9	2.2	2.5	V
TSD						
Thermal shut down temperature (Note 7)	T _{DET}		150	175	200	°C
Temperature hysteresis (Note 7)	T _{DETHYS}		20	30	40	°C
Quiescent current						
VM quiescent current at no power	I _{VMNOPOW}	VC=0V	-	-	1	μA
VM quiescent current at standby	I _{VMSTBY}	PSAVE="L", EN="H" INA="L", INB="L"	-	16	50	μA
VC quiescent current at standby	I _{VCSTBY}	PSAVE="L", EN="H" INA="L", INB="L"	-	150	400	μA
VC quiescent current at power save	I _{VMPSAVE}	PSAVE="H", EN="H"	-	-	1	μA
VC quiescent current at PWM operation	I _{VCPWM}	INA=200kHz, INB="H"	-	0.5	0.8	mA
Motor Driver						
Driver on resistance (High side or Low side)	R _{ON1}	VC=3.3V, Iload=100mA Ta=25°C	-	0.19	0.27	Ω
Driver on resistance (High side or Low side) (Note 7)	R _{ON2} Design certification	VC=3.3V, Iload=1.0A Ta=25°C (Equivalent Tj=50°C)	-	0.21	0.29	Ω
Driver on resistance (High side or Low side) (Note 7)	R _{ON3} Design certification	VC=3.3V, Iload=1.0A Ta=85°C (Equivalent Tj=115°C)	-	0.25	0.35	Ω

Body diode forward voltage	V_{FMD}	$I_F=100mA$	-	0.8	1.2	V
H-Bridge propagation delay time (“L”→”L”) (Note 8)	t_{PDLHB}	$t_r=t_f=10ns$	-	0.10	0.5	μs
H-Bridge propagation delay time (“H”→”H”) (Note 8)	t_{PDHHB}	$t_r=t_f=10ns$	-	0.35	1.0	μs
Motor Driver						
H-Bridge propagation delay time (HiZ→”H”)	t_{PDZHBB}	$t_r=t_f=10ns$	-	0.15	0.5	μs
H-Bridge propagation delay time (“H”→HiZ)	t_{PDHZBB}	$t_r=t_f=10ns$	-	0.15	1.0	μs
H-bridge output puls width	t_{PWOHB}	$PWL=1.0\mu s, t_r=t_f=10ns$	0.6	0.9	-	μs
Control logic						
Input “H” level voltage (INA, INB, EN, PSAVE)	V_{IH}	$V_{IO}=1.6V\sim 5.5V$	$0.7\times V_{IO}$	-	-	V
Input “L” level voltage (INA, INB, EN, PSAVE)	V_{IL}		-	-	$0.3\times V_{IO}$	V
Input “H” level current (INA, INB, EN, PSAVE)	I_{IH}	$V_{IO}=1.6V\sim 5.5V$	-	-	1	μs
Input “L” level current (INA, INB)	I_{IL}		-1	-	-	μs
Input terminal pullup register (EN, PSAVE)	R_{PU}		50	100	200	$k\Omega$
VIO input “H” level voltage (VIO)	V_{IOH}	$V_C=3.3V, V_M=15V, INA=’H’, INB=’L’, EN=’H’$ $V_{IO}: 0V \Rightarrow 1.1V$	1.1	-	-	V
VIO input “L” level voltage (VIO)	V_{IOL}	$V_C=3.3V, V_M=15V, INA=’H’, INB=’L’, EN=’H’$ $V_{IO}: 3.3V \Rightarrow 0.3V$	-	-	0.3	V

Note 7. Not tested under mass-production.

Note 8. Refer [Figure 3](#).

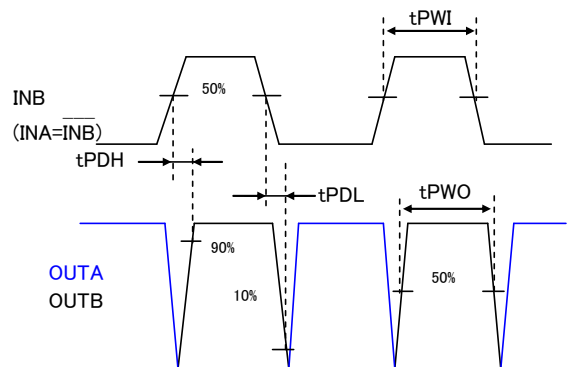


Figure 3. Time chart of propagation of delay time and pulse width

10. Descriptions

10.1 Control Logic

The relations of the input and output of each mode are as follows.

Table 1. Input and Output relations

PSAVE	EN	Input		Output		Motion
		INA	INB	OUTA	OUTB	
L	H	L	L	Z	Z	Standby (Idling)
L	H	L	H	L	H	Reverse
L	H	H	L	H	L	Forward
L	H	H	H	L	L	Break (Stop)
L	L	X	X	L	L	Stop (OSC and charge pump operation)
H	X	X	X	Z	Z	Power save (Note 9)

Note 9. TSD/UVLO/VREF/OSC/Charge pump are shut down.

Note 10. Input terminal is handled as “L” fixation when VIO is not input, OUTA/OUTB are “L” condition as same as PSAVE=”L” and EN=”L”.

10.2 Basic Architecture of the Motor Driver

The AP1013CEN places N-channel LDMOSFET on both sides of high side and low side in the output circuit and realize small package. High side MOSFET is driven by VG. VG=VM+VC is generated with a charge pump. VG reaches the targeted level at the time of the charge pump setup within 0.36ms (typ). Low side MOSFET is driven by VC.

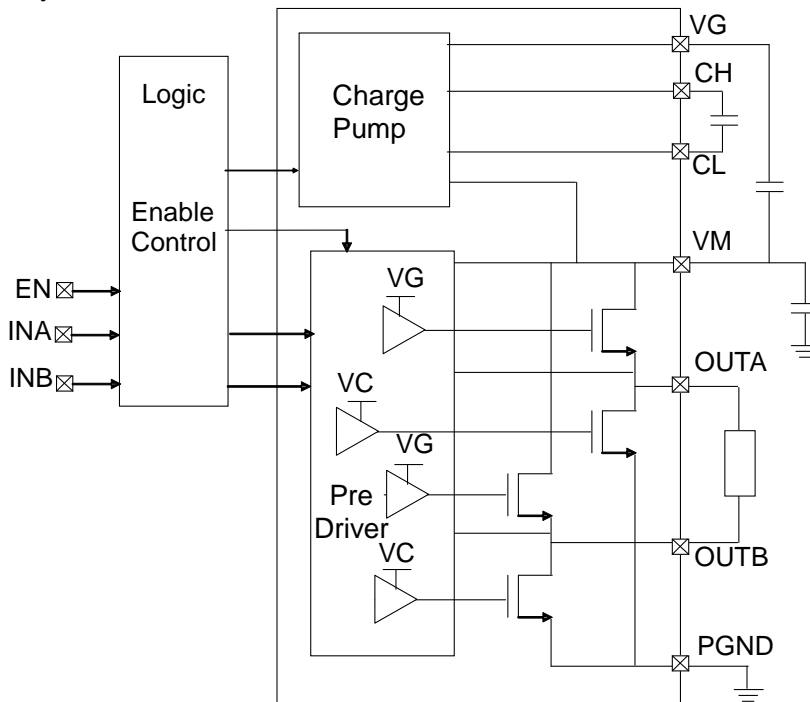


Figure 4. Motor driver part equivalent circuit

The OSC block supplies a drive pulse to a charge pump. The logic of input interface is operated by logic power supply VIO. The input interface does not work until VIO is input, and handled as “L” fixation.

10.3 Protection Circuits

The AP1013CEN has penetration current prevention, thermal shut down and under voltage detection circuits.

- Penetration current prevention circuit

MOSFET turns off both of high side and low side during the dead time period when penetration current prevention circuit operates. During this period, either body diode is turn on depends on the direction of the current. Figure 5 shows an example when the AP1013CEN drives the output from “L” to “H” in. (a) shows the case that current flows from external load to the AP1013CEN, (b) shows the case that current flows from the AP1013CEN to external load

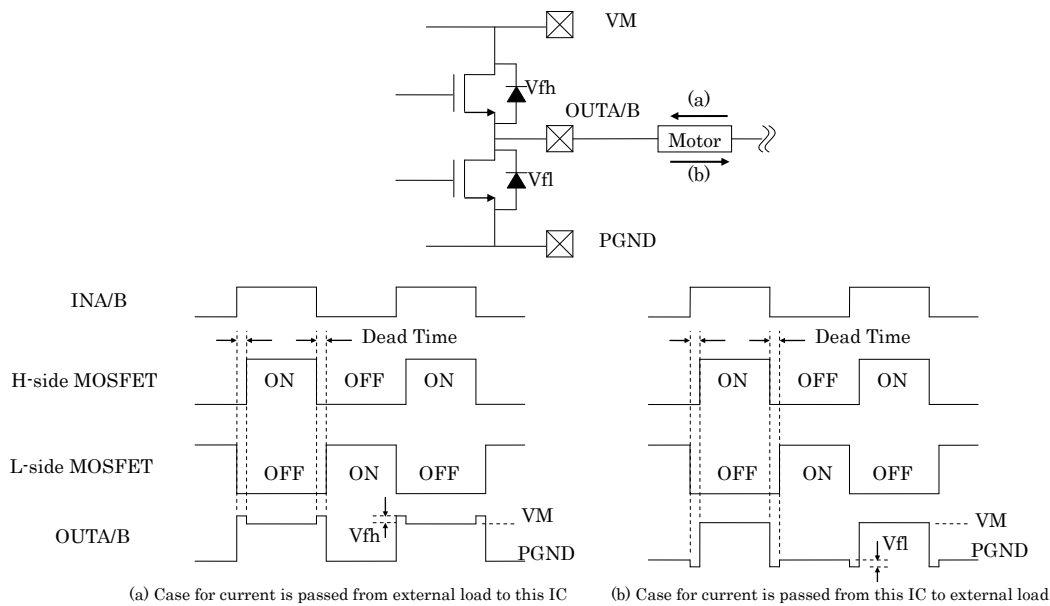


Figure 5. Difference in output terminal by load current direction

- Thermal Shut Down

The AP1013CEN prevents destruction due to the self-heat up by making OUTA and OUTB output Hi-Z as soon as abnormal high temperature is detected. The AP1013CEN restarts as soon as temperature becomes lower than the bottom detection threshold.

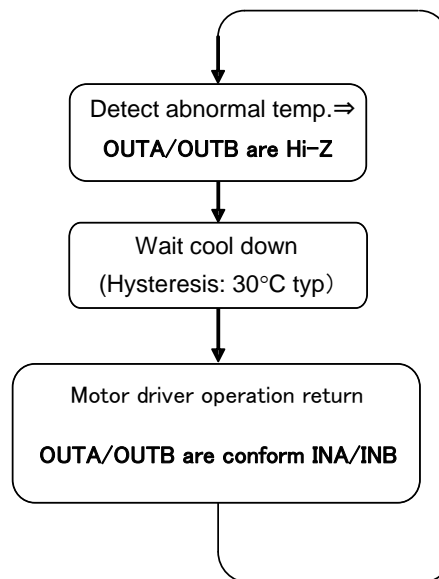


Figure 6. Detection of abnormal heat up and return operation

11. Recommended External Circuits

■ Recommended External Circuit

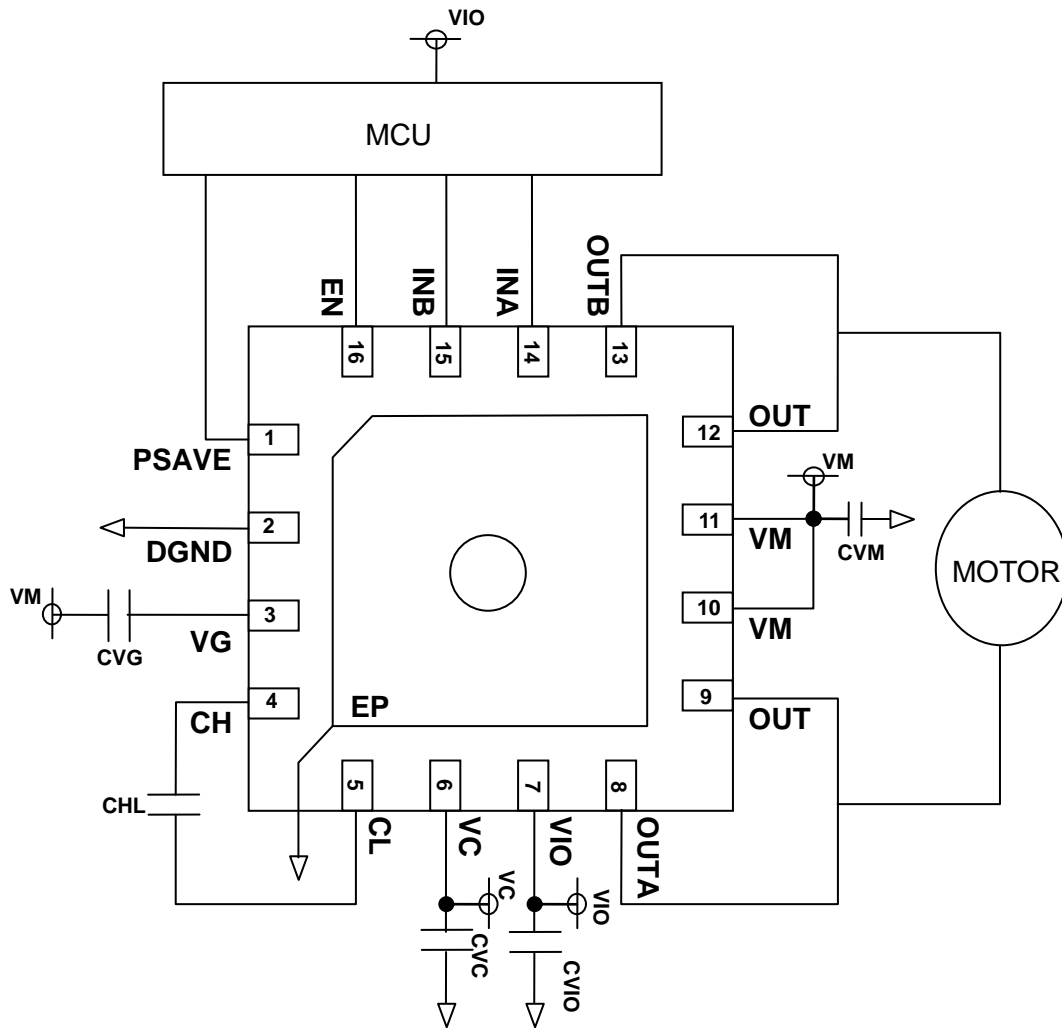


Figure 7. External circuit example

■ Parts List

Table 2. Recommended external components example

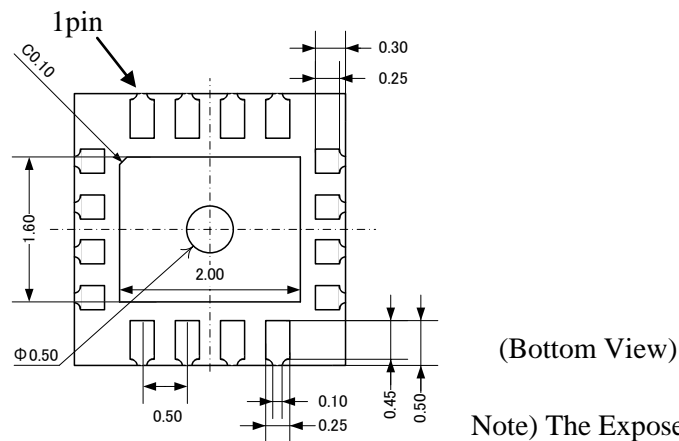
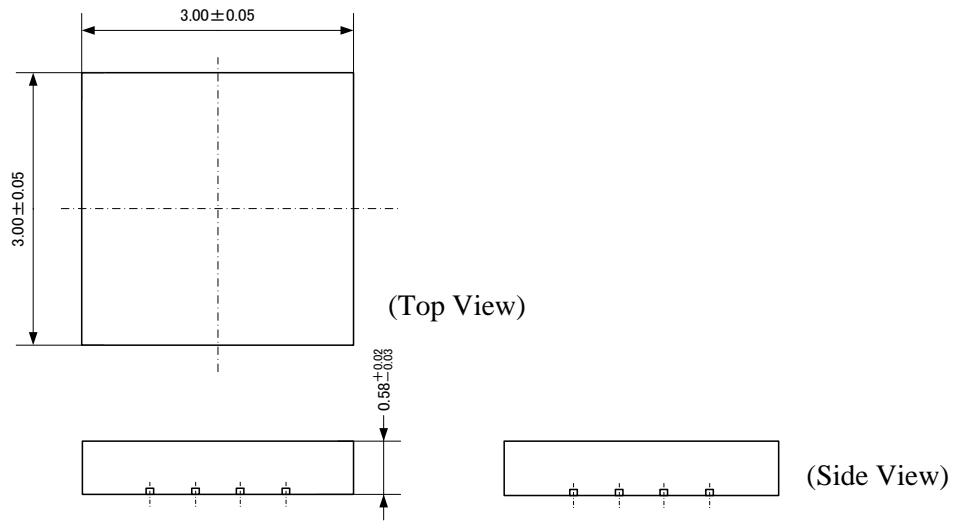
Items	Symbol	min	typ	max	Unit	Note
Motor driver power supply connection decoupling capacitor	CVM	1.0	-	-	uF	Please confirm it with application board appropriately.
Control power supply connection bypass capacitor	CVC	0.1	1.0	-	uF	Please confirm it with application board appropriately.
Logic input terminal power supply connection bypass capacitor	CVIO	0.1	1.0	-	uF	Please confirm it with application board appropriately.
Charge pump capacitor1	CVG	0.047	0.1	0.22	uF	Please confirm it with application board appropriately.
Charge pump capacitor2	CHL	0.047	0.1	0.22	uF	Please confirm it with application board appropriately.

Note 11. Please adjust the connecting capacitor of CVM, CVC and CVIO depending on the load current profile, the load capacitance, the line resistance and etc. with each application boards.

12. Package

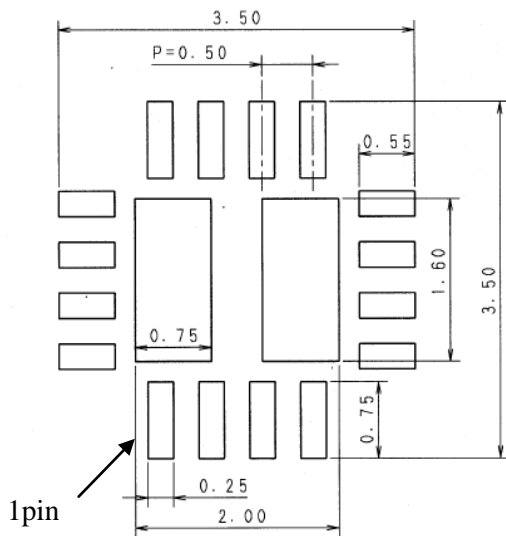
■ **Outline Dimensions**

• 16-pin QFN(Unit: mm)



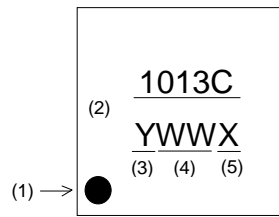
Note) The Exposed Pad is Power Ground.
The Exposed Pad is necessary soldered to PCB.

■ **Reference Foot Pattern**



Note) Please layout the foot pattern of Exposed Pad not to surround the steam beer of AP1013CEN. Please locate thermal via more than four for improve radiation.

■ **Marking**



- (1) Ipin Indication
- (2) Market No.
- (3) Year code (last 1 digit)
- (4) Week code
- (5) Management code

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
14/10/30	00	-	First edition
14/12/03	01	P10	Correct some sentences and Figure 5 in 10.3 Protection Circuits.

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