20.1 Absolute Maximum Ratings

Parameters	Min	Max	Unit
DC Supply voltage	-0.5	+6	V
DC input / output voltage	-0.5	Vdd + 0.5	V
DC input current	-20	+20	mA
Storage temperature	-40	+125	°C
Lead temperature		+300	°C

Table 20-1: DC maximum ratings

20.2 DC Operating Conditions

Parameters	Min	Max	Unit
DC Supply voltage	+2.7	+5.5	V
DC input / output voltage	0	Vdd	V
DC input current	-15	+15	mA
Operating temperature	0	+70	°C

Table 20-2: DC operating conditions

20.3 DC Characteristics

All characteristics are specified at Vdd = 3.0 to 3.6 volts and Vss = 0 volts over an operating temperature of 0°C to +70°C.

Symbol	Parameter	Min	Max	Unit	Conditions
VIH	CMOS input high voltage	0.7 x Vdd	Vdd + 0.3	V	
VIL	CMOS input low voltage	-0.3	0.2 x Vdd	V	
VT+	Schmitt trigger positive going threshold	1.52	2.26	V	
VT-	Schmitt trigger negative going threshold	0.72	1.29	V	
Vhst	Schmitt trigger hysteresis	0.64	1.13	V	VIL to VIH
VOH	CMOS output high voltage	Vdd - 0.1		V	IOH = 0.8 mA
	Standard drive output	Vdd - 1.0		V	IOH = 4 mA
	Medium drive output	Vdd - 1.0		V	IOH = 6 mA
	High drive output	Vdd - 1.0		V	IOH = 12 mA
	Very high drive output	Vdd - 1.0		V	IOH = 24 mA
VOL	CMOS output low voltage		0.1	V	IOL = -0.8 mA
	Standard drive output		0.5	V	IOL = -4 mA
	Medium drive output		0.5	V	IOL = -6 mA
	High drive output		0.5	V	IOL = -12 mA
	Very high drive output		0.5	V	IOL = -24 mA
IIN	Input leakage current	-10	+10	µA	VIN = VDD or GND
IOZ	Output Tri-state leakage current	-10	+10	µA	VOUT = VDD or GND
CIN	Input capacitance		5	pF	
COUT	Output capacitance		5	pF	
CI/O	Transceiver capacitance		5	pF	

Table 20-3: DC characteristics

Preliminary

Symbol	Parameter	Min	Max	Unit	Conditions
$IDD_{startup}$	Startup current consumption		100	µA	Initial 100 mSec from power up, 32 KHz oscillator not stable, POR signal at VIL, all other I/O static, VIH = VDD ± 0.1V, VIL = GND ± 0.1V
$IDD_{standby}$	Standby current consumption		50	µA	Just 32 KHz oscillator running, all other I/O static, VIH = VDD ± 0.1V, VIL = GND ± 0.1V
IDD_{idle}	Idle current consumption		5	mA	Both oscillators running, CPU static, LCD refresh active, VIH = VDD ± 0.1V, VIL = GND ± 0.1V
$IDD_{operating}$	Operating current consumption		30	mA	All system active, running typical program
$VDD_{standby}$	Standby supply voltage	2.2		V	Minimum standby voltage for state retention and RTC operation only.

Table 20-3: DC characteristics

20.4 AC Characteristics

All characteristics are specified at Vdd = 3.0 to 3.6 volts and Vss = 0 volts over an operating temperature of 0°C to +70°C.

Symbol	Parameter	Min	Max	Unit
T1	Falling CS to data bus Hi-Z	0	25	nS
T2	Address change to valid write data	0	35	nS
T3	DATA in to falling EXPCLK setup time	18		nS
T4	DATA in to falling EXPCLK hold time	0		nS
T5	EXPRDY to falling EXPCLK setup time	18		nS
T6	Falling EXPCLK to EXPRDY hold time	0	50	nS
T7	Rising nMWE to data nvalid hold time	5		nS
T8	Data valid to falling nMWE setup time	15		nS
T9	Row address to falling nCAS setup time	18		nS
T10	Falling nRAS to row address hold time	25		nS
T11	Column address to falling nCAS setup time	2		nS
T12	Falling nCAS to column address hold time	25		nS
T13	Write data valid to falling nCAS setup time	2		nS
T14	Write data valid from falling nCAS hold time	50		nS
T15	LCD CL2 low time	80	3475	nS
T16	LCD CL2 high time	80	3475	nS
T17	LCD rising CL2 to rising CL1 delay	0	25	nS
18	LCD falling CL1 to rising CL21	80	3475	nS
T19	LCD CL1 high time	80	3475	nS
T20	LCD falling CL1 to falling CL2	200	6950	nS
T21	LCD falling CL1 to frm toggle	300	10425	nS
T22	LCD falling CL1 to m toggle	-10	20	nS
T23	LCD rising CL2 to display data change	-10	20	nS

Table 20-4: AC Characteristics

Symbol	Parameter	Min	Max	Unit
Textrd	zero wait state memory read access time		70	nS
Texwr	zero wait state memory write access time		70	nS
Trc	DRAM cycle time		150	nS
Trac	Access time from RAS		70	nS
Trp	RAS precharge time		70	nS
Tcas	CAS pulse width		20	nS
Tcp	CAS precharge in page mode		12	nS
Tpc	Page mode cycle time		45	nS
Tcsa	CAS setup time		15	nS
Tras	RAS pulse width		80	nS

Table 20-5: System memory device parameter requirements

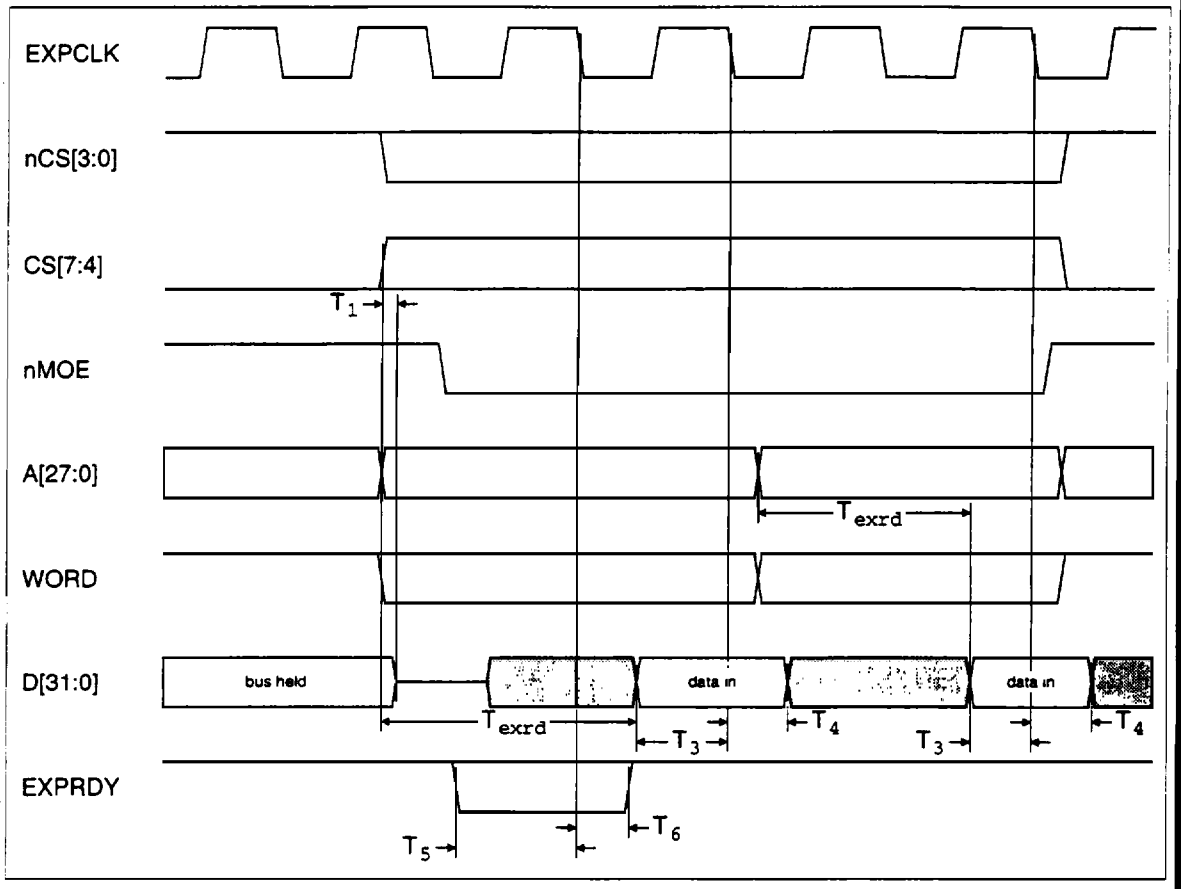

Figure 20-1: Expansion and ROM read timing

Notes

1 Texrd = 70nS for maximum wait states and a main oscillator frequency of 18.432 MHz. This time can be extended by integer multiples of the clock period (54nS), by either driving **EXPRDY** LOW or by by programming a number of wait states. **EXPRDY** is sampled on the falling edge of **EXPCLK** before the data transfer. If LOW at this point the transfer is delayed by one clock period where **EXPRDY** is sampled again. **EXPCLK** need not be referenced when driving **EXPRDY** but is shown for clarity.

2 Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states.

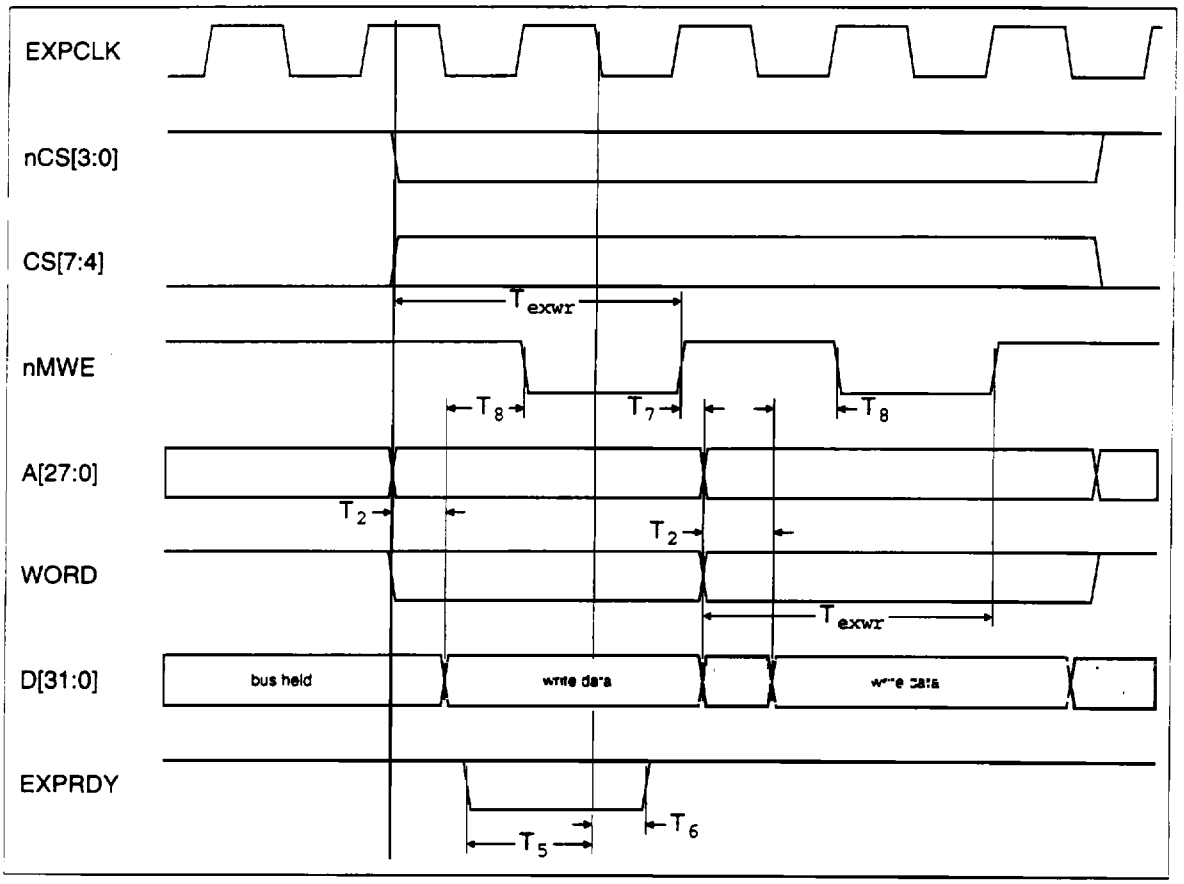

Figure 20-2: Expansion and ROM write timing

Notes

1 Texwr = 70nS max for zero wait states. This time can be extended by integer multiples of the clock period (54 nS), by either driving **EXPRDY** LOW or by programming a number of wait states. **EXPRDY** is sampled on the falling edge of **EXPCLK** before the data tansfer. If LOW at this point, the transfer is delayed by one clock period where **EXPRDY** is sampled again. **EXPCLK** need not be referenced when driving **EXPRDY** but is shown for clarity.

2 Consecutive writes with sequential access enabled are identical except that the sequential access wait state filed is used to determine the number of wait states.

3 Zero wait states for sequential writes is not supported, one state will automatically be added.

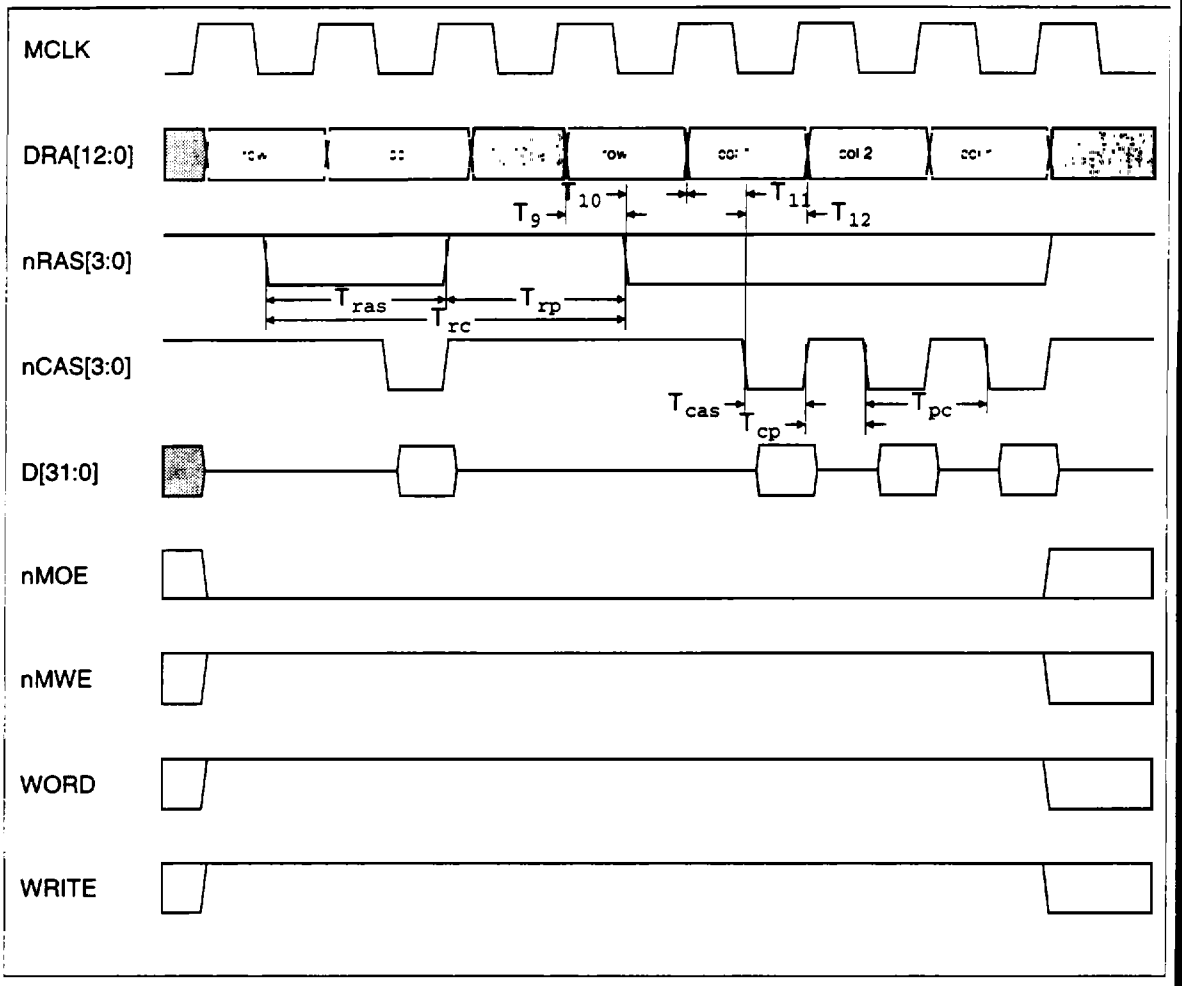

Figure 20-3: DRAM read cycles

Notes

1. Trc (Read cycle time) = 150nS max
2. Trac (Read access time from RAS) = 70nS max
3. Trp (RAS precharge time) = 70nS max
4. Tcas (CAS pulse width) = 20nS max
5. Tcp (CAS precharge in page mode) = 12nS max
6. Tpc (page mode cycle time) = 45nS min at max
7. Word reads shown, for byte reads only one of **CAS[3:0]** will be active, **CAS[0]** for byte 0 etc.

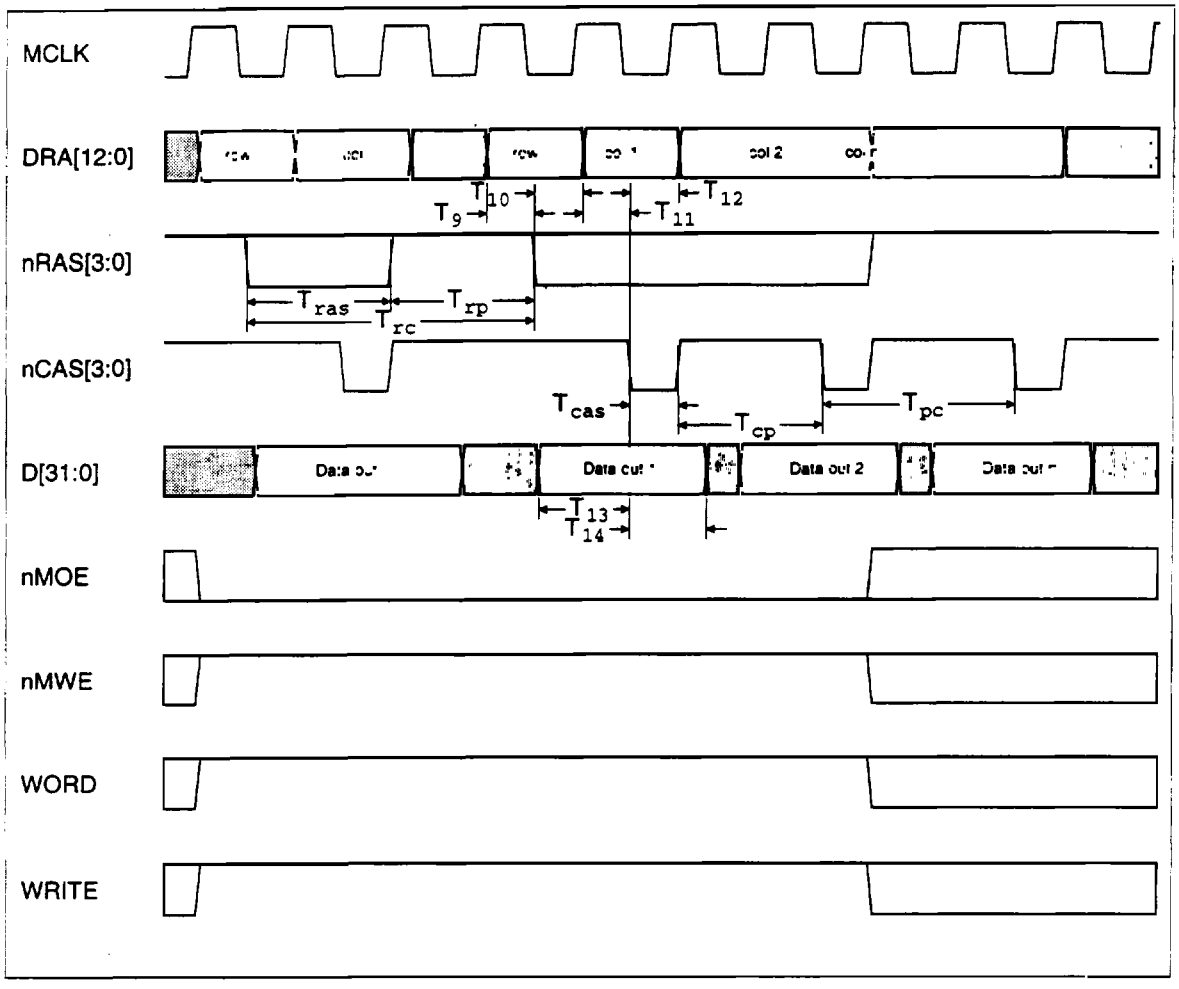

Figure 20-4: DRAM write cycles

Notes

1. Trc (Write cycle time) = 150nS max at **MCLK** = 18.432MHz
2. Trac (Write access time from RAS) = 70nS max at **MCLK** = 18.432MHz
3. Trp (RAS precharge time) = 70nS max at **MCLK** = 18.432MHz
4. Tcas (CAS pulse width) = 20nS max at **MCLK** = 18.432MHz
5. Tcp (CAS precharge in page mode) = 66nS max at **MCLK** = 18.432MHz
6. Tpc (page mode cycle time) = 45nS max at **MCLK** = 18.432MHz
7. Word writes shown, for byte writes only one off **CAS[3:0]** will be active, **CAS[0]** for byte 0 etc.

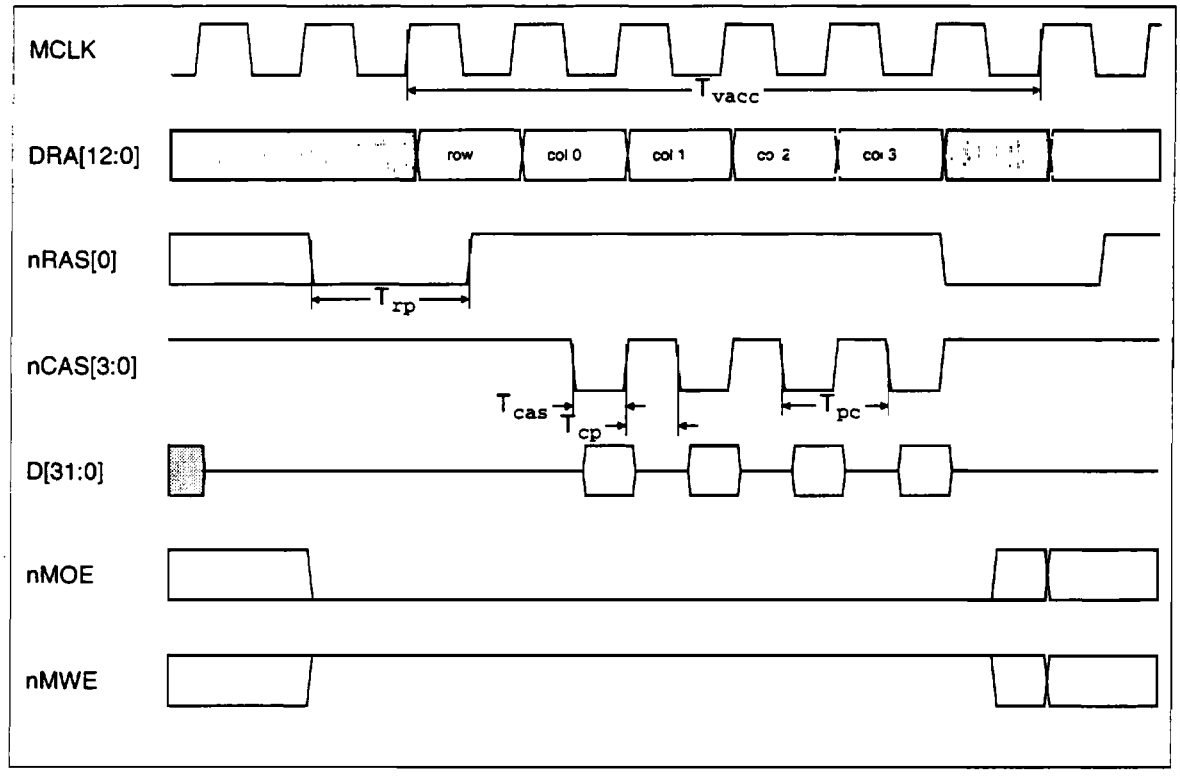

Figure 20-5: Video quad word read

Notes

1 Timings are the same as page mode word reads

2 Tvacc (video access cycle time) = 326nS at **MCLK** = 18.432 MHz

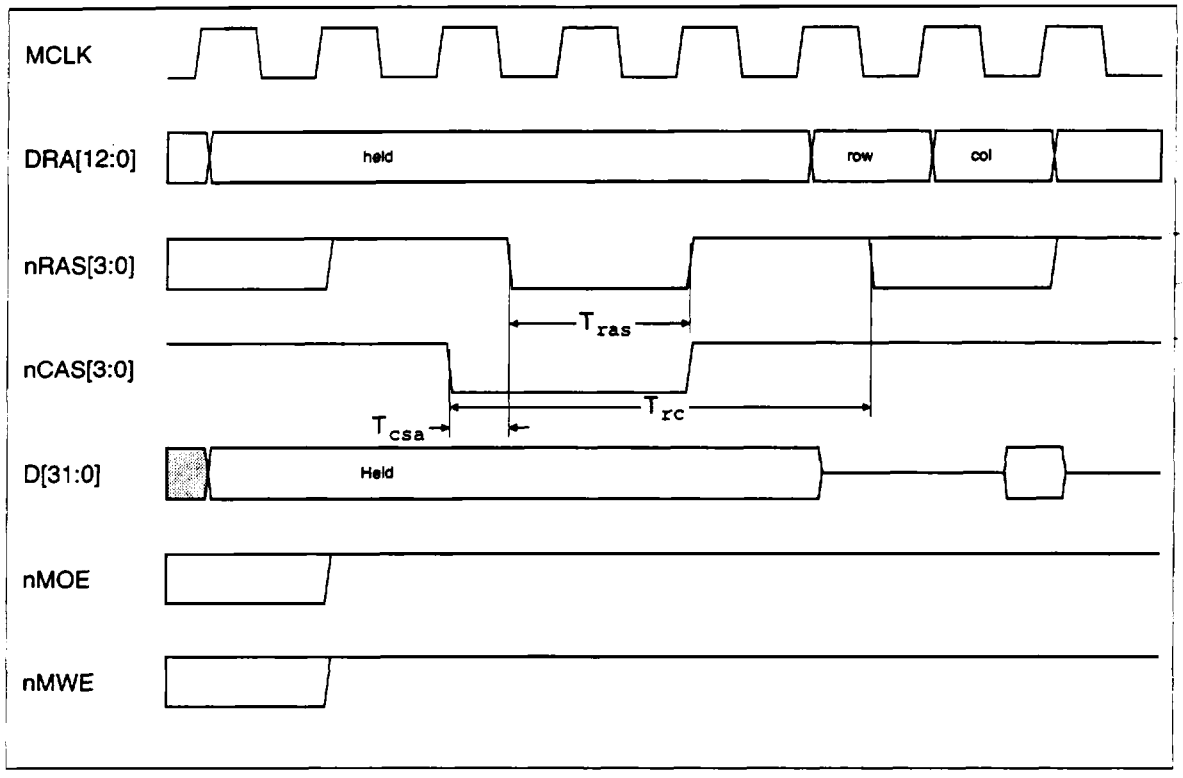

Figure 20-6: DRAM CAS before RAS refresh cycle

Notes

1. Tcsa (CAS set-up time) = 25nS min at **MCLK** = 18.432MHz
2. Tras (RAS pulse width) = 70nS min at **MCLK** = 18.432MHz
3. Trc (Cycle time) = 150nS min at **MCLK** = 18.432MHz
4. When DRAM's are placed in self refresh (entering standby), the same timings apply except that Tras is extended indefinitely.

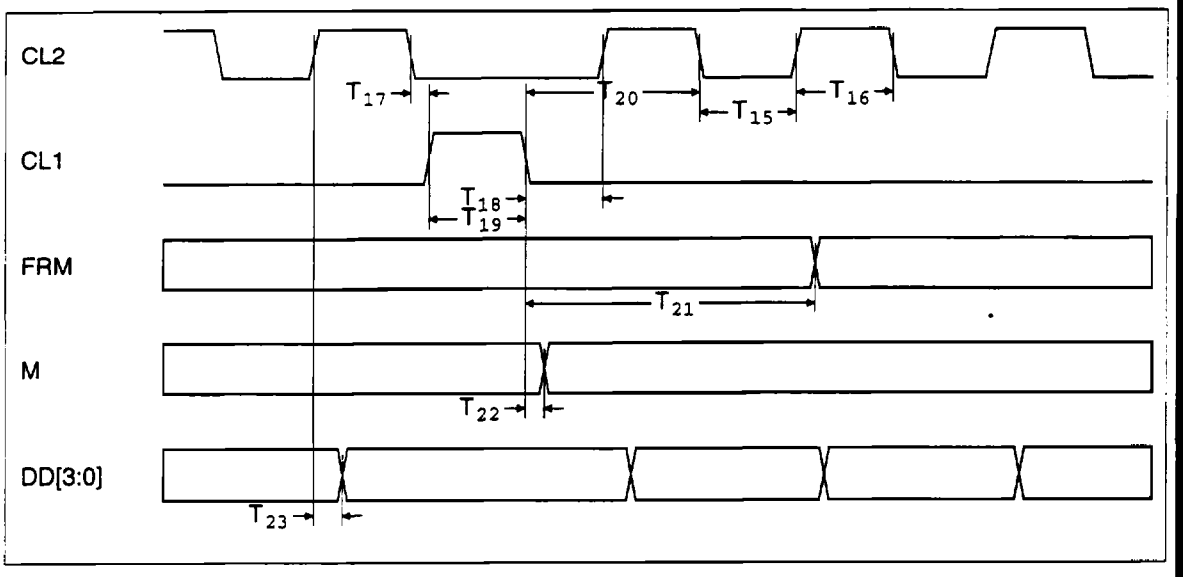

Figure 20-7: LCD controller timing

Notes

1 ⊃*Figure 20-7: LCD controller timing* shows the end of a line.

2 If **FRM** is HIGH during the **CL1** pulse, this marks the first line in the display.

3 **CL2** LOW time is doubled during the **CL1** high pulse.