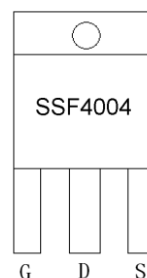
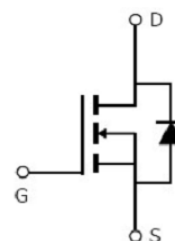


**Main Product Characteristics**

$V_{DSS}$	40V
$R_{DS(on)}$	2.3m $\Omega$ (typ.)
$I_D$	180A <sup>①</sup>


**TO-220**

**Marking and Pin Assignment**

**Schematic Diagram**
**Features and Benefits**

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


**Description**

SSF4004S utilizes the latest processing techniques to achieve high cell density and reduces on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

**Absolute Max Rating**

Symbol	Parameter	Max.	Units
$I_D$ @ TC = 25°C	Continuous Drain Current, $V_{GS}$ @ 10V(Silicon Limited)	180 <sup>①</sup>	A
$I_D$ @ TC = 100°C	Continuous Drain Current, $V_{GS}$ @ 10V	120 <sup>①</sup>	
$I_D$ @ TC = 25°C	Continuous Drain Current, $V_{GS}$ @ 10V(Package Limited)	75	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	710	
$P_D$ @TC = 25°C	Power Dissipation <sup>③</sup>	200	W
	Linear Derating Factor	1.3	W/°C
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=0.3mH	960	mJ
$I_{AS}$	Avalanche Current @ L=0.3mH	80	A
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C

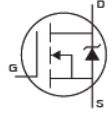
## Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.75	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ( $t \leq 10s$ ) ④	—	62	$^{\circ}C/W$

## Electrical Characteristics @ $T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	2.3	4	m $\Omega$	$V_{GS}=10V, I_D = 75A$
		—	4.1	—		$T_J = 125^{\circ}C$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.1	—		$T_J = 125^{\circ}C$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	50		$T_J = 125^{\circ}C$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
$Q_g$	Total gate charge	—	278	—	nC	$I_D = 75A,$ $V_{DS}=32V,$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source charge	—	41	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	119	—		
$t_{d(on)}$	Turn-on delay time	—	71	—	ns	$V_{GS}=10V, V_{DS} =20V,$ $R_{GEN}=3\Omega, I_D =1.3A$
$t_r$	Rise time	—	34	—		
$t_{d(off)}$	Turn-Off delay time	—	131	—		
$t_f$	Fall time	—	106	—		
$C_{iss}$	Input capacitance	—	12968	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output capacitance	—	940	—		$V_{DS} = 40V$
$C_{rss}$	Reverse transfer capacitance	—	905	—		$f = 1MHz$

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	75 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	750	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$I_S=30A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	—	28	—	nS	$T_J = 25^{\circ}C, I_F = 70A,$
$Q_{rr}$	Reverse Recovery Charge	—	20	—	nC	$di/dt = 100A/\mu s$

## Test circuits and Waveforms

**EAS Test Circuit**

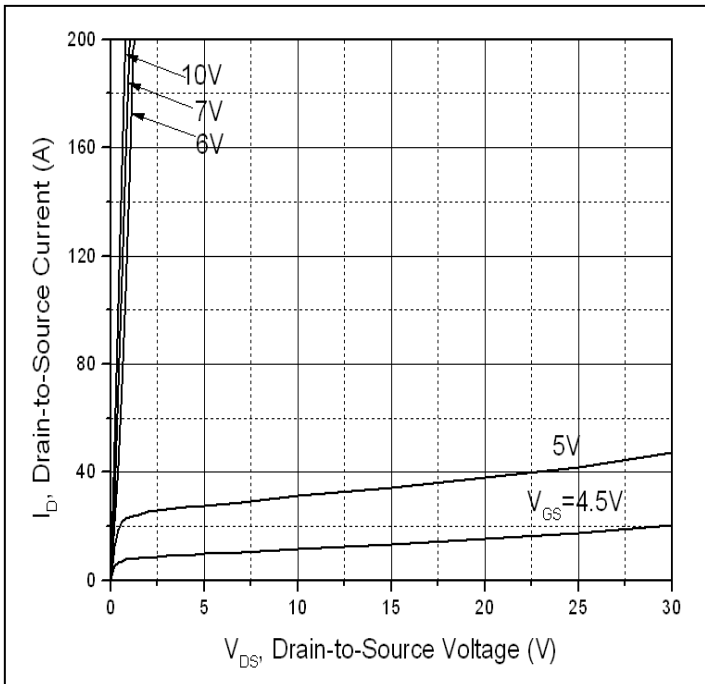
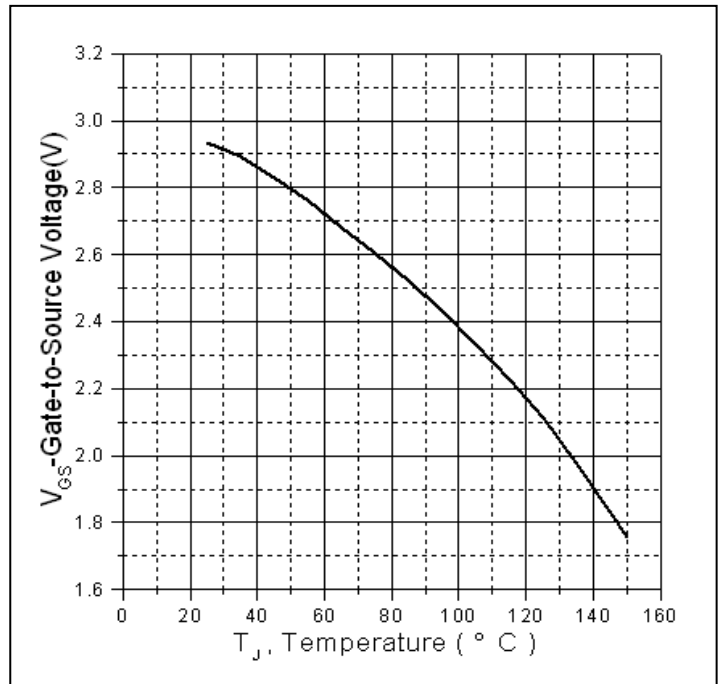
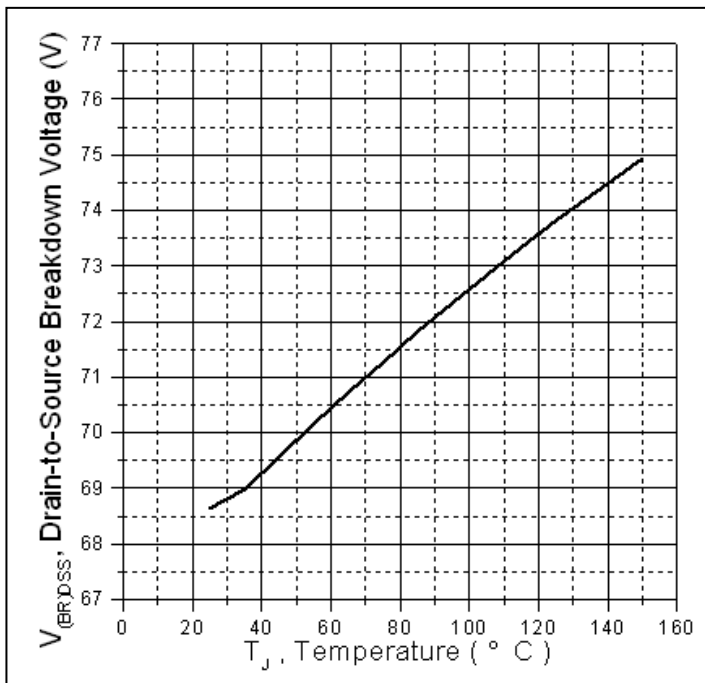
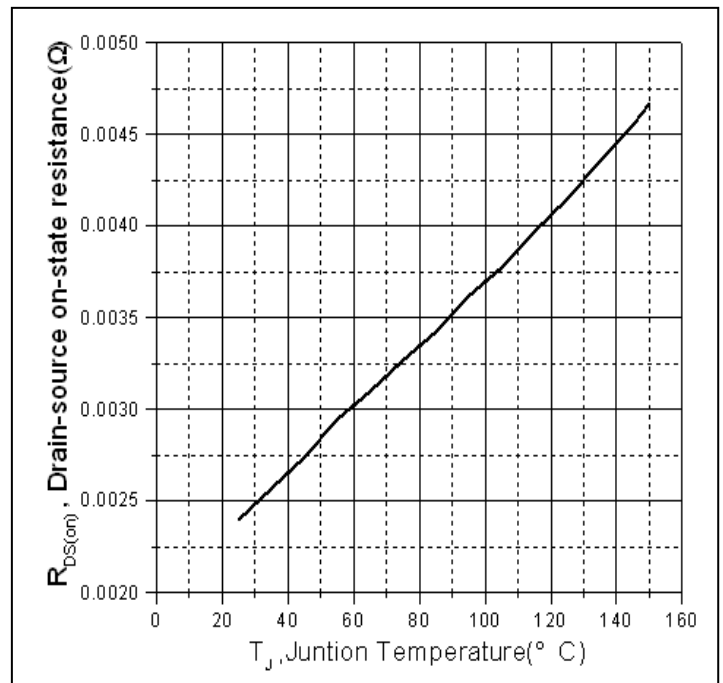
**Gate charge test circuit**

**Switching Time Test Circuit**

**Switching Waveforms**


### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$

**Typical electrical and thermal characteristics**

**Figure 1. Typical Output Characteristics**

**Figure 2. Gate to source cut-off voltage**

**Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature**

**Figure 4. Normalized On-Resistance Vs. Case Temperature**

Typical electrical and thermal characteristics

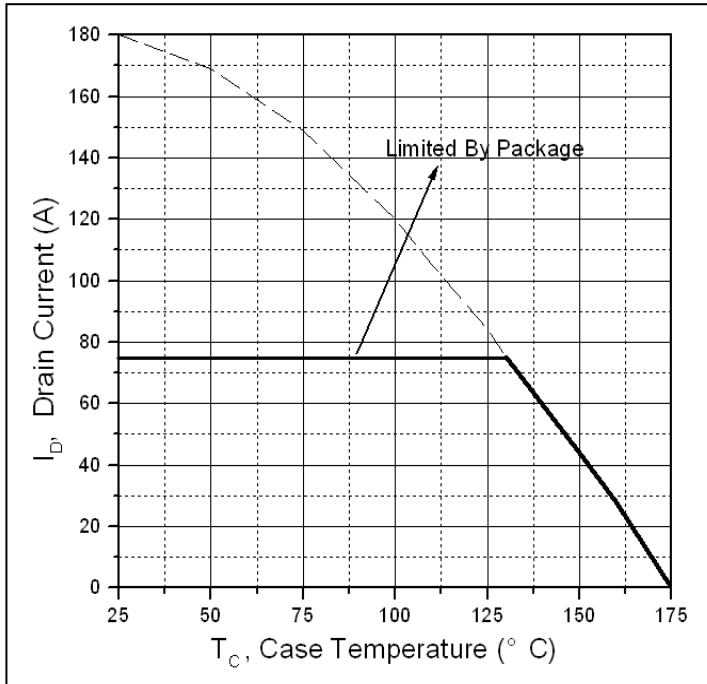


Figure 5. Maximum Drain Current Vs. Case Temperature

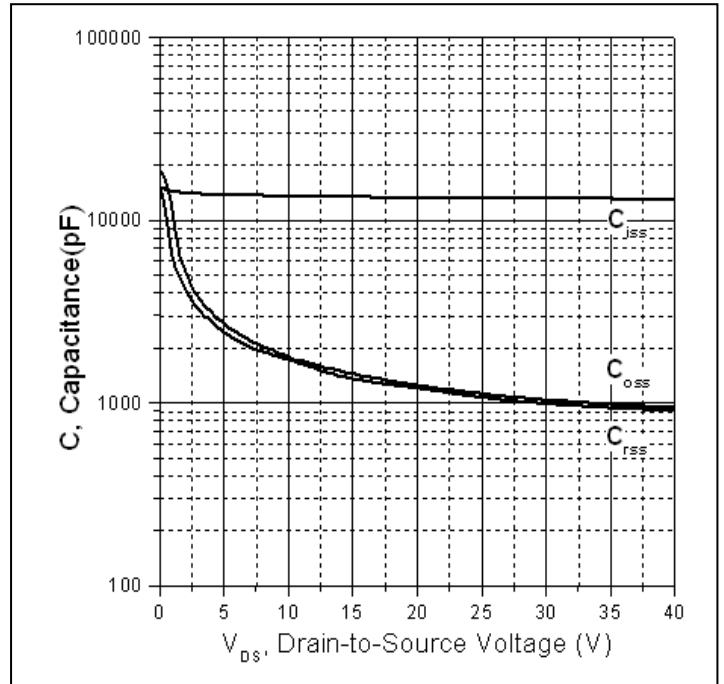


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

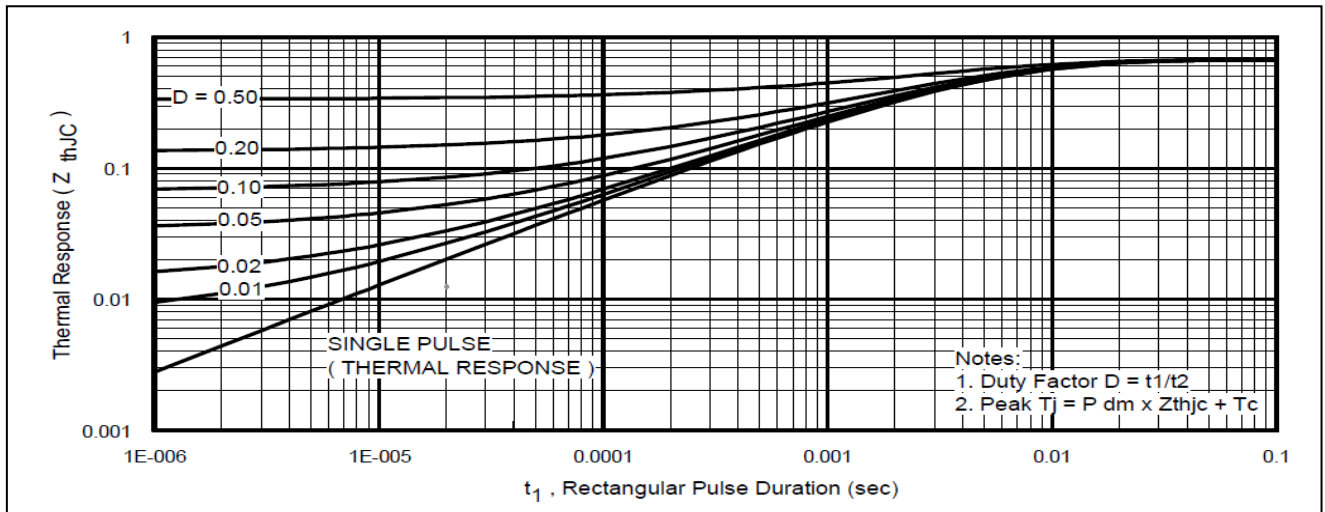
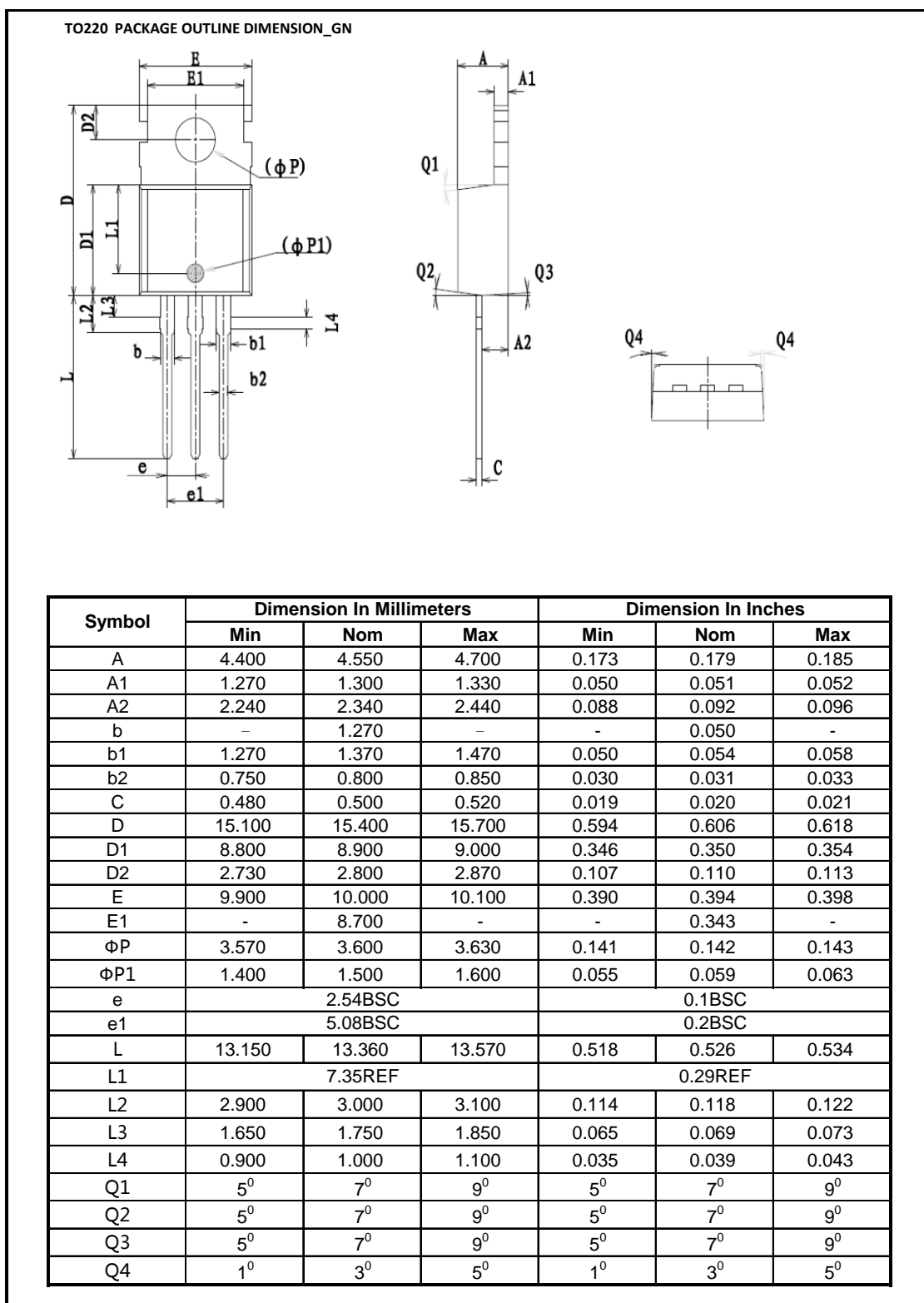


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Mechanical Data:**


**Ordering and Marking Information**

<b>Device Marking: SSF4004</b> <div style="text-align: center;"> <b>Package (Available)</b>  <b>TO-220</b>  <b>Operating Temperature Range</b>  <b>C : -55 to 175 °C</b> </div>
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**Devices per Unit**

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/VR$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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