TO-220AB
IRFB7440GPbF

Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free
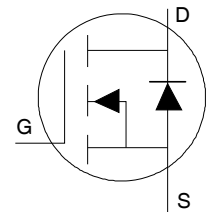
V_{DSS}		**40V**
$R_{DS(on)}$	**typ.**	**2.0mΩ**
	max.	**2.5mΩ**
I_D		**208A①**
$I_{D\ (Package\ Limited)}$		**120A**

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB7440GPbF	TO-220	Tube	50	IRFB7440GPbF
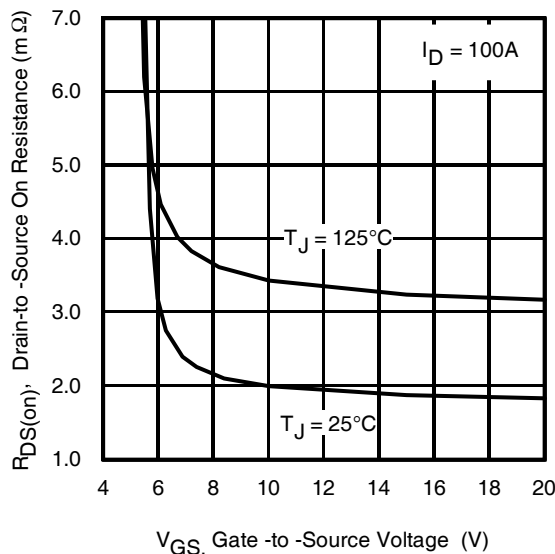
Fig 1. Typical On-Resistance vs. Gate Voltage
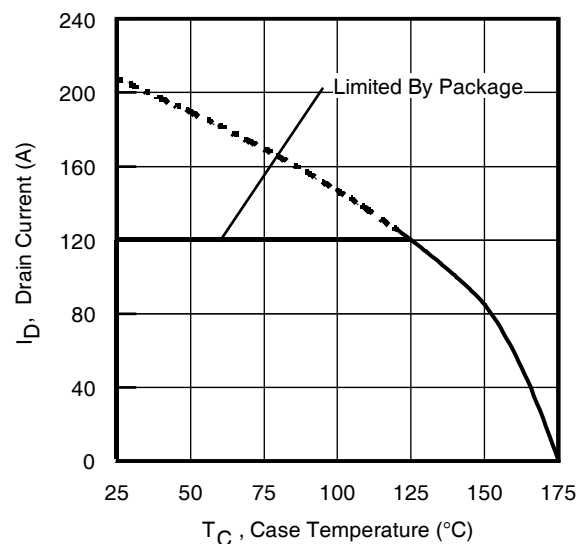
Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ 10V	208 [1]	
I_D @ $T_C = 100°C$	Continuous Drain Current, V_{GS} @ 10V	147 [1]	
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	120	A
I_{DM}	Pulsed Drain Current [2]	772	
P_D @ $T_C = 25°C$	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf· in (1.1N· m)	

Avalanche Characteristics

Symbol	Parameter	Max.	Units
$E_{AS (Thermally\ limited)}$	Single Pulse Avalanche Energy [3]	238	mJ
$E_{AS (tested)}$	Single Pulse Avalanche Energy Tested Value [9]	298	
I_{AR}	Avalanche Current [2]	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy [2]		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case [8]	———	0.72	
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	———	°C/W
$R_{\theta JA}$	Junction-to-Ambient	———	62	

Static @ T_J = 25°C (unless otherwise specified)

| Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	$V_{GS} = 0V$, $I_D = 250µA$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.035	——	V/°C	Reference to 25°C, $I_D = 5.0mA$ [2]
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	2.0	2.5	mΩ	$V_{GS} = 10V$, $I_D = 100A$ [5]
		——	3.0	——	mΩ	$V_{GS} = 6.0V$, $I_D = 50A$ [5]
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}$, $I_D = 100µA$
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	µA	$V_{DS} = 40V$, $V_{GS} = 0V$
		——	——	150		$V_{DS} = 40V$, $V_{GS} = 0V$, $T_J = 125°C$
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	——	——	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	——	2.6	——	Ω	
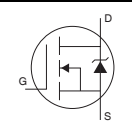
Notes:

[1] Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

[2] Repetitive rating; pulse width limited by max. junction temperature.

[3] Limited by T_{Jmax}, starting T_J = 25°C, L = 0.048mH
 R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.

[4] I_{SD} ≤ 100A, di/dt ≤ 1330A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

[5] Pulse width ≤ 400µs; duty cycle ≤ 2%.

[6] C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[7] C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[8] R_θ is measured at T_J approximately 90°C.

[9] This value determined from sample failure population, starting T_J = 25°C, L= 0.048mH, R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	88	——	——	S	V_{DS} = 10V, I_D = 100A
Q_g	Total Gate Charge	——	90	135	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	——	23	——		V_{DS} =20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	32	——		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	58	——		I_D = 100A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	24	——	ns	V_{DD} = 20V
t_r	Rise Time	——	68	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	115	——		R_G = 2.7Ω
t_f	Fall Time	——	68	——		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	——	4730	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	680	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	460	——		f = 1.0 MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	845	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑦
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	——	980	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions	
I_S	Continuous Source Current (Body Diode)	——	——	193	A	MOSFET symbol showing the integral reverse p-n junction diode.	
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	772	A		
V_{SD}	Diode Forward Voltage	——	0.9	1.3	V	T_J = 25°C, I_S = 100A, V_{GS} = 0V ⑤	
dv/dt	Peak Diode Recovery ④	——	6.8	——	V/ns	T_J = 175°C, I_S = 100A, V_{DS} = 40V	
t_{rr}	Reverse Recovery Time	——	24	——	ns	T_J = 25°C	V_R = 34V,
		——	28	——		T_J = 125°C	I_F = 100A
Q_{rr}	Reverse Recovery Charge	——	17	——	nC	T_J = 25°C	di/dt = 100A/µs ⑤
		——	20	——		T_J = 125°C	
I_{RRM}	Reverse Recovery Current	——	1.3	——	A	T_J = 25°C	
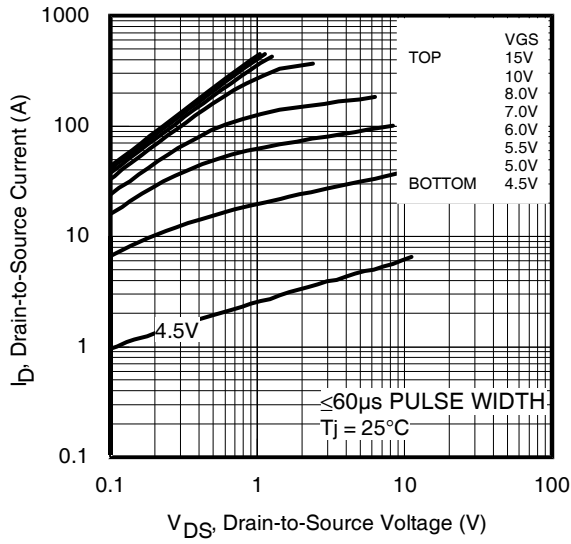
Fig 3. Typical Output Characteristics
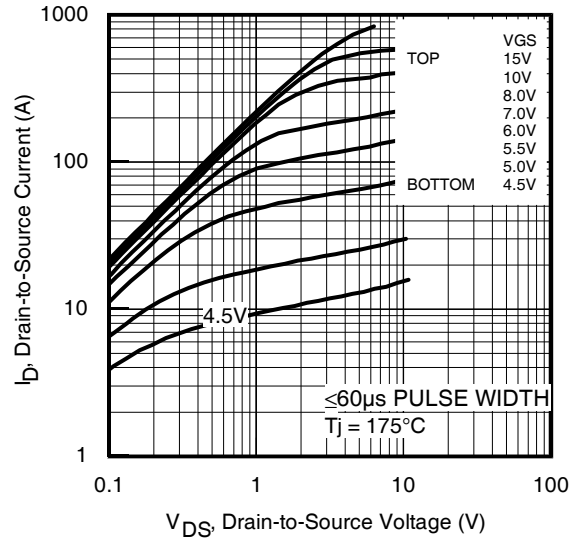
Fig 4. Typical Output Characteristics
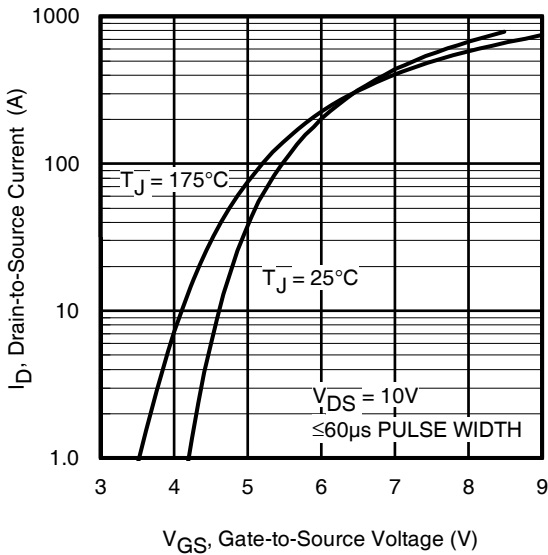
Fig 5. Typical Transfer Characteristics
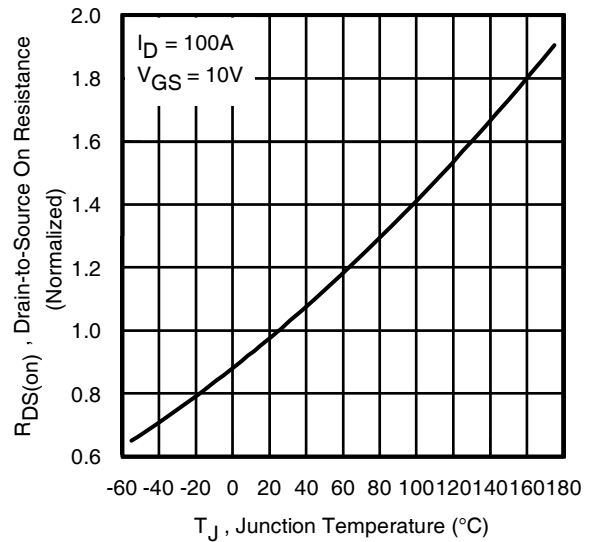
Fig 6. Normalized On-Resistance vs. Temperature
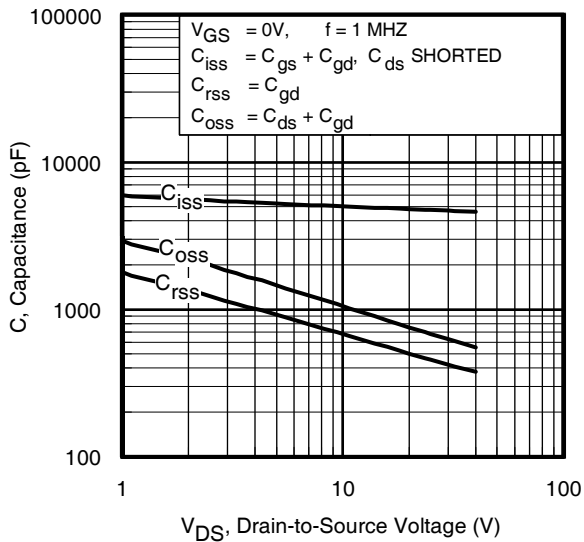
Fig 7. Typical Capacitance vs. Drain-to-Source Voltage
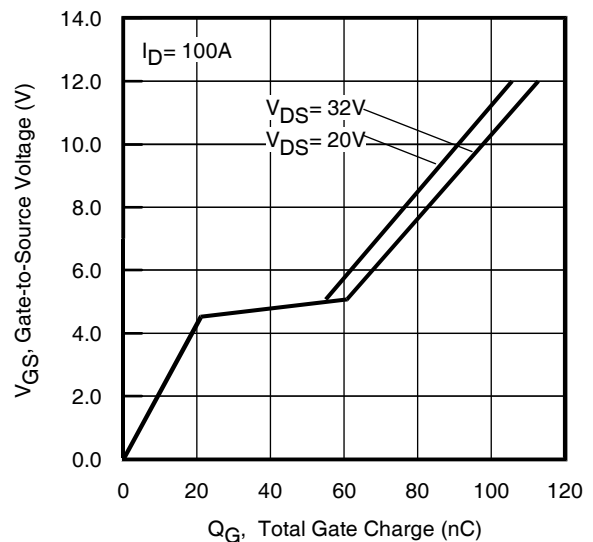
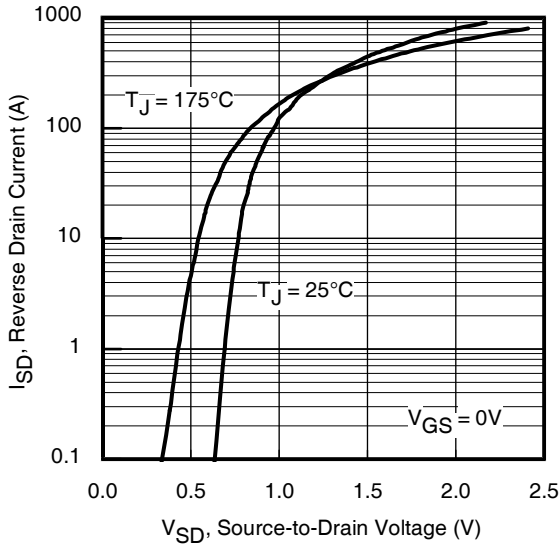**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage

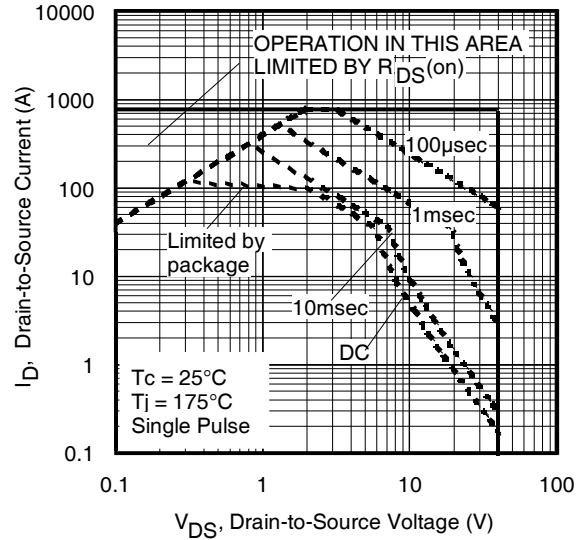**Fig 9.** Typical Source-Drain Diode Forward Voltage
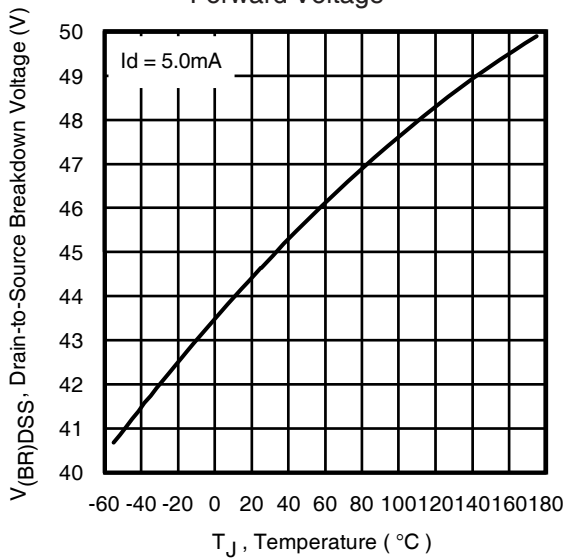

Fig 10. Maximum Safe Operating Area
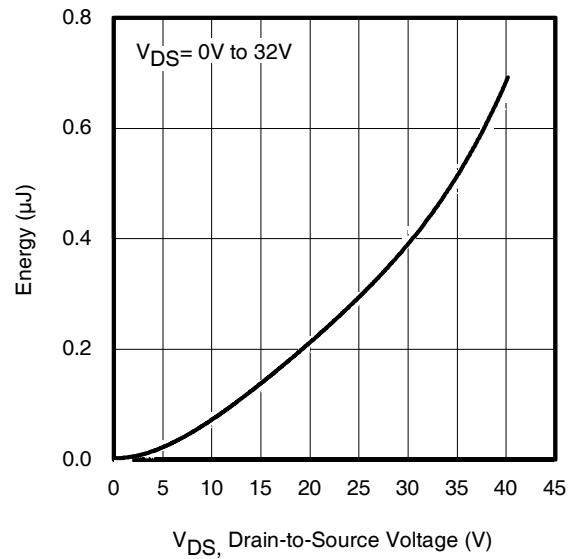

Fig 11. Drain-to-Source Breakdown Voltage

Fig 12. Typical C_{OSS} Stored Energy
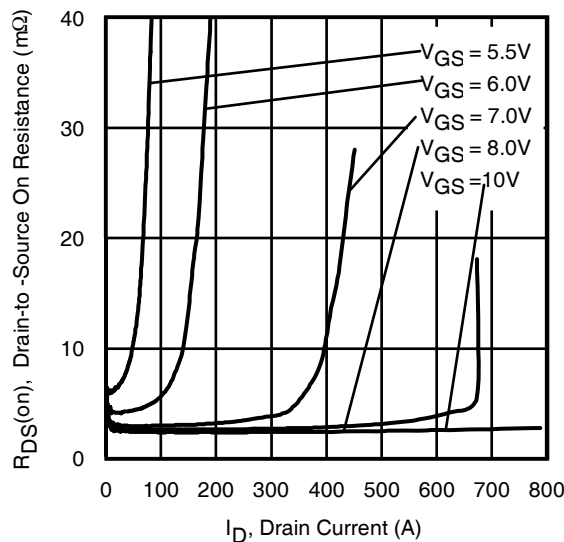
**Fig 13.** Typical On-Resistance vs. Drain Current
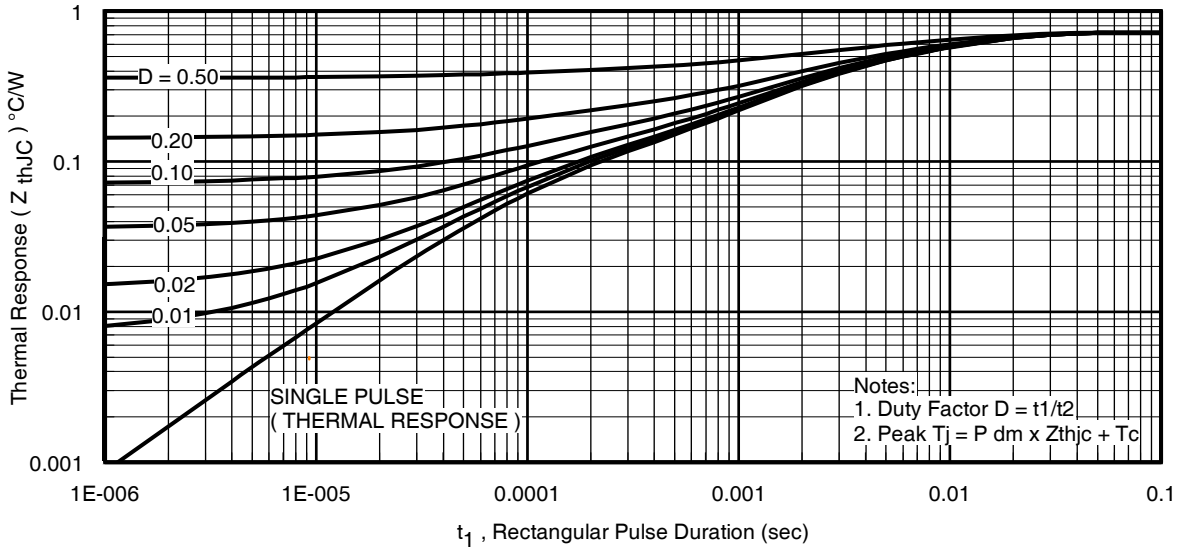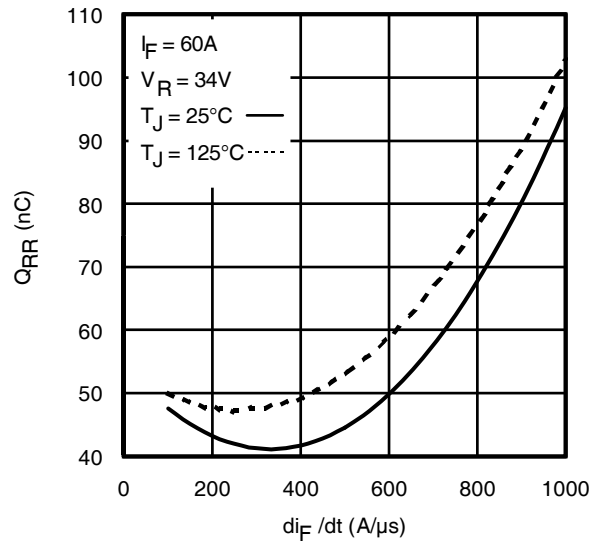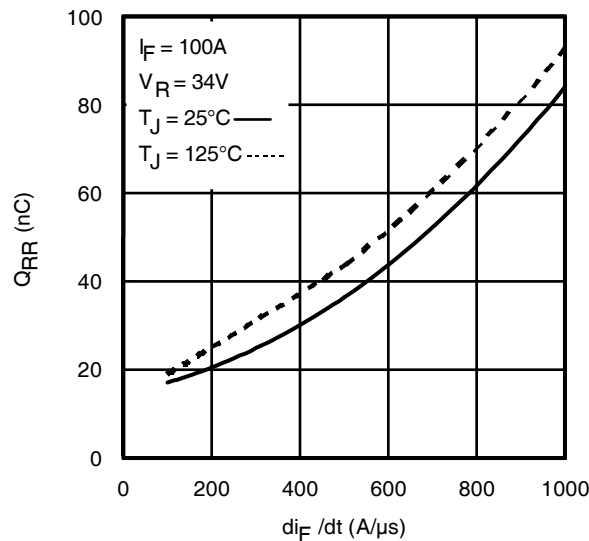
Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case
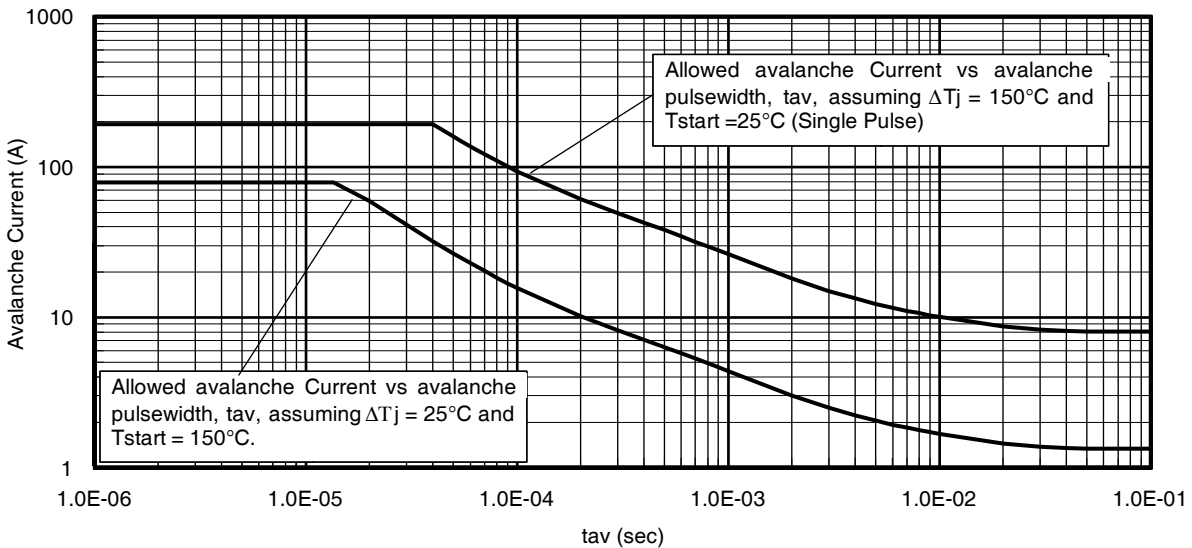
Fig 15. Typical Avalanche Current vs.Pulsewidth
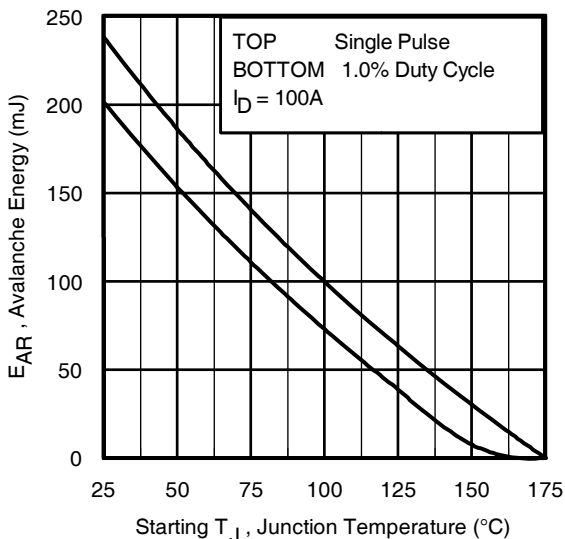
Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
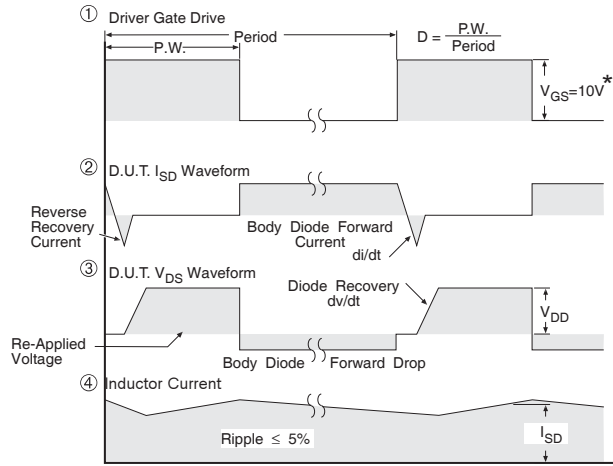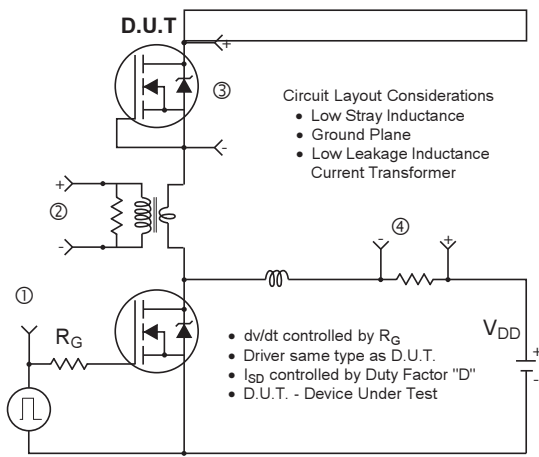**(For further info, see AN-1005 at www.irf.com)**
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$
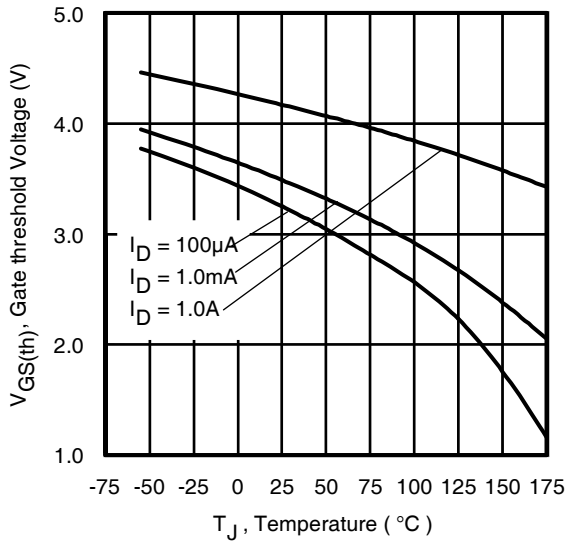
Fig 17. Threshold Voltage vs. Temperature
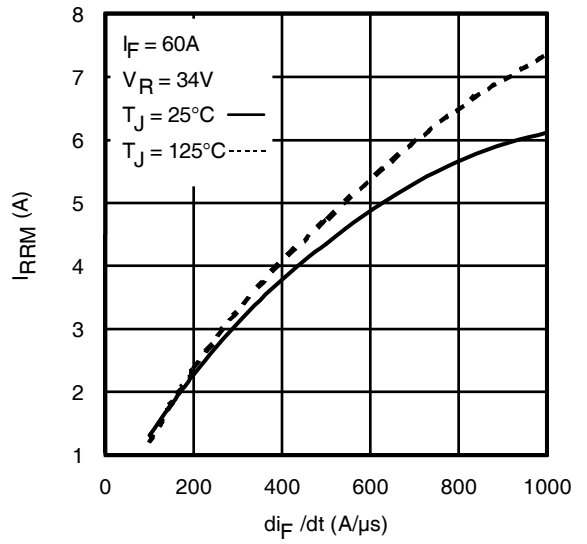
Fig. 18 - Typical Recovery Current vs. di$_f$/dt
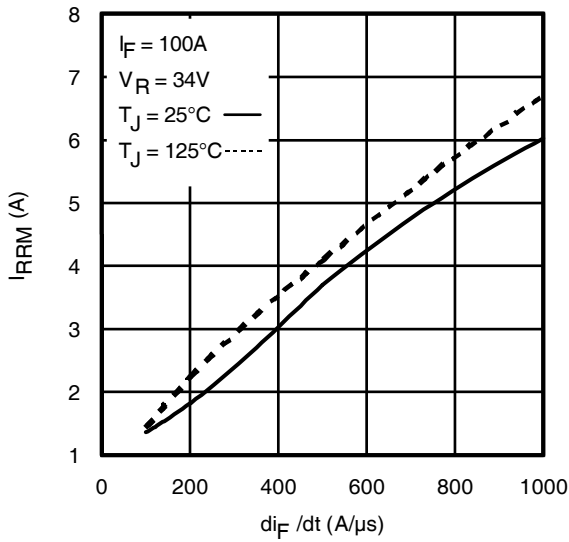
Fig. 19 - Typical Recovery Current vs. di$_f$/dt

Fig. 20 - Typical Stored Charge vs. di$_f$/dt

Fig. 21 - Typical Stored Charge vs. di$_f$/dt

Circuit Layout Considerations
• Low Stray Inductance
• Ground Plane
• Low Leakage Inductance Current Transformer

• dv/dt controlled by R_G
• Driver same type as D.U.T.
• I_{SD} controlled by Duty Factor "D"
• D.U.T. - Device Under Test

$D = \dfrac{P.W.}{Period}$

$V_{GS} = 10V$ *

* V_{GS} = 5V for Logic Level Devices

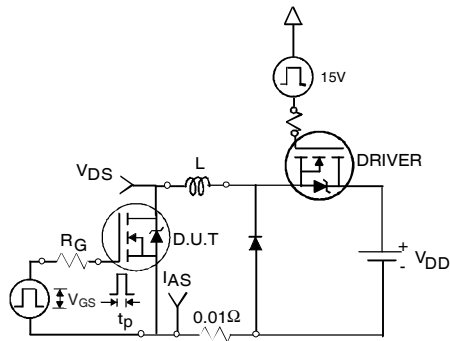**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel
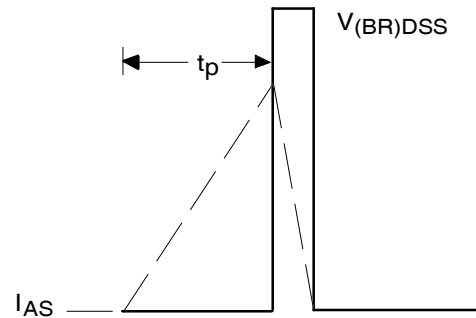Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit
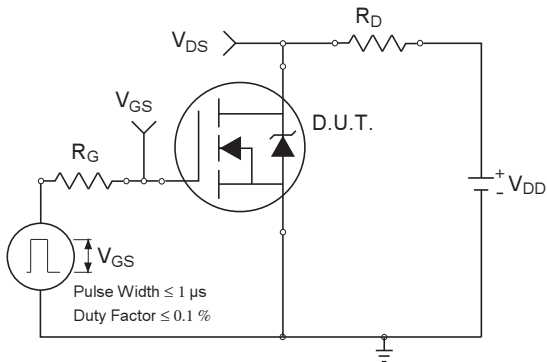

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit
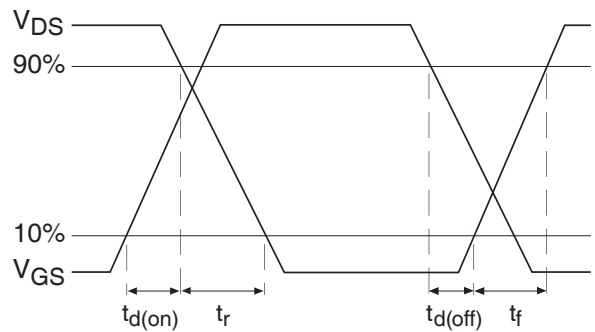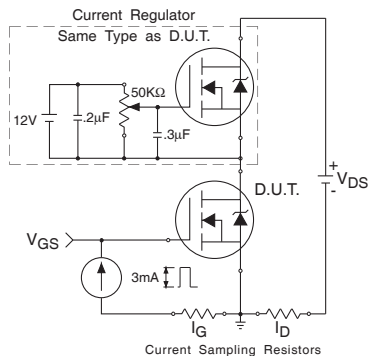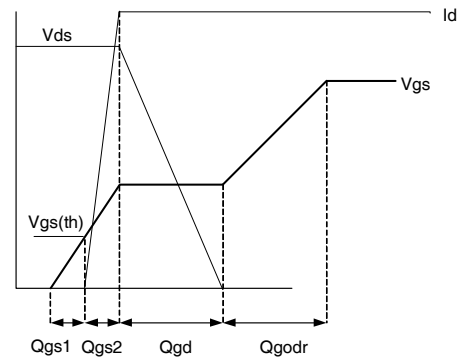

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform