MAS6512

Capacitive Sensor Signal Interface IC

This is preliminary information on a new product under development. Micro Analog Systems Oy reserves the right to make any changes without notice.

- **Single or Dual Capacitance Sensors**
- **Low Voltage Operation**
- **Low Power Consumption**
- **On Chip Temperature Sensor**
- **Internal Clock Oscillator**
- **16-Bit Ratiometric ΔΣ CDC**
- **EEPROM Calibration Memory**
- **Serial Interface**

DESCRIPTION

MAS6512 capacitive sensor signal Interface IC can interface both single and dual capacitance sensors.

It uses a 16-bit Capacitance-to-Digital Converter (CDC), which employs a delta-sigma (ΔΣ) conversion technique. The output data from the ΔΣ-modulator is processed by an on-chip decimator filter, producing a high resolution conversion result. The converter is run by an internal clock oscillator making an external converter clock unnecessary.

The converter input range is programmable to meet various sensor offset and changing capacitance values. Maximum sensor capacitance is 40pF but higher maximum value can be reached by using slower conversion speed or scaling the signal by using an external series capacitor.

The measurement resolution depends on the programmed capacitance range and over sampling ratio (OSR) selections.

MAS6512 supports two capacitance measurement modes. The output can be proportional either to capacitance difference (C_S-C_R) or to capacitance ratio (C_S-C_R)/C_S.

The IC is designed especially to meet the requirement for low power consumption, thus making it an ideal choice for battery powered systems. Current consumption values of 28 µA with high resolution or 1.9 µA with low resolution, at a conversion rate of one conversion per second, can be achieved.

In addition to measuring capacitance the device has an internal temperature sensor for temperature measurement and temperature compensation purposes. The 256-bit EEPROM memory stores trimming and calibration coefficients on chip.

A serial interface, compatible with a bi-directional 2-wire I^2C bus and 4-wire SPI bus, is used for conversion setup, starting a conversion and reading the conversion result.

FEATURES

- Single and Differential Capacitive Sensors
- Sensor Offset and Gain Adjustment
  - Changing Capacitance Range 2pF…30pF
  - Internal Offset Capacitance Matrix 0pF…22pF
  - External Capacitance up to 40pF (or higher using external clock)
- Resolution 14 bit (OSR=4096, ΔC=20pF)
- Internal Clock Oscillator
- On Chip Temperature Sensor -40°C...+85°C
- Low Voltage Operation 1.8 V…3.6 V
- Low Supply Current: 1.9 µA...28 µA
- Conversion Time 5.8ms...82.6ms (12Hz...173Hz)
- 16-bit Ratiometric ΔΣ CDC
- Internal 256-bit EEPROM Calibration Memory

APPLICATIONS

- I^2C and SPI Compatible Serial Interface
- QFN-16 Package
- Capacitive Pressure Sensors
- Humidity Sensors
- Medical Devices
- Flow Meters
- Sport Watches
- Altimeter and Barometer Systems
- Mobile and Battery Powered Systems
- Low Frequency Measurement applications
- Current/Power Consumption Critical Systems
- Industrial and Process Control applications in noisy environments

BLOCK DIAGRAM

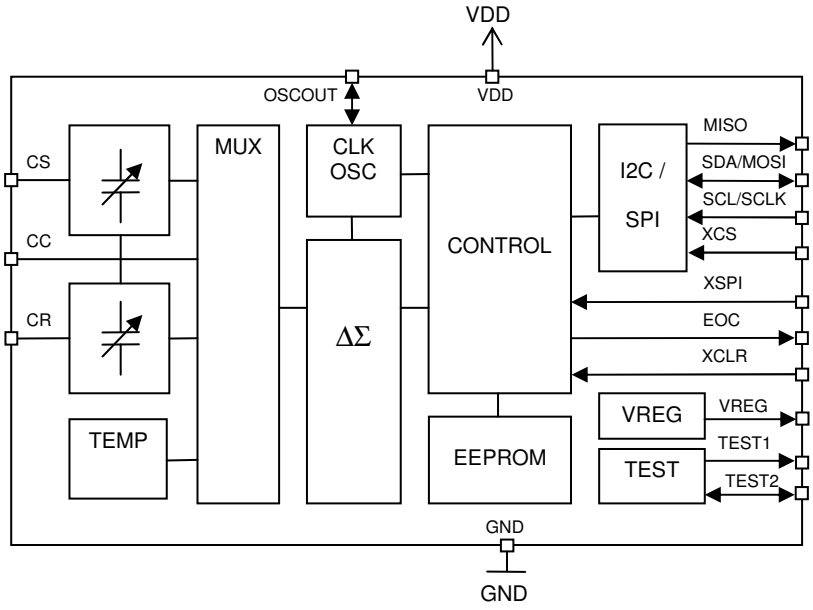


Figure 1. MAS6512 block diagram

FUNCTIONAL DESCRIPTION

MAS6512 can interface both single and dual capacitance sensors. Single capacitance sensors should be connected between the CS and the CC inputs. The second capacitor of a dual capacitance sensor should be connected between the CR and the CC inputs.

A Capacitance-to-Digital Converter (CDC) converts the input capacitances into a 16-bit output word (code). The converter front-end can be configured either for capacitance difference (C_S-C_R) or capacitance ratio (C_S-C_R)/C_S measurement mode. Converter resolution is selected by the over sampling ratio (OSR) setting. Higher OSR corresponds to higher resolution but also longer conversion time.

There are two internal 22pF capacitance matrices connected to the CS and the CR inputs. These matrices are used for sensor offset calibration and are programmable in 8-bit steps (86fF/step).

The gain is programmable with 8-bits resolution and sets the range for how much the measured capacitance can change.

MAS6512 includes an internal temperature sensor for temperature compensation purposes. A multiplexer in the front-end is used to select either the external capacitive sensor or the internal temperature sensor.

Trim and calibration coefficients can be stored in the 256-bit EEPROM memory. The stored trim values for the oscillator frequency, offset capacitance and gain are automatically read from the EEPROM memory in the beginning of each conversion. To avoid modification of the EEPROM by mistake there is an EEPROM write enable register which needs to be set to %01010101 (55_{HEX}) before any changes can be done to the EEPROM.

MAS6512 has an internal clock oscillator making an external clock unnecessary. To save power it's turned on only when a conversion is running. The frequency is trimmed to 200kHz using a 6-bit register. An external clock, connected to the OSCOUT pin, can however be used when a specific test mode is chosen. This might be necessary when measuring large capacitance since a slower clock frequency is needed in this case.

MAS6512 includes a 1.8V regulator that can be disabled in capacitance measurement mode. In temperature measurement mode the regulator is always used. The regulator is turned off between conversions.

Communication with MAS6512 is handled by the serial interface compatible with either a bi-directional 2-wire $I^2C^®$ bus or a 4-wire SPI bus. The XSPI pin is for selecting which bus type is used.

The XCLR pin can be used to reset the device including the serial communication.

The EOC pin indicates if a conversion has finished and the result is ready to be read from the memory via the serial interface.

I^2C is a registered trademark of NXP.

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	5.0	V
Voltage Range for All Pins			-0.3	V_{DD} + 0.3	V
Latchup Current Limit	I_{LUT}	For all pins, test according to JESD78A.	-100	+100	mA
Junction Temperature	T_{Jmax}			+ 150	℃
Storage Temperature	T_S	Note 1	- 55	+125	℃

Note 1: See EEPROM memory data retention at hot temperature. Storage or bake at hot temperatures will reduce the wafer level trimming and calibration data retention time.
Note: The absolute maximum rating values are stress ratings only. Functional operation of the device at conditions between maximum operating conditions and absolute maximum ratings is not implied and EEPROM contents may be corrupted. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions above absolute maximum ratings may be destructive to the devices.
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	Internal regulator disabled Internal regulator enabled	1.8 1.9	2.7 2.7	3.6 3.6	V
Supply Voltage at EEPROM Programming	V_{DD}	T=+25℃. Note 1.	3.0	3.3	3.6	V
Operating Temperature	T_A		-40	+25	+85	℃

Note 1. The recommended condition for EEPROM programming is room temperature.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7 V, T_A = -40℃ to +85℃, typical values at T_A = +27℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal regulator voltage	VREG	Regulator enabled		1.8		V
Quiescent current	I_Q	All inputs at VDD, no load. Note 1.			0.1	µA
Conversion current consumption	I_{DD_CONV}	During conversion		390		µA
Average current consumption	I_{DD_AVE}	1 conversion/s OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 28 14.1 7.1 3.7 1.9		µA
Conversion time	t_{CONV}	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		82.6 41.6 21.1 10.9 5.8		ms
VDD rise time for proper power on reset (POR)	t_{VDD_RISE}	Note 2.			400	ns
Internal system clock oscillator frequency	OSCOUT			200		kHz
Sensor excitation frequency	MCLK	No internal clock division Internal clock division		50 25		kHz

Note 1. Setting XCS low activates the EEPROM memory regardless of the XSPI setting and the device consumes 20µA …30µA current. To minimize current consumption XCS should be set low only during time periods when the device is used during SPI communication.
Note 2. Resetting the device using the XCLR pin is necessary in case the VDD rise time is longer than specified here.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7 V, T_A = -40°C to +85°C, typical values at T_A = +27°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal offset capacitor matrix selection	C_{R_OS}, C_{S_OS} C_{OS_STEP}		0	 0.086	22	pF
Changing capacitance range in capacitance difference mode	ΔC_{DIFF}	No internal clock division Internal clock / 2	2 2		20 30	pF
Maximum allowed sensor capacitance in capacitance difference mode	C_{S_MAX}	Internal clock Internal clock / 2 External clock			20 40 Note 1.	pF
Changing capacitance range in capacitance ratio mode	ΔC_{RATIO}	Note 2.	2		20	pF
Maximum allowed sensor capacitance in capacitance ratio mode	C_{S_MAX}	Note 2.			20 >20	pF
Integral nonlinearity	INL	OSR=256, capacitance difference mode		0.012		% of ΔC
RMS resolution		Difference mode $CODE_{DIFF}$~(C_S-C_R) ΔC=20pF OSR=4096		 14		 bit
RMS resolution		Ratio mode $CODE_{RATIO}$~(C_S-C_R)/C_S ΔC=20pF OSR=4096		 14		 bit
Internal temperature sensor	Linearity			±0.35	±0.5	°C
	Gain	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		267,8 267,6 267,3 33,3 4,1		LSB/°C
		Non-calibrated, note 3.	-4.5		+3.5	%
	Offset	Non-calibrated, note 3.			±11	°C

Note 1. In capacitance difference mode the maximum allowed sensor and reference capacitor values can be extended using lower external oscillator frequency; C_{S_MAX}=20pF*200kHz/f_{OSC_EXT}.
Note 2. In capacitance ratio mode also larger capacitances are possible depending on sensor characteristics. Please contact Micro Analog Systems to check sensor suitability.
Note 3. By calibrating the temperature measurement and compensating offset and gain errors an overall accuracy close to the linearity accuracy can be achieved.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7 V, T_A = -40°C to +85°C, typical values at T_A = +27°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EEPROM size				256		bit
EEPROM data retention		T_A = +85 °C T_A = +125 °C	10	24 1		years
Output data word length				16		bit
Linear output code range (10%...90% of full output code range)	$CODE_{DIFF}$	Difference mode Cs_min=8pF, Cs_max=12pF, Cr=10pF, gain setting 6Dhex OSR=256 OSR=512 OSR=1024 OSR=2048 OSR=4096	 89 71 5721 5727 5731		 799 6422 51494 51552 51580	
	$CODE_{RATIO}$	Ratio mode Cs_min=8pF, Cs_max=12pF, Cr=7.68pF, gain setting 4Dhex OSR=256 OSR=512 OSR=1024 OSR=2048 OSR=4096	 102 769 5944 5839 5786		 790 6389 51362 51486 51547	
Full output code range	$CODE_{DIFF}$	OSR=256 OSR=512 OSR=1024 OSR=2048 OSR=4096	0 0 0 0 0		892 7152 57280 57312 57328	
	$CODE_{RATIO}$	OSR=256 OSR=512 OSR=1024 OSR=2048 OSR=4096	0 0 0 0 0		888 7136 57216 57280 57312	

Digital inputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	VDD = 1.8…3.6V	80% VDD		100% VDD	V
Input Low Voltage	V_{IL}	VDD = 1.8…3.6V	0% VDD		20% VDD	V
Serial Bus Clock Frequency	f_{SCL_SCLK}				400	kHz

Digital outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage	V_{OH}	I_{Source}=0.6mA	80% VDD		100% VDD	V
Output low voltage	V_{OL}	I_{Sink}=0.6mA	0% VDD		20% VDD	V
Signal rise time	t_r			200		ns
Signal fall time	t_f			200		ns

OPERATING MODES

MAS6512 has two capacitance measurement modes and one temperature measurement mode. In capacitance measurement mode the output is proportional to either capacitance difference (C_S-C_R) or to capacitance ratio (C_S-C_R)/C_S. In temperature measurement mode the output is proportional to the absolute temperature.
Measurement mode configuration and start of conversion is done by writing 8-bit configuration data to the Measurement control register (address $E2_{HEX}$). See further details in the Measurement control register chapter.
MAS6512 includes a 256-bit EEPROM memory for storing trim and calibration data on chip. Four bytes (32 bits) of EEPROM are reserved for trim values but the remaining 28 bytes (224 bits) are free for calibration and other data.
The stored trim data consists of measurement configuration settings that are automatically read from EEPROM memory in the beginning of each conversion.
The calibration data should comprise of calibration and temperature compensation coefficients that can be used to calculate accurate calibrated sensor and temperature measurement results from the non-calibrated measurement reading. All calculations need to be done in an external micro controller unit (MCU).
A calibrated MAS6512 sensor system should be operated as illustrated in figure 2. The calibration and compensation coefficients need to be read to the MCU memory only once. From each pair of sensor and temperature measurement readings the accurate sensor and temperature values can then be calculated by using an external MCU.

All communication with MAS6512 is done using either the $I^2C^®$ bus or the SPI bus. Starting an A/D conversion, reading the conversion result and reading and writing data from and to the EEPROM memory are all accomplished via serial bus communication.
In addition to the serial buses the digital interface includes also end-of-conversion (EOC) and master reset (XCLR) pins. See A/D Conversion in the Serial Data Interface ($I^2C^®$ Bus) Control chapter.

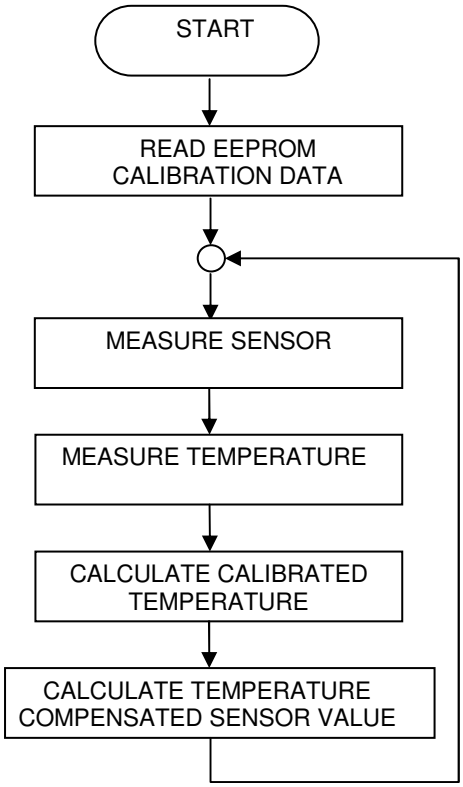


Figure 2. Flow chart for a calibrated MAS6512 sensor system

REGISTER AND EEPROM DATA ADDRESSES

Table 1. Register and EEPROM data addresses

A7	A6	A5	A4	A3	A2	A1	A0	I2C BUS HEX	SPI BUS HEX W=write R=read	Description	Note
A7	1	0	0	0	0	0	X	C0…C1	W: 40…41 R: C0…C1	EEPROM; free for any data	E
A7	1	0	0	0	0	1	0	C2	W: 42 R: C2	EEPROM; free for any data	E
A7	1	0	0	0	0	1	1	C3	W: 43 R: C3	EEPROM; CS capacitor matrix trim data	E+T
A7	1	0	0	0	1	0	0	C4	W: 44 R: C4	EEPROM; CR capacitor matrix trim data	E+T
A7	1	0	0	0	1	0	1	C5	W: 45 R: C5	EEPROM; Gain trim data	E+T
A7	1	0	0	0	1	1	0	C6	W: 46 R: C6	EEPROM; Oscillator frequency trim data	E+T
A7	1	0	0	0	1	1	1	C7	W: 47 R: C7	EEPROM; free for any data	E
A7	1	0	0	1	X	X	X	C8…CF	W: 48…4F R: C8…CF	EEPROM; free for any data	E
A7	1	0	1	X	X	X	X	D0…DF	W: 50…5F R: D0…DF	EEPROM; free for any data	E
A7	1	1	0	0	0	0	0	E0	W: 60 R: E0	Reset register; no data, only addressed for reset	R
A7	1	1	0	0	0	0	1	E1	W: 61 R: E1	Test register	R
A7	1	1	0	0	0	1	0	E2	W: 62 R: E2	Measurement control register	R
A7	1	1	0	0	0	1	1	E3	W: 63 R: E3	CS capacitor matrix register	R+T
A7	1	1	0	0	1	0	0	E4	W: 64 R: E4	CR capacitor matrix register	R+T
A7	1	1	0	0	1	0	1	E5	W: 65 R: E5	Gain register	R+T
A7	1	1	0	0	1	1	0	E6	W: 66 R: E6	Oscillator frequency control register	R+T
A7	1	1	0	1	0	1	0	EA	W: 6A R: EA	1st (MSB) byte of the conversion result	R
A7	1	1	0	1	0	1	1	EB	W: 6B R: EB	2nd (LSB) byte of the conversion result	R
A7	1	1	0	1	1	0	1	ED	W: 6D R: ED	Status register for EEPROM	R
A7	1	1	0	1	1	1	0	EE	W: 6E R: EE	Trimming control register	R

X = Don't care, E = EEPROM, R= Register, T = Trim data

Note: When using the SPI serial interface the register address bit A7 is also used for selecting write (A7= 0) or read (A7=1) operation. For the I^2C interface address bit A7 = 1.

REGISTER AND EEPROM DATA ADDRESSES

MAS6512 includes a 32 bytes (256 bits) EEPROM data memory and eleven registers. Four bytes (32 bits) of EEPROM are reserved for trim values but the remaining 28 bytes (224 bits) are free for storing sensor calibration and other data. See table 1 on the previous page for register and EEPROM data addresses.

In the SPI serial bus the address bit A7 selects between write (A7=0) and read (A7=1) operation. In the I^2C serial bus A7 is always high (A7=1) and selection between write and read operation is done with the LSB bit of the I^2C device address. See table 6 in chapter 2-WIRE SERIAL DATA INTERFACE (I^2C® BUS).

MAS6512 has four trim registers: CS capacitor matrix register ($E3/63_{HEX}$), CR capacitor matrix register ($E4/64_{HEX}$), Gain register ($E5/65_{HEX}$) and Oscillator frequency register ($E6/66_{HEX}$). These are marked with “R+T” in table 1. Each of these registers has a corresponding EEPROM byte where trim values can be permanently stored. These are marked with “E+T” in table 1. Trim values are automatically read from EEPROM in the beginning of each conversion when this feature is enabled in the trimming control register ($EE/6E_{HEX}$). When disabled it is possible to test different trim data in the trim registers before final trimming values are found and stored in the EEPROM.

Reset register ($E0/60_{HEX}$) does not contain any data. Any dummy data written to this register forces a reset. A reset initializes all control registers (addresses $E1_{HEX}$…EE_{HEX}) to a zero value.

Test register ($E1/61_{HEX}$) is mainly used for testing and trimming purposes. See table 2 in chapter TEST REGISTER. If an external clock signal is used the test register is needed for selecting the external clock signal.

The Measurement control register ($E2/62_{HEX}$) is used for configuring and starting an A/D conversion.

The CS ($E3/63_{HEX}$) and the CR ($E4/64_{HEX}$) capacitor matrix registers contain a capacitor value between 0 and 22pF in 86fF steps.
The Gain register ($E5/65_{HEX}$) controls the gain of the CDC front-end. Together with the CS and CR values it determines the input capacitance conversion range.

The Oscillator frequency control register ($E6/66_{HEX}$) is used only during internal clock oscillator trimming. During trimming this register value is iterated to give the desired 200kHz oscillator frequency. When the best value is found it can be written to the internal clock oscillator frequency trimming EEPROM address ($C6/46_{HEX}$). In normal operation the trim value is automatically read from the EEPROM memory in the beginning of each conversion. The clock frequency is trimmed by MAS during wafer level testing and there should be no need to modify it.

The 16-bit A/D conversion result (capacitance or temperature) is stored into two registers EA_{HEX} (MSB, most significant byte) and EB_{HEX} (LSB, least significant byte).

The EEPROM status register ($ED/6D_{HEX}$) reflects the EEPROM error correction status. This register can be used to verify that the EEPROM operation has finished without errors.

The Trimming control register ($E9/69_{HEX}$) defines if the trim data in the EEPROM or in the registers are used during operation. The Trimming control register is also used for enabling EEPROM write. The default setting is that all trim data is automatically read from the EEPROM memory in the beginning of each conversion and that the EEPROM write is disabled. See the Trimming control register description for details.

RESET REGISTER (E0/60$_{HEX}$)

This register is used to reset all control registers (addresses $E1_H$…EE_H) to a zero value. There are no data bits in this register. However it is necessary to write dummy data to this register to make a reset.

The reset will take place immediately after any data has been written to the address $E1/61_{HEX}$ via the I^2C or SPI interface.

TEST REGISTER (E1/61$_{HEX}$)

In normal operation the Test register value is 00_{HEX} and the internal clock oscillator is used for all the measurements.

The SEL_EXTCLK bit enables the use of an external clock signal connected to the OSCOUT pin. This may come necessary if the sensor capacitance is too high to be used with the internal 200kHz clock signal. Sensor capacitances up to around 20pF can be measured with the internal 200kHz oscillator, or up to 40pF if the internal clock frequency is divided by two (see SOSCOUT below).

By setting the SOSCOUT bit it is possible to divide the internal clock oscillator frequency by two, giving a 100kHz frequency. This lower clock frequency can be used for measuring up to about 40pF capacitances. For measuring larger than 40pF sensor capacitances (C_S) it is necessary to use an external clock frequency having a frequency of around f_{EXT}=200kHz*20pF/Cs or less. Note that the frequency division selection SOSCOUT applies only to the internal clock signal.

The STEST bits are used for connecting different internal signals to the TEST1 and TEST2 pins. In STEST[2:0]=101 test setup TEST1 and TEST2 operate as voltage inputs which are connected to the differential input of the ΔΣ-ADC. VTESTP is the positive input and VTESTN is the negative input of the ΔΣ-ADC.

FOSC can be used to force the internal oscillator to be on all the time. Normally the internal oscillator is turned on only during the measurements to save power.

Table 2. MAS6512 test register (*E1/61$_{HEX}$*) description

Bit Number	Bit Name	Description	Value	Function
7-6	-	Not used	-	-
5	SEL_EXTCLK	Selects external clock	0 1	Normal mode An external clock can be connected to OSCOUT and the internal oscillator is disabled
4-2	STEST[2:0]	TEST1 and TEST2 signal selection	000…100 101 110…111	Reserved for internal testing purpose (TEST1 and TEST2 are outputs) VTESTP => TEST1 (input) VTESTN => TEST2 (input) No function
1	SOSCOUT	Select OSCOUT frequency	0 1	OSCOUT = 200 kHz OSCOUT = 100 kHz
0	FOSC	Forces the oscillator on without conversion	0 1	OSC is on only during conversion OSC is forced on

X = Don't care, SDM = Sigma delta modulator

MEASUREMENT CONTROL REGISTER (E2/62$_{HEX}$)

This register is used to configure and initiate a measurement. See table 3 below. A new conversion is started simply by writing 8-bit configuration data to the measurement control register (E2/62$_{HEX}$).

Table 3. Measurement control register (E2/62$_{HEX}$) description

Bit Number	Bit Name	Description	Value	Function
7-5	OSRS	Over Sampling Ratio (OSR) Selection	000 001 010 011 100	OSR = 256 OSR = 512 OSR = 1024 OSR = 2048 OSR = 4096
4	REGEN	Regulator Enable	0 1	Voltage regulator disabled Voltage regulator enabled
3	SCO	Start Conversion	0 1	No conversion Start conversion
2	XETS	Sensor Selection	0 1	External capacitive sensor Internal temperature sensor
1	-	Not used	-	-
0	XRC	Front end function selector	0 1	Ratio converter Difference converter

The OSRS over sampling ratio selection bits choose between five different OSR values. High OSR value corresponds to high resolution but also longer conversion time. See Electrical characteristics for further details.

The REGEN bit enables/disables the internal voltage regulator. When enabled the regulator is turned on during conversions and automatically turned off after each conversion to save power. During temperature measurements the regulator is always enabled regardless of the REGEN bit setting. Note that if Test register FOSC=1 and if REGEN=1 the regulator is forced on all the time independently of measurements.

The SCO Start conversion bit needs to be set 1 for every new measurement. It is automatically reset to 0 after each measurement.

The XETS Sensor selection bit controls the front-end multiplexer and connects either the external capacitive sensor (XETS=0) or the internal temperature sensor (XETS=1) to the ΔΣ-converter.

The XRC bit selects between two external capacitive sensor measurement modes. It does not have any effect on temperature measurement. In Ratio converter mode the measured value will be proportional to capacitance ratio (C_S-C_R)/C_S. In Difference converter mode the measurement will be proportional to capacitance difference (C_S-C_R).

CS AND CR CAPACITOR MATRIX REGISTERS (E3/63$_{HEX}$ AND E4/64$_{HEX}$)

There are two internal capacitor matrices that add capacitance in parallel to the sensor capacitor (CS) and the reference capacitor (CR). These offset capacitances are used to adjust the sensor signal to an optimal range. Each capacitor matrix has a selectable capacitance from 0pF up to 22pF in typical 86fF steps. The three sigma process variation of the capacitor matrix capacitance is ±10%.The CS capacitor matrix register (E3/63$_{HEX}$) has a corresponding EEPROM byte (C3/43$_{HEX}$) for storing the trim value. Also the CR capacitor matrix register (E4/64$_{HEX}$) has corresponding EEPROM byte (C4/44$_{HEX}$) for storing the trim value. After finding suitable CS and CR capacitor matrix register values the trim values can be stored in the non-volatile EEPROM.
In normal operating mode these trim values are automatically read from the EEPROM during each conversion start. See also table 9 Trimming control Register (EE/6E$_{HEX}$) for other operating modes.

Table 4. CS capacitor matrix register (E3/63$_{HEX}$), EEPROM (C3/43$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	OCDACS	CDAC control bits	0$_{HEX}$…FF$_{HEX}$	CS offset trimming

Table5. CR capacitor matrix register (E4/64$_{HEX}$), EEPROM (C4/44$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	OCDACR	CDAC control bits	0$_{HEX}$…FF$_{HEX}$	CR offset trimming

GAIN REGISTER (E5/65$_{HEX}$)

The gain register sets the excitation signal level for the capacitive sensor. The eight bits (GRDAC) can be programmed to values between 0 and 255. Together with the CS and the CR capacitor matrix trim parameters it's used to adjust the sensor signal to an optimal range. The goal is to get a maximum dynamic range and keep the signal within linear input range of the ΔΣ-modulator. This condition is met when the signal minimum and maximum covers the whole linear input range.

The output of MAS6512 has the following relationship to the ΔΣ-modulator output:

$$CODE_{OUT} = Q_{AVE} \cdot CODE_{RANGE}$$

Q_{AVE} is the average measurement result (from the over sampling) of the ΔΣ-modulator and varies from 0 to 1. The $CODE_{RANGE}$ is the maximum output code which depends on OSR and measurement mode selections. See page 5 Full output code range specification in the Electrical characteristics table. The linear signal range of the modulator is from Q_{AVE}=10% to Q_{AVE} =90%.

In case of capacitance difference measurement mode;

$$Q_{AVE} = \frac{1}{2} + \frac{C_S - C_R}{C_{REF}} * \frac{V_S}{2 * V_R}$$

In this mode the gain register value GRDAC sets the V_S level.
V_S= (VDD/1.8V)*(33mV+GRDAC*2.88mV)
V_R = (VDD/1.8V)*144mV
C_S = External sensor + CS matrix capacitance
C_R = External reference + CR capacitance
C_{REF} = 6pF, three sigma variation ±10%

In case of capacitance ratio measurement mode;

$$Q_{AVE} = \left(1 - \frac{C_R}{C_S}\right) * \frac{V_R}{V_S}$$

In this mode the gain register value GRDAC sets the V_S level.
V_S = (VDD/1.8V)*GRDAC*0.52mV
V_R= (VDD/1.8V)*100.8mV
C_S = External sensor + CS matrix capacitance
C_R = External reference + CR capacitance

The gain register (E5/65$_{HEX}$) has a corresponding EEPROM byte (C5/45$_{HEX}$). After finding a suitable gain register value it can be stored in the EEPROM memory. In normal operating mode the gain trim value is read automatically from the EEPROM during each conversion start.

Table 6. Gain register (E5/65$_{HEX}$), EEPROM (C5/45$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	GRDAC	RDAC control bits	0$_{HEX}$…FF$_{HEX}$	Gain control by sensor excitation signal level control

OSCILLATOR FREQUENCY CONTROL REGISTER ($E6/66_{HEX}$)

Note that the internal clock oscillator frequency has been factory trimmed and the trim value has been stored in the EEPROM ($C6/46_{HEX}$). It is recommended not to change the factory programmed value!

The oscillator frequency control register ($E6/66_{HEX}$) is for trimming the internal clock oscillator to 200 kHz frequency. This 200kHz (or 100kHz if SOSCOUT=1) can be measured at the OSCOUT pin. The six LSB bits adjust the oscillator period in 104ns steps. The period increases when the trim value increases. Typically a register value of 28_{HEX} corresponds to the nominal 200kHz clock oscillator frequency.
After finding a suitable trim value it can be stored to the EEPROM ($C6/46_{HEX}$).

Table 7. Oscillator frequency control register ($E6/66_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
5-0	OSCF	Oscillator frequency control bits	0_{HEX}…$3F_{HEX}$	Oscillator frequency control

EEPROM STATUS REGISTER ($ED/6D_{HEX}$)

The EEPROM status register ($ED/6D_{HEX}$) indicates if the stored EEPROM byte is corrupted. The register is updated after each EEPROM data byte read command. See table 8 below. The ERROR bit tells whether an data error has been detected or not. The DED bit tells whether two or more bit errors have been detected. The EEPROM can correct internally only single bit errors i.e. when ERROR=1 and DED=0. The read EEPROM data byte is corrupted if ERROR=DED=1.

Table 8. MAS6512 EEPROM status register ($ED/6D_{HEX}$). Only bits (7:6) are used.

Bit Number	Bit Name	Description	Value	Function
7	ERROR	EEPROM error detection	0 1	No errors Error detected
6	DED	EEPROM double error detection	0 1	No errors 2 (or more) data errors
5-0			0	-

X = Don't care

CONVERSION RESULT REGISTERS ($EA_{...}EB_{HEX}$)

After measuring capacitance or temperature the 16-bit conversion result is stored into two register addresses EA_{HEX} and EB_{HEX}. The MSB (most significant byte) is at EA_{HEX} and LSB (least significant byte) at EB_{HEX}.

TRIMMING CONTROL REGISTER ($EE/6E_{HEX}$)

The Trimming control register ($EE/6E_{HEX}$) is used to select between different trimming operating modes and enabling EEPROM write. See table 9 showing the functions of the Trimming control register.

After a power-up reset, master reset via XCLR or a software reset the Trimming control register ($EE/6E_{HEX}$) gets the value %00000000 (00_{HEX}). This is the normal operating mode for a trimmed MAS6512 device. In this mode the capacitive front-end trim values to use (CS, CR and Gain) are automatically read from the EEPROM memory in the beginning of each conversion start.

The EEPROM is normally write protected. To disable the write protection the Trimming control register should be set to %01010101 (55_{HEX}).

When calibrating a sensor there is an operating mode in which only the factory calibrated internal oscillator (OSC) clock trim data is read from the EEPROM memory. This mode is selected by writing %10101010 (AA_{HEX}) to the Trimming control register. In this mode it is possible to run conversion tests for different front-end trim register values before suitable values are found and programmed to the EEPROM.

There is also a trimming mode in which all trim data including the internal oscillator trim data is taken from the trim registers rather than from the EEPROM. This mode is selected by writing %11111111 (FF_{HEX}) to the Trimming control register.

Table 9. Trimming control Register ($EE/6E_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	REGEE<7:0>	EEPROM control bits	00000000	All trim data from EEPROM (normal operating mode)
			01010101	EEPROM write enabled
			10101010	Only OSC from EEPROM
			11111111	All trim data from registers
			OTHER	All trim data from EEPROM

EEPROM WRITE PROCEDURE

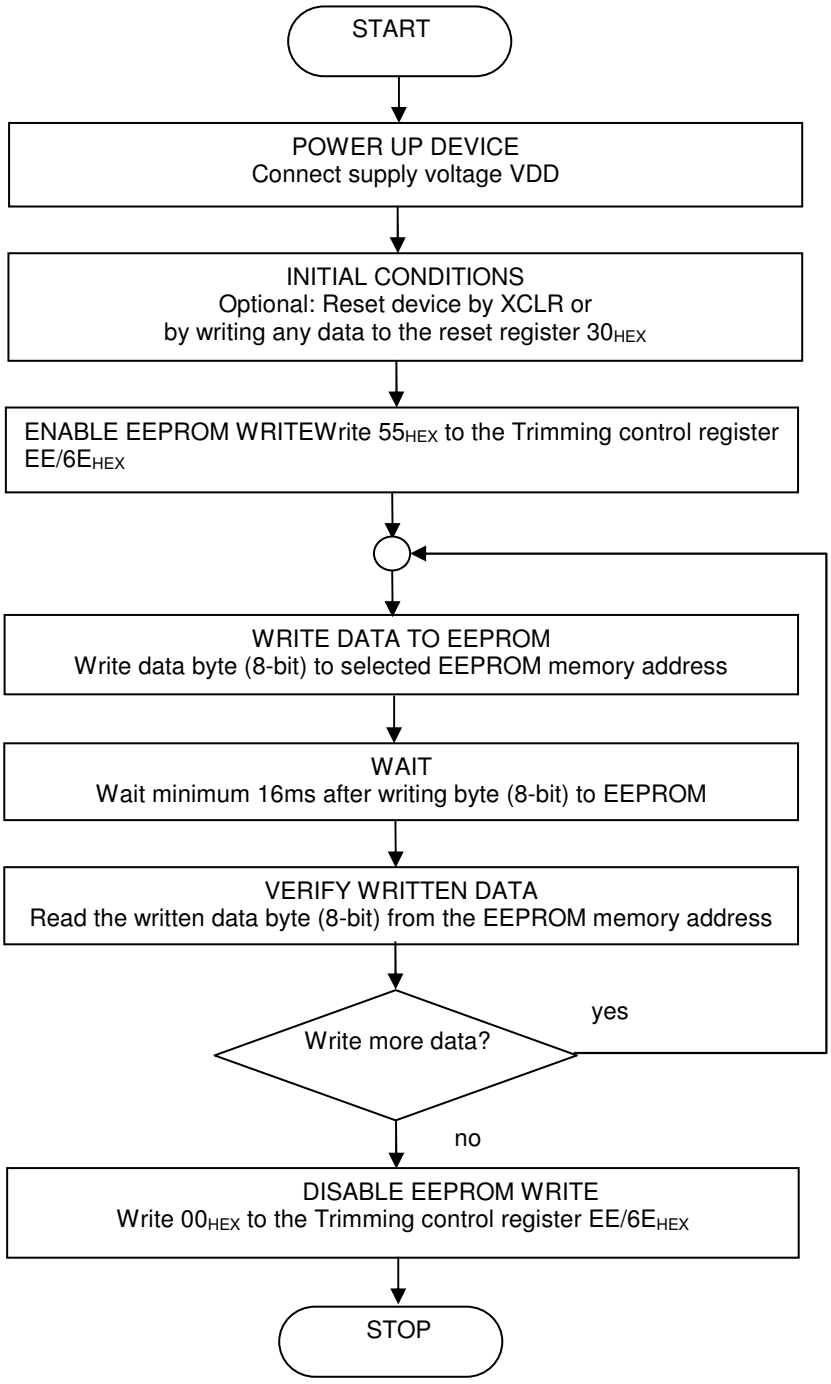


Figure 3. Flow chart for MAS6512 EEPROM write

EEPROM WRITE PROCEDURE

This chapter gives instructions for writing data to the EEPROM memory.

The MAS6512 16-bit Capacitance to Digital Converter (CDC) has a 256 bit (32 bytes) EEPROM memory. 8 bits (1 byte) has been reserved for storing internal clock oscillator trimming data. 24 other bits (3 bytes) are for trimming the capacitive sensor front-end. The remaining 232 bits (28 bytes) are free for other use.

See figure 3 on previous page showing the EEPROM write procedure.

Make sure in the beginning of the EEPROM write procedure that the MAS6512 initial conditions are met. Connecting VDD triggers power-on-reset (POR) but to make sure the device is reset an additional reset can be given using the XCLR pin or writing any data on the reset register $E0/60_{HEX}$ via the serial bus.

EEPROM write is enabled by writing value 55_{HEX} to the Trimming control Register ($EE/6E_{HEX}$). The default register value after power on is 00_{HEX}.

Next the data can be written to the EEPROM memory one byte (8-bit) at a time. It is necessary to have a delay of minimum 16ms after programming each byte (8-bit). The success of each write can be verified by reading back the data (8-bit) and comparing it to the original byte (8-bit). Additionally it is also possible to check the EEPROM status register ($ED/6D_{HEX}$) value after each read back. The EEPROM status register value should be 00_{HEX} when the read EEPROM data byte is free of errors.

After all data bytes are written the EEPROM memory can be protected from write by writing 00_{HEX} to the Trimming control Register ($EE/6E_{HEX}$).

See table 1 showing the MAS6512 register and EEPROM data addresses.

2-WIRE SERIAL DATA INTERFACE (I²C® BUS)

Serial Interface

MAS6512 has an I²C® bus compatible two wire serial data interface comprising of serial clock (SCL) and bi-directional serial data (SDA) pins. In the I²C® bus both SCL & SDA lines are of open-drain design, thus, external pull-up resistors are needed.

The serial data interface is used to configure and start the A/D conversion and read the measurement result when the A/D conversion has finished.

The digital interface includes also end of conversion (EOC) and master reset (XCLR) pins. The EOC goes high when the A/D conversion has finished.

The XCLR is used to reset the A/D converter. A reset initializes internal registers, counters and the serial communication bus. After connecting the supply voltage to MAS6512, and before starting operating the device via the serial bus, it is required to reset the device with the XCLR reset pin if the supply voltage rise time has been longer than 400 ns (typ). If the supply voltage rise time is shorter than this making an external reset with the XCLR pin is not necessary since the device is automatically reset by the power on reset (POR) circuitry. It is however recommended to use the XCLR reset feature to solve unexpected error state conditions.

Device Address

The I²C® bus definition allows several I²C® bus devices to be connected to the same bus. The devices are distinguished from each other by unique device address codes. MAS6512 device address is shown in table 10. The LSB bit of the device address defines whether the bus is configured for Read (1) or Write (0) operation. EC_{HEX}= Write, ED_{HEX}= Read.

Table 10. MAS6512 device address (EC/ED_{HEX})

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	1	0	1	1	0	0/1

I²C® Bus Protocol Definitions

Data transfer is initiated with a Start bit (S) when SDA is pulled low while SCL stays high. Then, SDA sets the transferred bit while SCL is low and the data is sampled (received) when SCL rises. When the transfer is complete, a Stop bit (P) is sent by releasing the data line to allow it to be pulled up while SCL is constantly high.

Figure 4 shows the start (S) and stop (P) bits and a data bit. Data must be held stable at the SDA pin when SCL is high. Data at the SDA pin can change value only when SCL is low.

Each SDA line byte transfer must contain 8-bits where the most significant bit (MSB) always comes first. Each byte has to be followed by an acknowledge bit (see further below). The number of bytes transmitted per transfer is unrestricted.

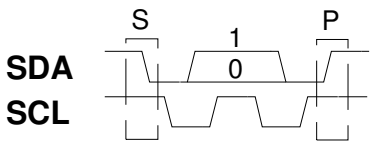


Figure 4. I²C® bus protocol definitions

Bus communication includes Acknowledge (A) and not Acknowledge (N) messages. To send an acknowledge the receiver device pulls the SDA low for one SCL clock cycle. For not acknowledge (N) the receiver device leaves the SDA high for one SCL clock cycle in which case the master can then generate either a Stop (P) bit to abort the transfer, or a repeated Start (Sr) bit to start a new transfer.

Abbreviations:
A= Acknowledge by Receiver
N = Not Acknowledge by Receiver
S = Start
Sr = Repeated Start
P = Stop
▭ = from Master (MCU) to Slave (MAS6512)
▭ = from Slave (MAS6512) to Master (MCU)

2-WIRE SERIAL DATA INTERFACE (I²C® BUS)

Conversion Starting – Write Sequence

Conversion is started by writing configuration bits into the Measurement control register (address $E2_{HEX}$). The write sequence is illustrated in Table 11.

Table 11. MAS6512 I2C bus write sequence bits

S	AW	A	MC	A	DC	A	P

Abbreviations:
AW = Device Write Address (%1110 1100)
AR = Device Read Address (%1110 1101)
MC = Measurement control register (%1110 0010)
Ax = Conversion Result Registers; MSB (x=M, %1110 1010) or LSB (x=L, %1110 1011)
DC = Measurement Control Register Data
Dx = Conversion Result Register Data; MSB (x=M), ISB (x=I) or LSB (x=L)

Each serial bus operation, like write, starts with the start (S) bit (see figure 4). After start (S) the MAS6512 device address with write bit (AW, see table 10) is sent followed by an Acknowledge (A). After this the Measurement control register address (see table 1) is sent and followed by an Acknowledge (A). Next the Measurement control register data (DC, see table 3) is written and followed by an Acknowledge (A). Finally the serial bus operation is ended with stop (P) command (see figure 4).

A/D Conversion

After power on reset or external reset (XCLR) the EOC output is high. After an A/D conversion is started the EOC output is set low until the conversion is finished and the EOC goes back high, indicating that the conversion is done and data is ready for reading. The EOC is set low only by starting a new conversion. To save power the internal oscillator runs only during conversion.
During an A/D conversion the input signal is sampled continuously leading to an output conversion result that is a weighted average of the samples taken.

Conversion Result – Read Sequence

Table 12 presents a general control sequence for a single register data read.

Table 12. MAS6512 I2C bus single register (address Ax) read sequence bits

S	AW	A	Ax	A	Sr	AR	A	Dx	N	P

Table 13 shows the control sequence for reading the 16-bit A/D conversion result from the Conversion result registers. The LSB (DL) register data read can follow right after the MSB register data (DM) read since if the read sequence is continued (not ended by a Stop bit P) the register address is automatically incremented to point to the next register.

Table 13. MAS6512 I2C bus MSB (first) and LSB (second) A/D conversion result read sequence

S	AW	A	AM	A	Sr	AR	A	DM	A	DL	N	P

4-WIRE SERIAL DATA INTERFACE (SPI BUS)

SPI bus communication is selected by setting XSPI pin low.

SPI communication differs from I2C bus in the following way. It requires four wires for bi-directional communication since each line operates in one direction only. Device selection is done by using separate chip select XCS control lines instead of using device address. Each SPI bus device has its own XCS control line and a device is selected by pulling its XCS line low (see figure 5 below). The fourth wire in the SPI bus is the serial clock line, SCLK. Data is transferred at rising edges of the serial clock during which the data line should be stable.

The selection between write or read access is done by register address MSB bit A7 (see table 1 "*Register and EEPROM data addresses*"). In write access bit A7 cleared (0) and in read access it is set (1).

Figure 5 illustrates write access communication. MAS6512 has an auto increment function which means that if there are more than one data byte transferred the additional data bytes are delivered to following register addresses. In write communication the MISO line is high impedance.

In SPI bus communication it is good to note that setting XCS low activates the EEPROM memory regardless of the XSPI setting and the device consumes 20µA …30µA current. To minimize current consumption XCS should be set low only during time periods when the device is used during SPI communication.

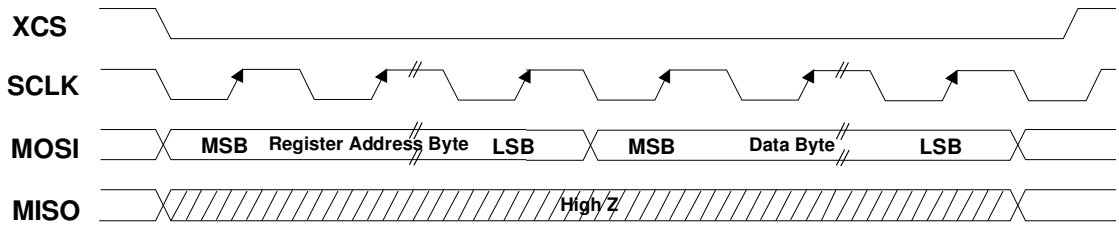


Figure 5. *SPI Protocol – Write Access (register address MSB bit A7=0)*

Figure 6 illustrates read access communication. The auto increment function can be utilized also in read access and if there are more than one data byte read the additional data bytes are delivered from following register addresses.

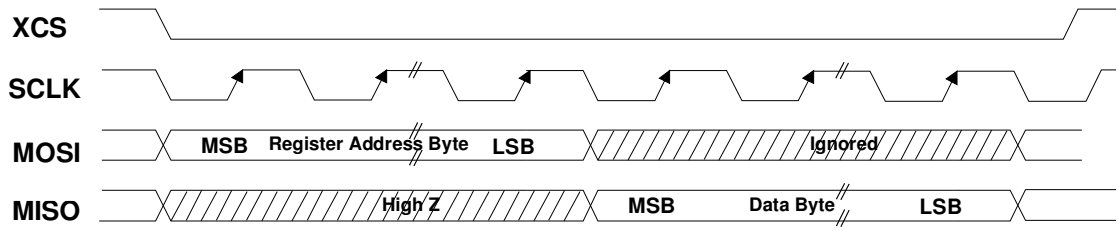


Figure 6. *SPI Protocol – Read Access (register address MSB bit A7=1)*

TRIMMING FOR SENSOR CAPACITANCE

MAS6512 has two capacitance measurement modes and a temperature measurement mode. In capacitance measurement mode the output can be proportional either to capacitance difference (C_S-C_R) or to capacitance ratio (C_S-C_R)/C_S. In temperature measurement mode the output is proportional to absolute temperature.

For trimming it is necessary to know the sensor capacitance C_S range $C_{S\ MIN}$…$C_{S\ MAX}$. For optimal utilization of the MAS6512AA1 input range the trimming is based on selecting the minimum linear range capacitance same as $C_{S\ MIN}$ and maximum linear range capacitance same as $C_{S\ MAX}$. At the linear range minimum and maximum limits the average of the ΔΣ-modulator output is 10% and 90% respectively. In the following trimming equations we denote these by

D_{MIN} = 0.1
D_{MAX} = 0.9

MAS6512 in capacitance difference mode

The reference capacitor value C_R is calculated from

$$C_R = [C_{S\ MIN}*(D_{MAX}-0.5)-C_{S\ MAX}*(D_{MIN}-0.5)] / (D_{MAX}-D_{MIN})$$

If an external C_R is used, it is connected between pins CR and CC. If an internal C_R is used, the trim code for C_R is calculated from

$$REG_{E4HEX} = (C_R/C_{R\ MAX})*255$$

where $C_{R\ MAX}$ is nominally 22pF, but subject to ±10 % (±3 sigma) process variation.

The reference voltage, $V_{S,}$ can be calculated using the following equation:

$$V_S = [144mV*(D_{MAX}-D_{MIN})*2*C_{REF}] / (C_{S\ MAX}-C_{S\ MIN})$$

where C_{REF} is nominally 6 pF, but also has ±10 % variation.

The gain register trim value is calculated from

$$REG_{E5HEX} = [(V_S-33\ mV) / 734mV]*255$$

REG_{E4HEX} and REG_{E5HEX} are 8-bit values, so they range from 0 to 255. When their values are found, the same values can be written to corresponding EEPROM addresses $C4_{HEX}$ and $C5_{HEX}$. However, with SPI bus, the address MSB in write operation is 0, so the addresses are actually 44_{HEX} and 45_{HEX}.

Example: Single capacitance sensor

$C_{S\ MIN}$=8pF
$C_{S\ MAX}$=12pF

C_R = [8pF*(0.9-0.5)-12pF*(0.1-0.5)]/(0.9-0.1) = 10pF
REG_{E4HEX} = (10pF/22pF)*255 = 115.9 ~ 116

V_S = [144mV*(0.9-0.1)*2*6pF] / (12pF-8pF) = 345.6mV
REG_{E5HEX} = [(345.6-33 mV) / 734mV]*255 = 108.6 ~109

REG_{E3HEX} = 0 (no internal C_S capacitor matrix used)

TRIMMING FOR SENSOR CAPACITANCE

MAS6512 in capacitance ratio mode

The reference capacitor C_R is calculated from

$C_R = [C_{S\,MIN}*C_{S\,MAX}*(D_{MAX}-D_{MIN})] / (C_{S\,MAX}*D_{MAX}-C_{S\,MIN}*D_{MIN})$

If an external C_R is used, it is connected between pins CR and CC. If an internal C_R is used, the trim code for C_R is calculated from

$REG_{E4HEX} = (C_R/C_{R\,MAX})*255$

where $C_{R\,MAX}$ is nominally 22pF, but subject to ±10 % (±3 sigma) process variation.

The reference voltage, $V_{S,}$ can be calculated using the following equation:

$V_S = 100.8mV * (C_{S\,MAX}-C_{S\,MIN}) / (C_{S\,MAX}*D_{MAX}-C_{S\,MIN}*D_{MIN})$

The gain register trim value is calculated from

$REG_{E5HEX} = (V_S / 133.3mV)*255$

REG_{E4HEX} and REG_{E5HEX} are 8-bit values, so they range from 0 to 255. When their values are found, the same values can be written to corresponding EEPROM addresses $C4_{HEX}$ and $C5_{HEX}$. However, with SPI bus, the address MSB in write operation is 0, so the addresses are actually 44_{HEX} and 45_{HEX}.

Example: Single capacitance sensor

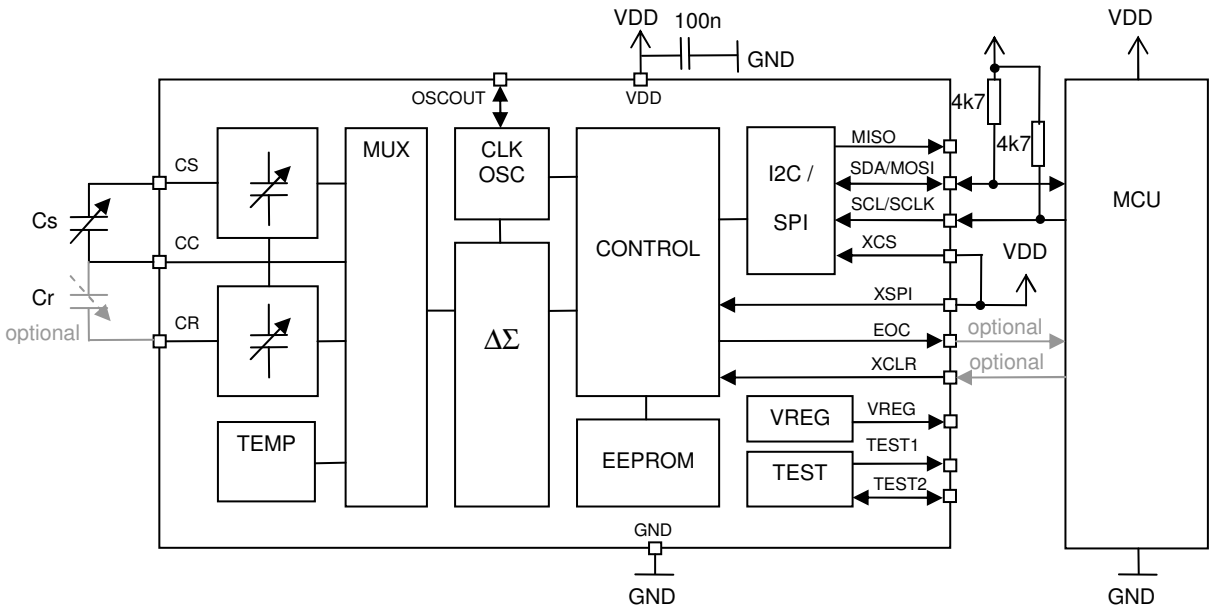
$C_{S\,MIN}$=8pF
$C_{S\,MAX}$=12pF

$C_R = [8pF*12pF*(0.9-0.1)] / (12pF*0.9-8pF*0.1) = 7.68pF$
$REG_{E4HEX} = (7.68pF/22pF)*255 = 89.0 \sim 89$

$V_S = 100.8mV*)/(12pF-8pF)/(12pF*0.9-8pF*0.1)=40.32mV$
$REG_{E5HEX} = (40.32mV/133.3mV)*255 = 77.1 \sim 77$

$REG_{E3HEX} = 0$ (no internal C_S capacitor matrix used)

APPLICATION INFORMATION



NOTE: It is recommended to use the XCLR reset feature to solve unexpected error state conditions. The XCLR pin can be left unconnected if not used. It has internal pull up to VDD.

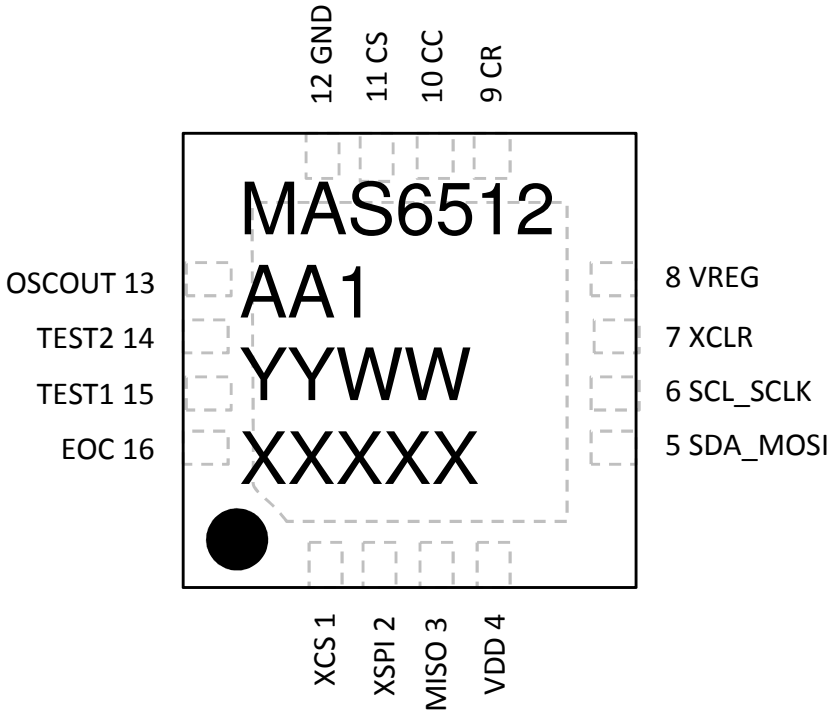
Figure 7. MAS6512 configured for I^2C bus communication

Note: MAS6512 has an effective ESD clamp protection structure that can be triggered if the VDD rises too fast. For this reason it's recommended to use a supply decoupling capacitor having a value of 100nF or higher to slow down the VDD rise time.

Accuracy Improvement – Averaging

An averaging technique can be used to remove conversion errors caused by noise and thus improve measurement accuracy. By doing several A/D conversions and calculating the average result it's possible to average out noise. Theoretically the noise is reduced by a factor $\sqrt{N}$ where N is the number of averaged samples. A/D converter nonlinearities cannot be removed by averaging.

MAS6512 IN QFN-16 4x4x0.75 PACKAGE



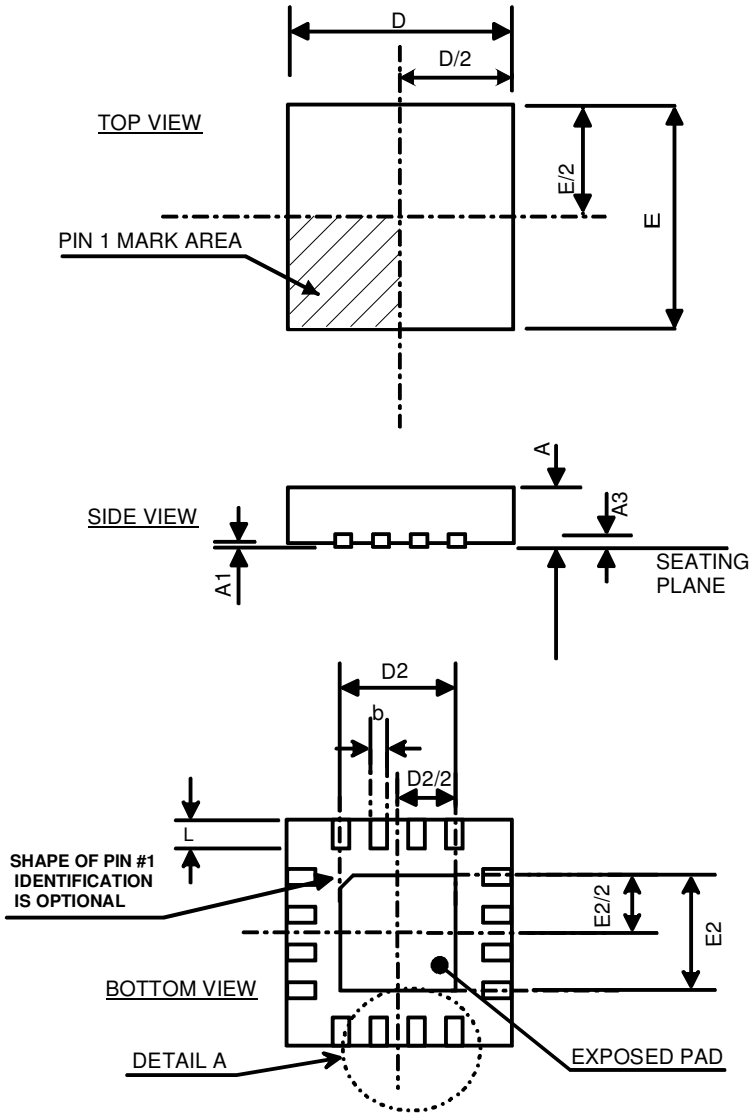
Top Marking Information:
MAS6512 = Product Number,
AA1 = Version Number
YYWW = Year Week
XXXXX = Lot Number

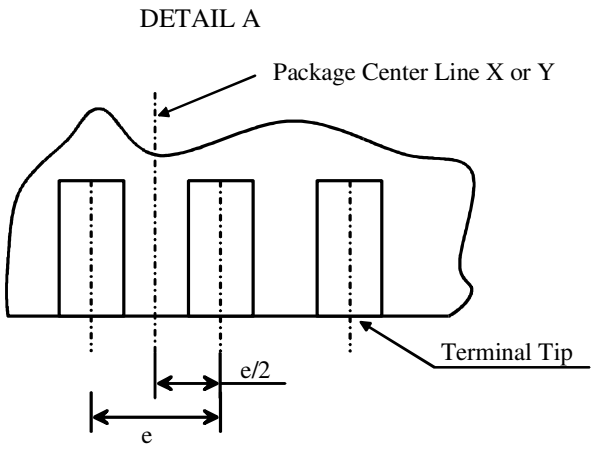
QFN-16 4x4x0.75 PIN DESCRIPTION

Pin Name	Pin	Type	Function
XCS	1	DI	Chip Select (SPI)
XSPI	2	DI	SPI / I2C Bus Selection SPI: XSPI=low I2C: XSPI=high
MISO	3	DO	Master Input Slave Output (SPI)
VDD	4	P	Power Supply Voltage
SDA_MOSI	5	DI/O	Serial Bus Data (I2C) Master Output Salve Input (SPI)
SCL_SCLK	6	DI	Serial Bus Clock (I2C / SPI)
XCLR	7	DI	Master Reset
VREG	8	AO	Voltage Regulator Output 1.8V
CR	9	AI	Reference Capacitance Pin
CC	10	AI	Common Capacitance Pin
CS	11	AI	Sensing Capacitance Pin
GND	12	G	Power Supply Ground
OSCOUT	13	DI/DO	Oscillator Output
TEST2	14	AI/O	Test pin 2
TEST1	15	DO	Test pin 1
EOC	16	DO	End of Conversion

P = Power, G = Ground, DO = Digital Output, , DI = Digital Input, AO = Analog Output, AI = Analog Input

PACKAGE (QFN-16 4X4x0.75) OUTLINE





Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.700	0.750	0.800	mm
A1	0.000	0.020	0.050	mm
A3		0.203 REF		mm
b	0.250	---	0.350	mm
D	3.950	4.000	4.050	mm
D2 (Exposed.pad)	2.700	---	2.900	mm
E	3.950	4.000	4.050	mm
E2 (Exposed.pad)	2.700	---	2.900	mm
e		0.650 BSC		mm
L	0.350	---	0.450	mm

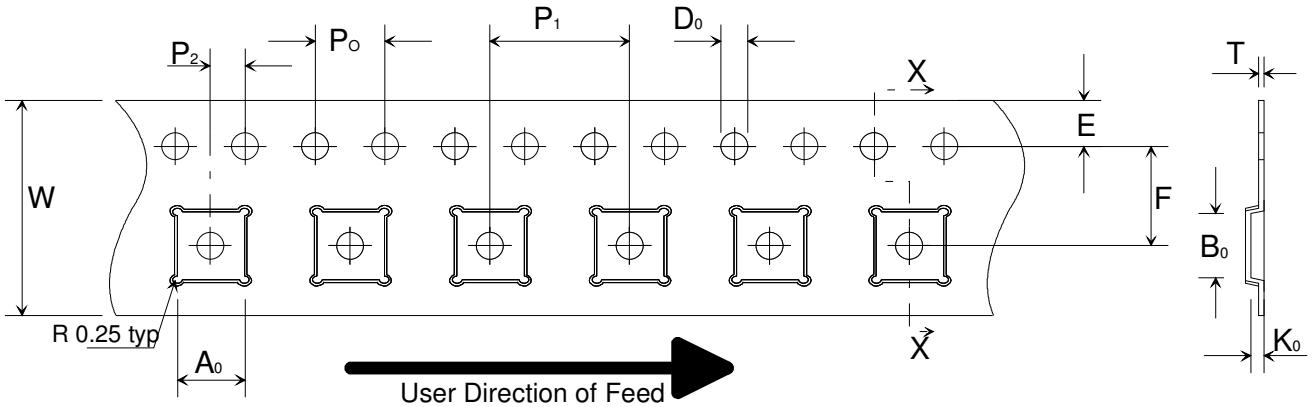
Dimensions do not include mold or interlead flash, protrusions or gate burrs.

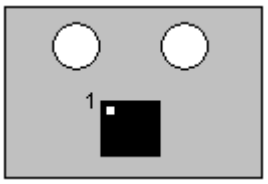
SOLDERING INFORMATION

◆ **For Lead-Free / Green QFN 4mm x 4mm**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS



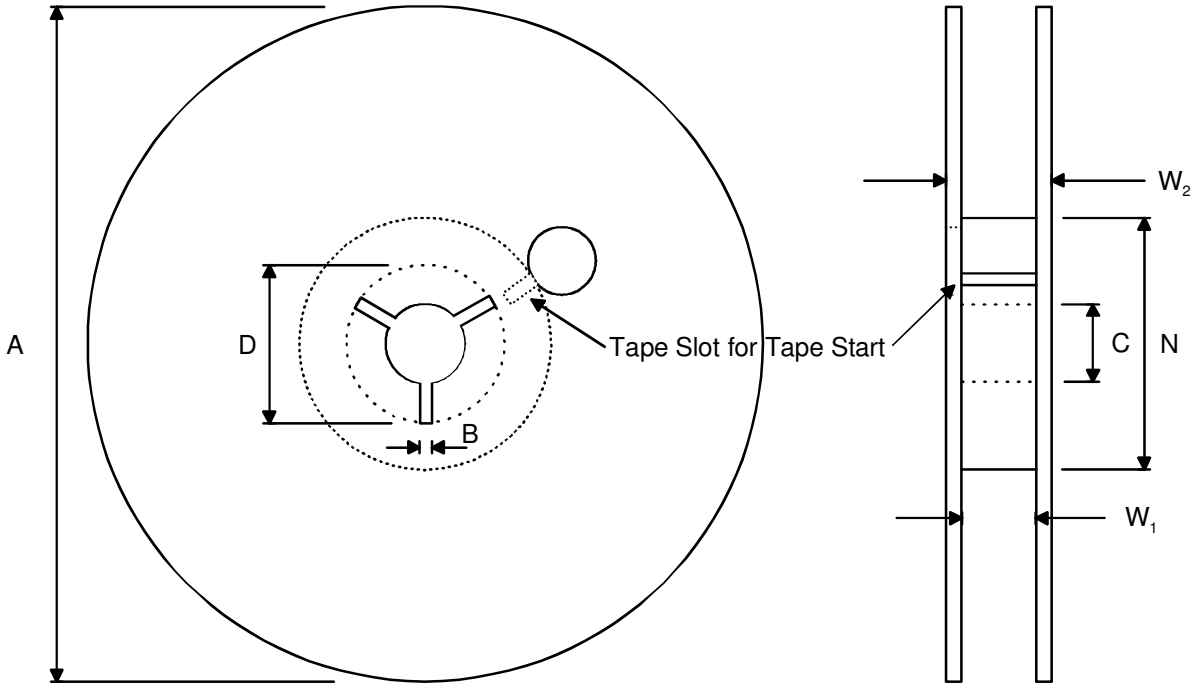


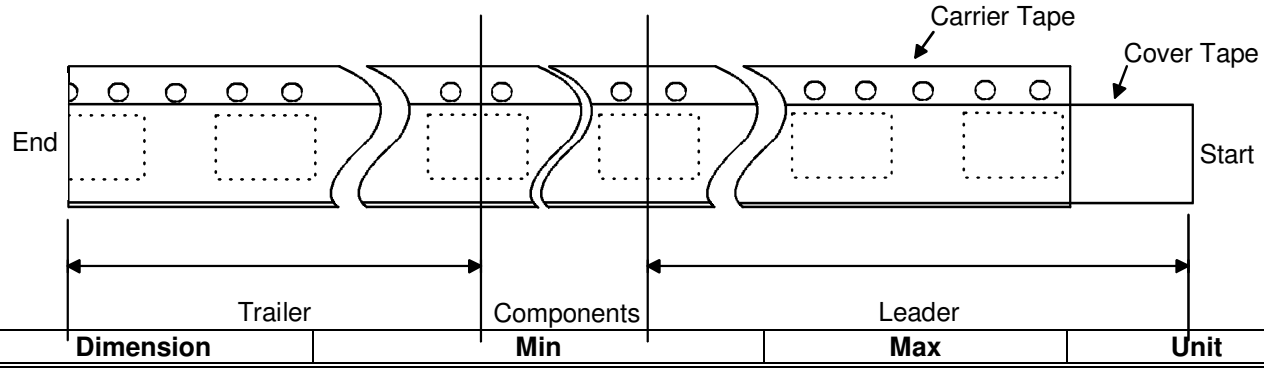
Orientation on tape

Dimension	Min/Max	Unit
A_o	4.30 ±0.10	mm
B_o	4.30 ±0.10	mm
D_o	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.05	mm
K_o	1.10 ±0.10	mm
P_o	4.0	mm
P_1	8.0 ±0.10	mm
P_2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

All dimensions in millimeters

REEL SPECIFICATIONS





Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	100		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative

ORDERING INFORMATION

Product Code	Product	Description
MAS6512AA1WAD00	Capacitive Sensor Signal Interface IC	EWS-tested wafer, thickness 370 µm
MAS6512AA1WAD05	Capacitive Sensor Signal Interface IC	Dies on waffle pack, thickness 370 µm
MAS6512AA1Q1706	Capacitive Sensor Signal Interface IC	QFN-16 4x4x0.75 Package, Pb-free, RoHS compliant, Tape & Reel, 1000 / 3000 pcs components on reel

Contact Micro Analog Systems Oy for other wafer thickness options.

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy Kutomotie 16 FI-00380 Helsinki, FINLAND	Tel. +358 10 835 1100 Fax +358 10 835 1119 http://www.mas-oy.com