Ethernet/IEEE 802.3 LAN Controller
Advance Data Sheet

FEATURES

- Integrated Controller, MENDEC and 10BASE-T solution for IEEE 802.3 Local Area Networks (LANs)
- CMOS technology, 5-volt supply
- No external precision components required
- Available in 84-pin PLCC and 100-pin PQFP

LAN Controller

- Supports industry standard 8-, 16-, and 32-bit microprocessor interfaces
- Offers three loopback modes:
  - Controller only
  - Controller and MENDEC
  - Controller, MENDEC, and transceiver
- 16-byte internal FIFO with programmable threshold control
- Contains two 16-bit DMA channels
- Provides network statistics storage
- Supports physical, multicast, and broadcast address filtering

MENDEC

- Provides Manchester encoding/decoding
- Provides 802.3 AUI media interface for 10BASE5 or the NCR92C392 10BASE2 transceiver
- Generates a receive clock from receive data
- External half- or full-step mode of operation at transmit output
- Internal 20 MHz system clock
- Tolerates up to ±20 ns jitter on incoming data

10BASE-T Transceiver

- Meets IEEE 10BASE-T standard for link integrity, AUI and twisted pair squelch, collision detection, SQE test, jabber, and AUI loopback
- High-speed receiver architecture minimizes jitter (patent pending)

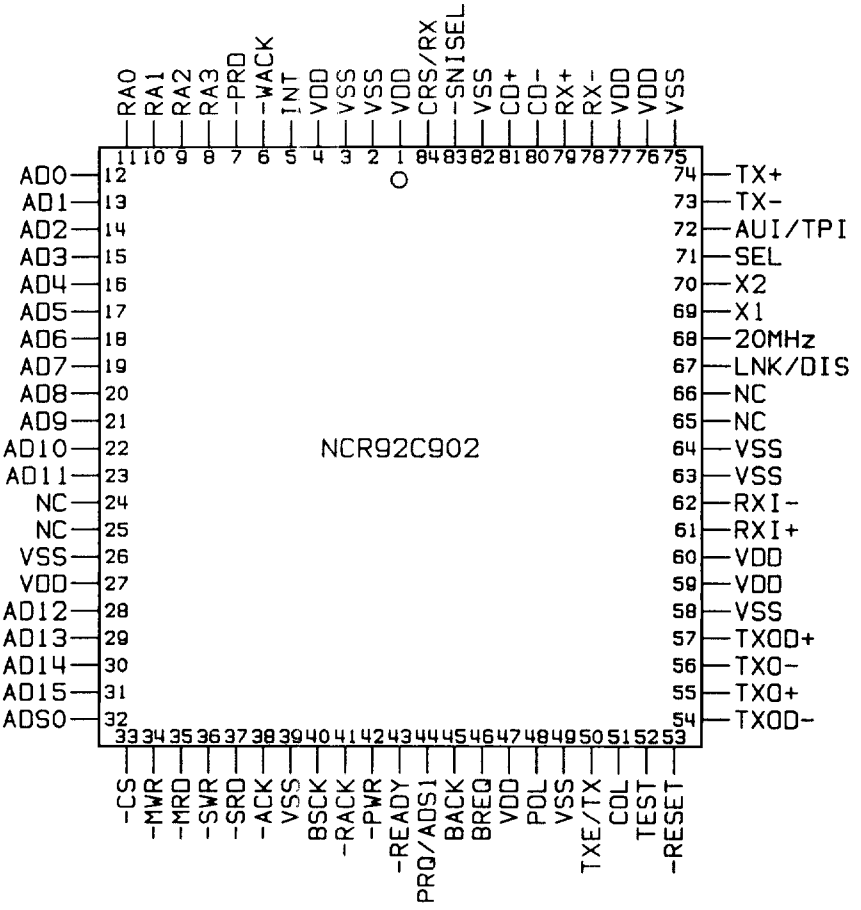


Figure 1 84-pin Plastic Leaded Chip Carrier (PLCC)

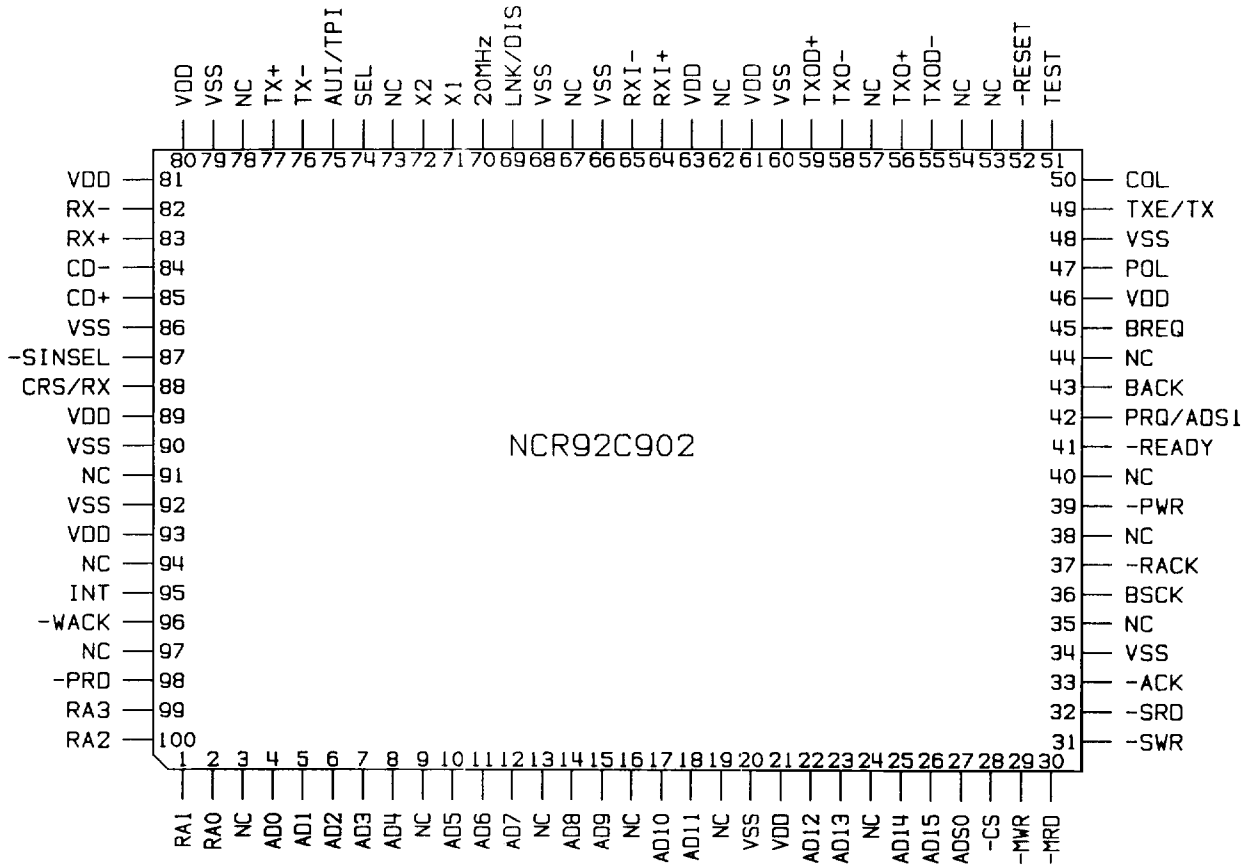


Figure 2 100-pin Plastic Quad Flat Pack (PQFP)

Pinout Summary

Signal Name	Type	Pin No.		Pin Descriptions
		84-pin PLCC	100-pin PQFP	
RA1	Input	10	1	Register Address
RA0	Input	11	2	Register Address
NC	–	–	3	No Connect
AD0	In/Out	12	4	Multiplexed Address/Data Bus
AD1	In/Out	13	5	Multiplexed Address/Data Bus
AD2	In/Out	14	6	Multiplexed Address/Data Bus
AD3	In/Out	15	7	Multiplexed Address/Data Bus
AD4	In/Out	16	8	Multiplexed Address/Data Bus
NC	–	–	9	No Connect
AD5	In/Out	17	10	Multiplexed Address/Data Bus
AD6	In/Out	18	11	Multiplexed Address/Data Bus
AD7	In/Out	19	12	Multiplexed Address/Data Bus
NC	–	–	13	No Connect
AD8	In/Out	20	14	Multiplexed Address/Data Bus

Pinout Summary [continued]

Signal Name	Type	Pin No.		Pin Descriptions
		84–pin PLCC	100–pin PQFP	
AD9	In/Out	21	15	Multiplexed Address/Data Bus
NC	–	–	16	No Connect
AD10	In/Out	22	17	Multiplexed Address/Data Bus
AD11	In/Out	23	18	Multiplexed Address/Data Bus
NC	–	24	19	No Connect
NC	–	25	–	No Connect
VSS	Ground	26	20	Ground
VDD	Power	27	21	Power
AD12	In/Out	28	22	Multiplexed Address/Data Bus
AD13	In/Out	29	23	Multiplexed Address/Data Bus
NC	–	–	24	No Connect
AD14	In/Out	30	25	Multiplexed Address/Data Bus
AD15	In/Out	31	26	Multiplexed Address/Data Bus
ADS0	In/Out	32	27	Address Strobe 0
–CS	Input	33	28	Chip Select (active low)
–MWR	Output	34	29	Master Write Strobe (active low)
–MRD	Output	35	30	Master Read Strobe (active low)
–SWR	Input	36	31	Slave Write Strobe (active low)
–SRD	Input	37	32	Slave Read Strobe (active low)
–ACK	Output	38	33	Acknowledge (active low)
VSS	Ground	39	34	Ground
NC	–	–	35	No Connect
BSCK	Input	40	36	Bus Clock
–RACK	Input	41	37	Read Acknowledge (active low)
NC	–	–	38	No Connect
–PWR	Output	42	39	Port Write (active low)
NC	–	–	40	No Connect
–READY	Input	43	41	Ready (active low)
PRQ/ADS1	Output	44	42	Port Request/Address Strobe 1
BACK	Input	45	43	Bus Acknowledge
NC	–	–	44	No Connect
BREQ	Output	46	45	Bus Request
VDD	Power	47	46	Power
POL	Output	48	47	Polarity
VSS	Ground	49	48	Ground
TXE/TX	Output	50	49	Transmit Enable/Transmit
COL	Output	51	50	Collision
TEST	Input	52	51	TEST should be tied low for normal operation.
–RESET	Input	53	52	Reset (active low)
NC	–	–	53	No Connect
NC	–	–	54	No Connect
TXOD–	Output	54	55	Twisted Pair Transmit Output Delay Minus
TXO+	Output	55	56	Twisted Pair Transmit Output Plus
NC	–	–	57	No Connect
TXO–	Output	56	58	Twisted Pair Transmit Output Minus
TXOD+	Output	57	59	Twisted Pair Transmit Output Delay Plus

Pinout Summary [continued]

Signal Name	Type	Pin No.		Pin Descriptions
		84-pin PLCC	100-pin PQFP	
VSS	Ground	58	60	Ground
VDD	Power	59	61	Power
NC	–	–	62	No Connect
VDD	Power	60	63	Power
RXI+	Input	61	64	Twisted Pair Receive Input Plus
RXI–	Input	62	65	Twisted Pair Receive Input Minus
VSS	Ground	63	66	Ground
NC	–	–	67	No Connect
VSS	Ground	64	68	Ground
NC	–	65	–	No Connect
NC	–	66	–	No Connect
LNK/DIS	In/Out	67	69	Link/Link Disable
20 MHz	Output	68	70	20 MHz signal
X1	Input	69	71	Crystal or External Oscillator input
X2	Output	70	72	Crystal feedback output
NC	–	–	73	No Connect
SEL	Input	71	74	Mode Select
AUI/TPI	Input	72	75	AUI/TPI Select
TX–	Output	73	76	AUI Transmit Minus
TX+	Output	74	77	AUI Transmit Plus
NC	–	–	78	No Connect
VSS	Ground	75	79	Ground
VDD	Power	76	80	Power
VDD	Power	77	81	Power
RX–	Input	78	82	AUI Receive Minus
RX+	Input	79	83	AUI Receive Plus
CD–	Input	80	84	AUI Collision Input Minus
CD+	Input	81	85	AUI Collision Input Plus
VSS	Ground	82	86	Ground
–SNISEL	Input	83	87	–SNISEL should be tied high for normal operation
CRS/RX	Output	84	88	Carrier Sense/Receive
VDD	Power	1	89	Power
VSS	Ground	2	90	Ground
NC	–	–	91	No Connect
VSS	Ground	3	92	Ground
VDD	Power	4	93	Power
NC	–	–	94	No Connect
INT	Output	5	95	Interrupt
–WACK	Input	6	96	Write Acknowledge (active low)
NC	–	–	97	No Connect
–PRD	Output	7	98	Port Read (active low)
RA3	Input	8	99	Register Address
RA2	Input	9	100	Register Address

DESCRIPTION

The NCR92C902 is designed to interface with CSMA/CD (Carrier Sense Multiple Access with Collision Detection) local area networks. The NCR92C902 supports the IEEE 802.3 standard including 10BASE5, 10BASE2, and 10BASE-T. The NCR92C902 provides the Media Access Control (MAC), Manchester Encoder/Decoder (MENDEC) with an Attachment Unit Interface (AUI) and 10BASE-T transceiver.

The NCR92C902 provides Media Access Control (MAC) for efficient packet transmission and reception control by using unique, dual DMA channels and an internal FIFO. Bus arbitration and memory control logic are integrated to reduce board cost.

The integrated MENDEC allows Manchester encoding and decoding through a differential transceiver and phase-lock-loop decoder at 10 Mbit/sec. The MENDEC includes an integrated crystal-controlled oscillator, collision detector, and loopback diagnostics. The MENDEC interfaces directly to the transceiver, and supports IEEE-compatible AUI for connection to other media transceivers.

The 10BASE-T transceiver includes the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity as defined in the IEEE standard. When combined with transmit/receive filters, equalization resistors, and pulse transformers, the transceiver provides a complete physical interface between the MENDEC and the twisted pair medium.

The NCR92C902 provides an integrated solution for 10BASE-T IEEE 802.3 networks. It is designed for easy access to other transceivers through the AUI interface. For 10BASE5 and 10BASE2 applications, isolation is required at the AUI differential signal interface.

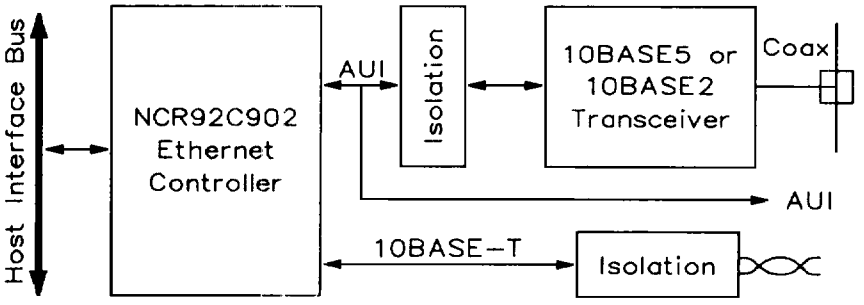


Figure 3 System Block Diagram

PIN DESCRIPTIONS

The pin descriptions are grouped into the bus interface pins and the network interface pins. For timing information related to these signals, refer to the AC Characteristics section.

BUS INTERFACE PINS

-ACK: Acknowledge
This active-low output allows the host to access the NCR92C902 when active. During a register read/write cycle, the NCR92C902 holds -ACK high until the host is synchronized with the NCR92C902.

AD(15:0): Multiplexed Address/Data bus
These sixteen input/output pins multiplex the address and data in and out of the NCR92C902 during host and bus master accesses.

When the host is accessing the NCR92C902 (register accesses and setup), the lower eight bits of this bus, AD(7:0), are used to transfer the register data. AD(15:8) float during host accesses. Refer to the descriptions for -SRD, -SWR, -CS, ADS0, RA(3:0), and -ACK for more details on this operation.

When the NCR92C902 is in the bus master mode, these 16 pins are used by the on-chip DMA controllers to multiplex addresses and data to and from the buffer RAM. Refer to the descriptions for BACK, -MWR, and -MRD, for more details on this operation.

ADS0: Address Strobe 0
This input/output pin has two functions. As an input during register accesses by the host, the falling edge of this signal latches the RA(3:0) inputs into the NCR92C902. If this line remains high, the value on RA(3:0) specifies the register address, but is not latched.

As an output during bus master mode (DMA), this signal latches the address from the AD(15:0) bus.

BACK: Bus Acknowledge
When this active-high input is asserted, the NCR92C902 has control of the bus. BREQ can be tied to BACK for the fastest bus accesses by the NCR92C902, but this may impact host performance. Do not tie this signal high; the NCR92C902 would never release the bus.

BREQ: Bus Request
This active-high output is used in the bus master mode by the NCR92C902 to request the bus. This signal is asserted when the FIFO needs service. Refer to the pin description for BACK.

BSCK: Bus Clock
This input controls the bus master logic. Four clock cycles are typically used for a normal DMA data transfer, but can be extended by using the -READY input.

-CS: Chip Select
When this input is low, the NCR92C902 registers are accessed by the host. Refer to the descriptions for AD(15:0), RA(3:0), -SWR, -SRD, and ADS0 for more information.

INT: Interrupt
When this output is high, one or more flags in the Interrupt Status Register (ISR) are set high. This signal is cleared low by clearing the ISR bits (by writing to the ISR).

-MRD: Master Read Strobe
This active-low output goes low during DMA read operations. Data transferred to the NCR92C902 during this read must be valid on the rising edge of -MRD. This output is in the high impedance state when not in the bus master mode (BACK high).

-MWR: Master Write Strobe
This active-low output goes low during NCR92C902 DMA write operations. Data output from the NCR92C902 during this write is valid on the rising edge of this signal. This output is in the high impedance state when not in the bus master mode (BACK high).

-PRD: Port Read
This active-low output is used during remote write operations from the host to local RAM on the local bus. When -PRD is low, data from a latch is expected on the local bus for latching by the local RAM.

PRQ/-ADS1: Port Request/Address Strobe 1
This output functions as Port Request in the 16-bit addressing mode, or Address Strobe 1 in the 32-bit addressing mode. This signal remains in the high impedance state until the Data Configuration Register (DCR) is set. PRQ/-ADS1 is in the high impedance state when not in the bus master mode (BACK high).

PRQ is specified when the LAS bit in the DCR is set low (16-bit addressing). This signal is asserted high during remote bus master transfers to initiate a single DMA transfer.

-ADS1 is specified when the LAS bit is set high (32-bit addressing). This signal is used to externally latch the high address lines, A(31-16). Data is valid on the rising edge of -ADS1. Refer to the description for AD(15:0). A(31:16) are fixed values stored in the Remote Start Address Registers (RSAR0 and RSAR1).

-PWR: Port Write
This active-low output externally latches data from NCR92C902 during remote bus master read operations to local RAM. Data is valid on the rising edge of this signal.

RA(3:0): Register Address
These inputs specify which register the host is accessing within the NCR92C902. Refer to the descriptions for AD(15:0), -CS, -SWR, -SRD, and ADS0 for more information.

-RACK: Read Acknowledge
This active-low input, when low, indicates to the NCR92C902 that the external latch containing the data to be read by the host has been read. The NCR92C902 is then free to update the latch.

-READY: Ready
When this active-low input is high, the NCR92C902 continues to extend the bus master memory cycle.

-RESET: Reset
This active-low input immediately places the NCR92C902 in the reset state. No activity occurs on the media from this device until the Command Register is initialized. The NCR92C902 completes the reset cycle after 10 BSCK cycles. -RESET initializes the following registers: Command, Interrupt Mask Register (IMR), Data Configuration Register (DCR) and the Transmit Configuration Register (TCR).

-SRD: Slave Read Strobe
This active-low input strobes register data out of the NCR92C902 during host reads. Refer to the descriptions for AD(15:0), RA(3:0), -CS, -SWR, and ADS0.

-SWR: Slave Write Strobe
This active-low input signals the NCR92C902 that a write by the host is occurring. The NCR92C902 latches the data into the register on the rising edge of -SWR. Refer to the descriptions for AD(15:0), RA(3:0), -CS, -SRD, and ADS0.

-WACK: Write Acknowledge
This active-low input signals the NCR92C902 that data is available to be transferred into the local memory during bus master mode. The host drives -WACK low to indicate it has written the external latch with the data.

NETWORK INTERFACE PINS

AUI/TPI: AUI/TPI Select
This TTL level input selects either the AUI or the TPI (10BASE-T) interface for operation with the MENDEC circuitry. When this input is high, the AUI is selected. When this input is low, the TPI is selected.

CD+/-: Collision Plus and Minus
This differential input pair receives the AUI collision input from the transceiver. When active, they inform the NCR92C902 that a collision is occurring

COL: Collision
This TTL/MOS active-high output is asserted for approximately 50 ms whenever the NCR92C902 detects a collision in either the AUI or the TPI modes.

CRS/RX: Carrier Sense/Receive
This TTL/MOS active-high output is asserted for approximately 50 ms whenever valid transmit

or receive data is detected while in AUI mode or receive data is detected while in TPI mode.

LNK/DIS: Link/Link Disable
This input/output signal performs two link-related functions. Its function is determined on the rising edge of the -RESET signal. If LNK/DIS is tied low, the LINK function is disabled and LINK integrity checking is disabled. If the internal pull-up resistor pulls this signal high, it functions as the LINK indicator signal for driving an LED.

As an output this pin is configured as an open drain N-channel device and is capable of driving an LED (a green-colored LED is recommended). It will be configured as an output if connected to an LED or left floating. Under normal operating conditions (LINK is continuously detected on the twisted pair) the output will be low and the LED will be lit. The open drain output will go high (turning off the LED) if the twisted pair LINK is not detected. This output will be pulled high in AUI mode by an internal 15 kΩ resistor.

POL: Polarity
This TTL/MOS active-high output is normally low. POL is asserted when the TPI circuitry detects seven consecutive link pulses or three consecutive received packets with reversed polarity.

RX+/-: AUI Receive Plus and Minus
This differential input pair receives the AUI receiver input from the transceiver and sends it to the MENDEC circuitry.

RXI+/-: Twisted Pair Receive Inputs
This input pair receives 10BASE-T data from the media (through transformers). It is then fed into the TPI circuitry within the NCR92C902.

SEL: Mode Select
This pin allows the system designer to specify Ethernet I or IEEE 802.3 modes of operation. For IEEE 802.3 operation, tie this input high and TX+ and TX- will have the same voltage during the idle state. For Ethernet I operation, tie this signal low and TX+ and TX- will have the opposite voltage during idle.

-SNISEL: Test Select
This input is used for testing during manufacturing. For normal operation, -SNISEL must be tied high.

TEST: Test
This input is used for testing during manufacturing. For normal operation, TEST must be tied low.

20 MHz: 20 MHz signal
This TTL/MOS level signal is a buffered version of the oscillator X2 and is suitable for driving external logic.

TX+/-: AUI Transmit Plus and Minus
This differential output pair sends the AUI transmit data to the transceiver from the MENDEC circuitry.

TXE/TX: Transmit Enable/Transmit
This TTL/MOS active-high output is asserted for approximately 50 ms whenever the NCR92C902 transmits data in either AUI or TPI modes.

TXO+/-, TXOD+/-: Twisted Pair Transmit Out
These high drive CMOS level outputs are used to transmit TPI data to the media via transformers. They are resistively combined externally to produce a differential output signal with equalization to compensate for intersymbol interference on the twisted pair medium.

X1: Crystal or External Oscillator
On the NCR92C902-C, this input is used along with X2 to connect a 20 MHz crystal to the internal oscillator, or as the input for an external 20 MHz TTL clock with X2 left floating. On the NCR92C902-T, only a 20 MHz TTL clock is supported.

X2: Crystal Feedback
On the NCR92C902-C, this output provides the feedback to a crystal when the internal oscillator is being used. With the NCR92C902-C, this pin must be left floating when a TTL clock is used. On the NCR92C902-T, this output is left internally floating, so the pin may be grounded, left floating, or tied high.

FUNCTIONAL DESCRIPTION

The NCR92C902 consists of three primary sections: the LAN Controller, the Manchester Encoder/ Decoder, and the Twisted Pair Transceiver.

LAN CONTROLLER

The primary logical functions of the LAN Controller are shown on the left side of Figure 4.

- Receiver
- Transmitter
- DMA Control
- FIFO Logic
- Protocol Control
- Backoff Timers
- Bus Interface
- Multiplexer

Receiver

The receiver translates incoming NRZ serial data to standard data using the receive clock when the –CS input is asserted. The received data is byte–aligned by detecting the Start of Frame Delimiter (SFD). The data byte is placed in the internal 16–byte FIFO and the Receive Byte Count register is incremented. The first six bytes after the Start of Frame Delimiter are address fields which are checked by internal logic to validate further receptions. If the address field is not valid for receptions, the packet is discarded and the FIFO is cleared. During reception, a CRC for the incoming data packet is generated. If the CRC does not match the received CRC, an error condition is detected and the packet rejected. The first six bytes of the received packet (destination address field) is compared to the physical address registers. If they do not match, the packet is rejected. Multicast and broadcast addresses can also be used.

Transmitter

The data waiting for transmission is placed in the internal FIFO and shifted out with the most significant bit first. The Transmit Clock (TXC) is generated by the MENDEC logic. The transmitter appends 62 bits of preamble and a synchronization pattern prior to each packet transmission. The transmitted data is also routed to the internal CRC generator. After the last byte of the packet has been transmitted, the 32–bit FCS field is shifted out of the CRC logic directly. If the LAN Controller detects a collision during transmission, a 32–bit JAM pattern of all ones is generated.

DMA Control

The NCR92C902 contains two 16–bit DMA channels: a local DMA channel and a remote DMA channel. During reception, the local DMA stores received packets in a receive buffer ring which is located in the local buffer memory. During transmission, the local DMA channel transfers packets from local buffer memory to an internal FIFO. The remote DMA channel is used as a slave DMA to transfer data between the local buffer memory and the host system. The local DMA channel has higher internal priority than the remote DMA channel and this is internally arbitrated. External arbitration is performed with a standard bus request, acknowledge handshake protocol. Both DMA channels use a common external bus clock to generate all required bus timing.

FIFO and FIFO Control Logic

A 16–byte FIFO buffer is built into the NCR92C902. The threshold of the FIFO is programmable. The local DMA channel transfers the bytes (or words) contained in the FIFO into local memory when this threshold is reached. The local DMA must be given access to the bus within a minimum bus latency time to avoid a FIFO underflow (or overflow).

These FIFO underflows or overflows are caused by either 1) the bus latency is is too long and the FIFO has filled (or emptied) from the network before the local DMA has serviced the FIFO or 2) the bus latency has slowed the local DMA channel to a point where it is slower than the network data rate of 10 Mbit per second. Number 2 is also dependent upon DMA clock and word length (byte or word). The overall bus latency can be limited in the worst case condition. The NCR92C902 can tolerate this condition.

The FIFO control logic flags an overflow as the 13th byte is written into the buffer. This is to assure that data will not be overwritten and short-

ens the the FIFO to 13 bytes. The FIFO operates differently dependent upon whether byte or word mode is being used. In byte mode, a threshold is indicated when the n+1 byte has entered the FIFO. For example, with a threshold set for 8 bytes a BREQ will be issued when the 9th byte has entered the FIFO. In word mode BREQ is generated when n+2 bytes have entered the FIFO. For a 4 word threshold (same as 8 bytes), BREQ is asserted when the 10th byte has entered the FIFO.

The FIFO must not be read during normal operation and should be read only during loopback diagnostic operations. Under normal operation, the NCR92C902 will not issue an ACK back to the host if the FIFO is read.

Transmit and Receive

Prior to transmitting, a prefetch from memory is performed to load the FIFO with the number of bytes equal to the programmed FIFO threshold. The next BREQ will not be asserted until after transmission of data has begun (after SFD).

When reception begins, the entire address field of each incoming packet is stored in the FIFO for comparison with the NCR92C902's physical address registers or one of the multicast registers. This causes the FIFO to accumulate 8 bytes. There are also some synchronization delays in the DMA PLA. The actual time to to the BREQ being issued from the time the SFD is detected is 7.8 µs. This operation affects the bus latencies at 2- and 4-byte thresholds during the first receive BREQ since the FIFO must be filled to 8 bytes (or 4 words) before issuing a BREQ.

The NCR92C902 enters its end of packet processing sequence when the MENDEC detects the end of a packet. The NCR92C902 holds the bus and the FIFO is emptied and status information is written at the beginning of the packet. The longest time that BREQ may be extended occurs when a packet ends just as the last FIFO burst is performed. A programmed burst transfer is then performed followed by flushing the remaining bytes in the FIFO, and the header information is written to memory.

During this sequence, BREQ is issued because the FIFO threshold has been reached. BREQ is extended because the packet ends during the burst. The remaining bytes are then flushed from the FIFO and the NCR92C902 prepares to write the 4-byte (2-word) header into memory. The BREQ is then canceled.

Protocol Control

The protocol logic fully implements the IEEE 802.3 protocol. Collision recovery and random back-off logic is also implemented. This circuitry also formats packets in the transmission mode and strips preamble and synch in the receiving mode.

Backoff Timers

When a collision condition occurs, the NCR92C902 stops transmission, waits for a random period of time, and starts transmission again. The waiting period is determined by the back-off timers.

Bus Interface

The bus interface generates all bus interface signals necessary for DMA operations, bus request and bus acknowledge handshake protocol.

Multiplexer

The multiplexer is used to multiplex address and data bus contents at various bus cycles.

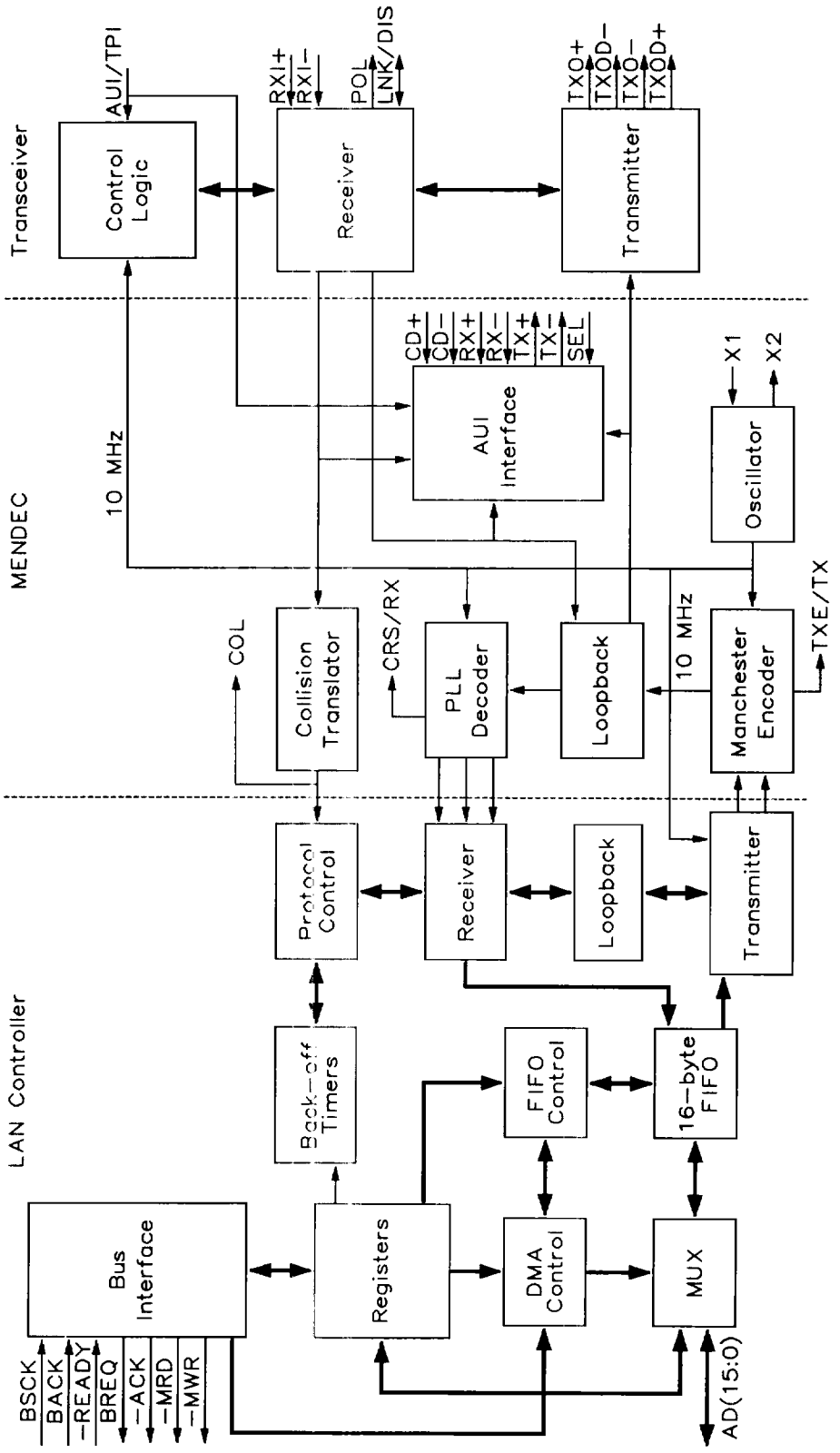


Figure 4 Chip Block Diagram

MANCHESTER ENCODER/DECODER

The Manchester Encoder/Decoder consists of the following. Refer to Figure 4.

- 20 MHz Crystal Oscillator
- Transmitter/Encoder
- Receiver/Decoder
- Collision Translator

Oscillator

A 20 MHz parallel resonant crystal or a 20 MHz TTL clock is used to control the oscillator that provides the 20 MHz clock signal. An internal divide-by-two counter generates the 10 MHz clock for the controller. The oscillator also provides internal clock signals to the encoding and decoding circuits.

The NCR92C902-C has an on-chip oscillator that operates with a crystal across X1 and X2, or with a TTL clock on X1 if X2 is left floating. For optimal performance, the total crystal load capacitance should not exceed 20 pF. The NCR92C902-T requires a TTL clock to drive X1, and X2 can be left floating or grounded.

Transmitter/Encoder

When transmitting, the NCR92C902 combines clock pulses and the non-return-to-zero (NRZ) data from the controller and generates Manchester encoded data which is sent to the transceiver. The first half of the bit cell of a Manchester code contains the complement of the data and the second half contains the data, so a transition is always guaranteed in the middle of a bit cell.

The differential transmit pair (TX+/-) drives up to 50 meters of twisted pair AUI cable through an isolation transformer. These output pins are source followers which require two 270 Ω pulldown resistors to ground.

The NCR92C902 allows half-step and full-step functions to be compatible with the original Ethernet, Version 1.0, and IEEE 802.3 specifications. With the SEL signal low (for the original Ethernet), TX+ is positive with respect to TX- during the idle state. With SEL high (for the IEEE 802.3 specifications), TX+ and TX- are equal in the idle state. This provides zero differential voltage to operate with transformer coupled loads.

Receiver/Decoder

The decoder consists of a differential receiver to sense the signal on the transceiver cable and a Phase-Locked Loop (PLL) to lock onto the preamble of the incoming signal. The differential inputs (RX+/-) must be externally terminated with two 39 Ω resistors connected in series if the standard 78 Ω transceiver drop cable is used. In thin Ethernet applications, these resistors are optional.

The carrier receiver detects the presence of an incoming data packet by discerning and rejecting noise from expected Manchester data. Transient noise with pulses less than 30 ns or signals with negative peaks smaller than -175 mV are rejected by the receiver. Carrier is detected for input signals with pulse widths of more than 30 ns and less than -300 mV. Data typically becomes valid within 5 bit times.

The NCR92C902 tolerates jitter up to 20 ns in the receive data. The decoder detects the end of a frame when no mid-bit transitions are detected within 1.5 bit-times after the last bit. The receive clock stays active five more bit-times after the end of the receive frame to guarantee the receive timing on the controller.

Collision Translator

A transceiver detects collision on the network and generates a 10 MHz signal on the CD+/- inputs. This collision signal passes through an input stage that detects signal levels and pulse duration (the same way as the differential receive inputs). When a collision is detected, the NCR92C902 stops its current transmission and transmits again later.

The differential collision inputs are terminated in the same manner as the differential receive inputs. The squelch function also rejects pulses with levels less than -175 mV.

TWISTED PAIR INTERFACE

The NCR92C902 supports complete 10BASE-T functionality and includes the following features:

- Collision Detection
- Jabber Detection
- Squelch Logic
- Link Integrity
- Polarity Detection and Correction

Collision Detection

A collision is sensed by the NCR92C902 when the transmit and receive channels are active simultaneously. The NCR92C902 signals the occurrence of a collision to the MENDEC circuitry internally and externally by driving the COL pin high. Collisions will not be reported when the device is in a link-fail state. COL is also active when the device has detected a jabber condition.

Jabber Detection

The jabber is a self-interrupt function that keeps a damaged node from continuously transmitting on the network. The NCR92C902 will isolate a "jabbering" DTE from the network if it surpasses a 26.2 ms maximum allowed transmit time. If a transmission exceeds this duration, the jabber function inhibits transmission (except for link pulses) and sends a collision signal on COL. The NCR92C902 releases the jabber state after the DTE has been idle for at least 420 ms.

Squelch Logic

The twisted pair squelch circuitry dynamically adjusts the sensitivity of the twisted pair data comparator and the threshold levels of the dual twisted pair receiver peak detectors. Before signals begin to arrive on the RXI+/- twisted pair circuit, the NCR92C902 is in a high noise rejection, squelch state. When in a squelch state, no data is received. To qualify incoming data, the smart squelch circuitry monitors the peak detectors for three peaks of alternating polarity that occur within a 400 ns window. Once a signal has been qualified by the squelch circuitry, the NCR92C902 assumes an unsquelch state and reduces the peak detector threshold.

If the NCR92C902 detects activity on the twisted pair RXI+/- circuit while the DTE is transmitting, a collision condition is occurring. In this case, incoming data is qualified by the squelch circuitry on five peaks of alternating polarity within a 600 ns window. This provides additional protection against false collisions from impulse noise that may exist on the twisted pair cable caused by cross-talk and nearby electrical equipment.

The twisted pair smart squelch circuitry is returned to a squelch state by any of these conditions:

- A normal Start-of-Idle (SOI) signal
- An inverted SOI signal
- A missing SOI signal

Link Integrity

During periods of inactivity, positive link pulses 100 ns wide are generated and received every 13 ms by both MAUs at either end of the twisted pair to ensure that the cable has not been broken or shorted. The NCR92C902 assumes a link-good state if it detects valid link-pulse activity on the twisted pair receive circuit. If no link pulse (positive or negative) or no receive data is seen on the receive circuit for 105 ms, the NCR92C902 enters a link-fail state. If a link-fail condition occurs, four consecutive positive link pulses (or eight negative link pulses) must be received before a link-good condition is resumed. Only link pulses spaced greater than 3 ms and less than 105 ms are considered valid.

In a link-fail state, the NCR92C902 disables normal Transmit, Receive, AUI loopback, and Collision. NOTE: The reception of a packet will place the device in a link-good state, but the packet will not be accepted. Subsequent packets will be transferred normally as long as the device remains in a link-good state.

Polarity Detection/Correction

Because twisted pair differential signals can be inverted due to wiring errors, the NCR92C902 incorporates polarity detection and correction circuitry. This circuitry monitors the twisted pair receiver to determine if normal or inverted data is being received. This is performed by an algorithm that monitors the polarity of the received start-of-idle (SOI) and link pulses. If the signal is inverted, the NCR92C902 automatically corrects the data internally and no wiring correction is necessary. If a polarity inversion is detected, the POL output is asserted high from its normally low state. The autopolarity function is reset on power-up or when a link failure is detected. For this reason, the autopolarity function should be disabled if the link integrity function is disabled.

Status Information

The NCR92C902 provides status information on the CRS/RX, TXE/TX, LNK/DIS, COL, and POL outputs. These pins are all suitable for driving LED indicators. All LED drivers except POL and LNK/DIS have a stretched time constant of 26.2 ms to ensure that the LED annunciation can be visually detected.

Power On Reset

The NCR92C902 uses a power-on-reset sequence to place itself into a known digital state, to allow the analog sections to stabilize, and to calibrate the internal delay line.

TYPICAL TPI CONNECTION

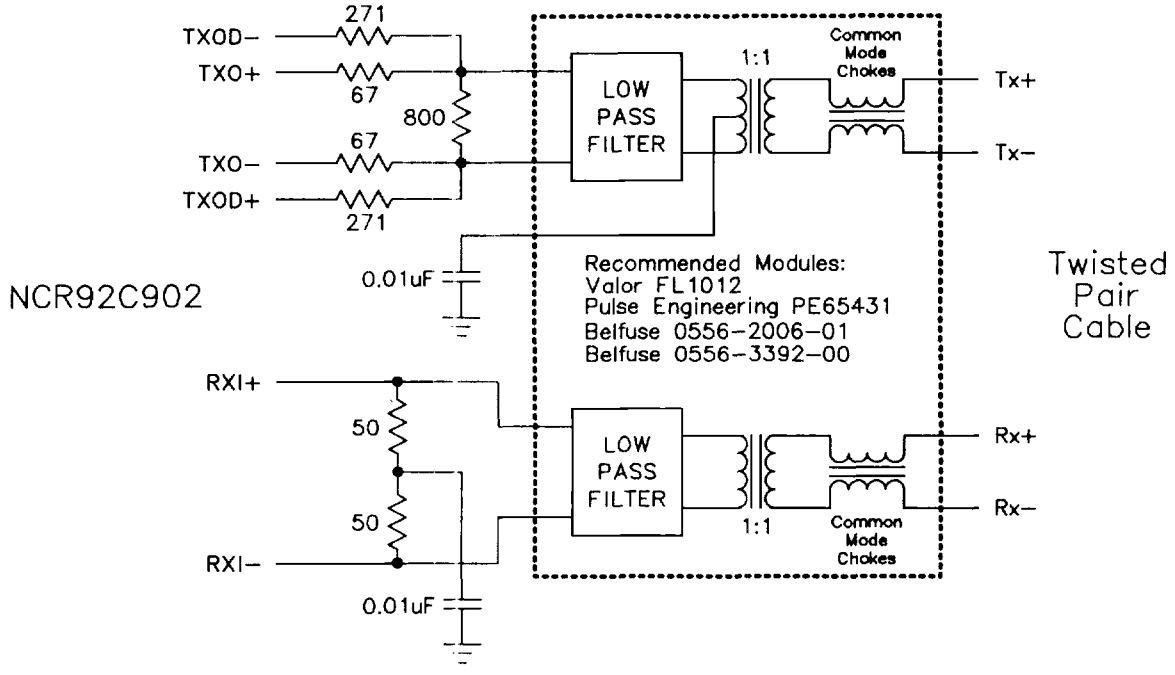
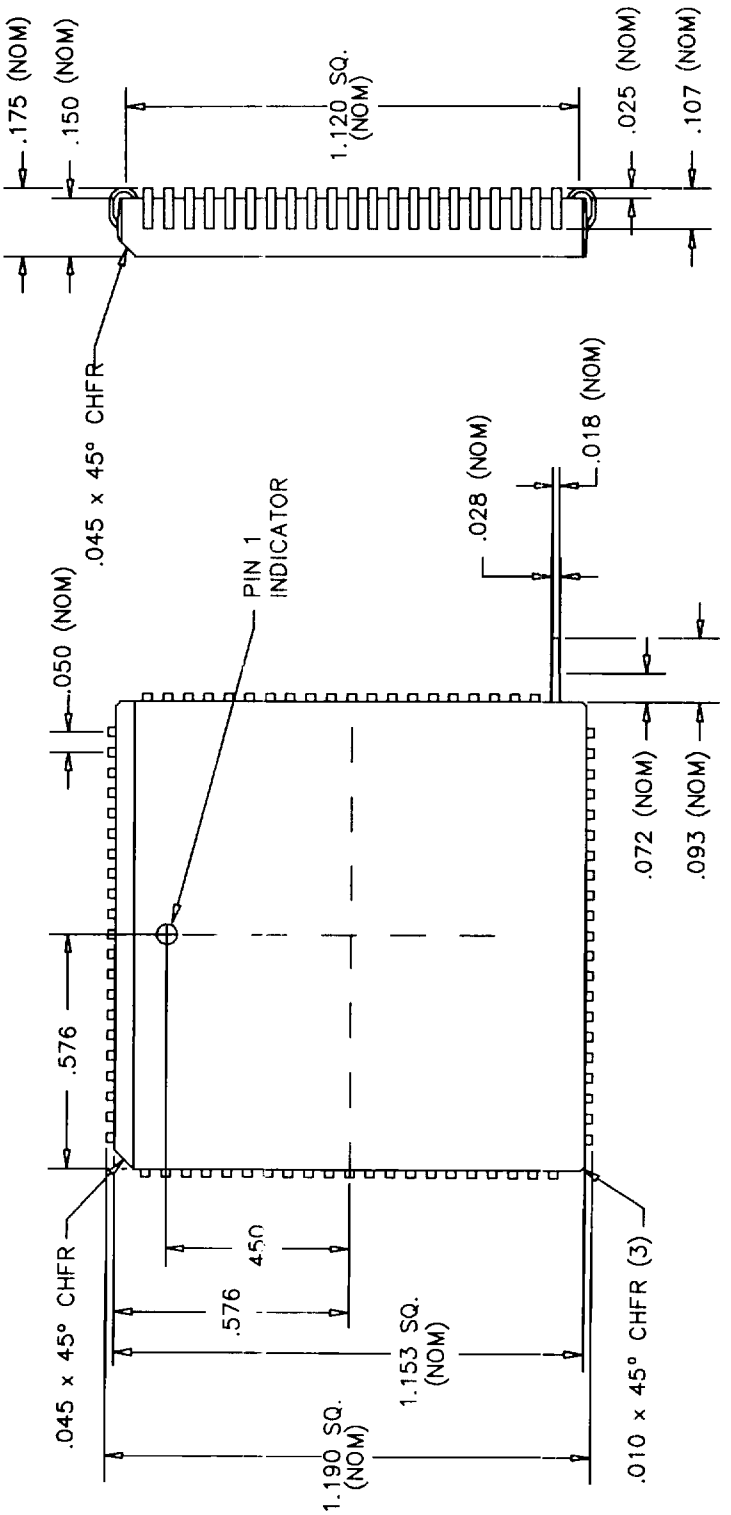
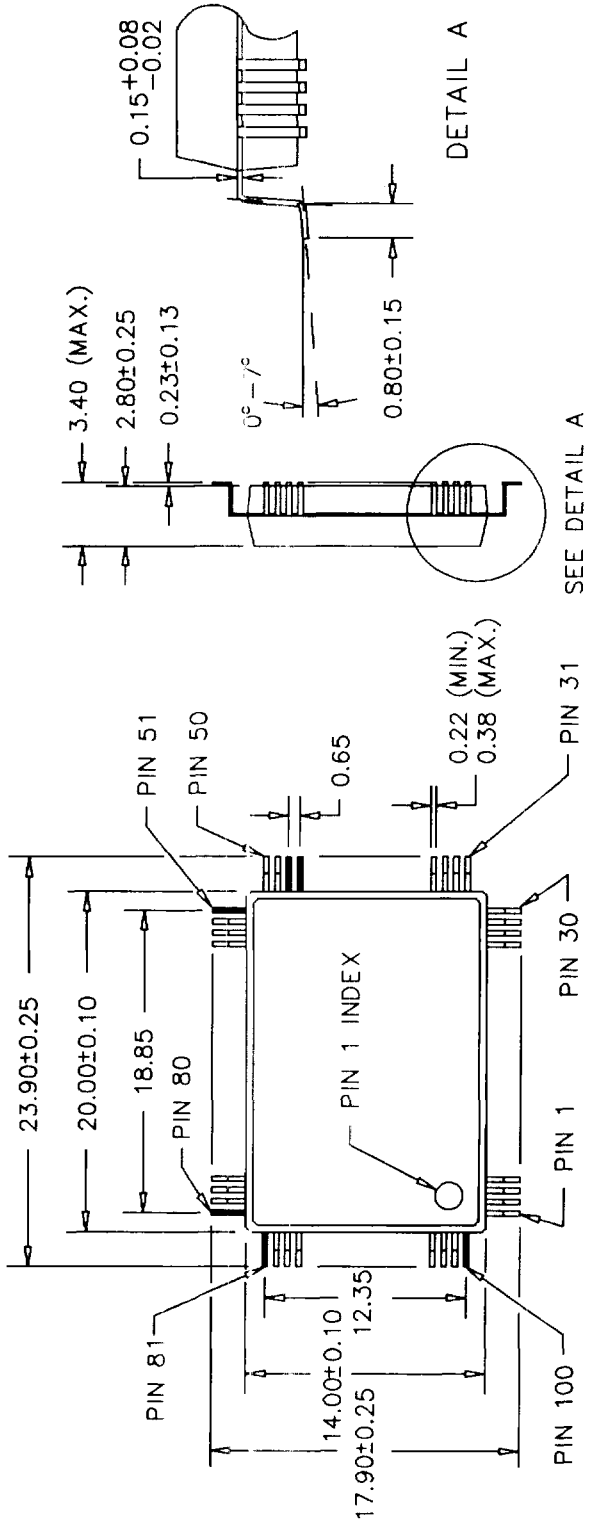


Figure 5 Twisted Pair Cable Connection

MECHANICAL SPECIFICATIONS



NOTE : All dimensions are in inches.



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

ORDERING INFORMATION

The NCR92C902 is available in two versions.

1. The NCR92C902-C has an on-chip oscillator that operates with a crystal across X1 and X2, or with a TTL clock on X1 if X2 is left floating.
2. The NCR92C902-T requires a TTL clock to drive X1, and X2 can be left floating or grounded.

Each version of the NCR92C902 is available in an 84-pin Plastic Leaded Chip Carrier (PLCC) and a 100-pin Plastic Quad Flat Pack (PQFP). Use the following part numbers to order the part.

Package Type	Part Number
84-pin PLCC	NCR92C902-T-84PL
84-pin PLCC	NCR92C902-C-84PL
100-pin PQFP	NCR92C902-T-100QFP
100-pin PQFP	NCR92C902-C-100QFP

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUMS

Symbol	Parameter	Minimum	Maximum	Units
T_A	Ambient Temperature	0	70	°C
T_S	Storage Temperature	−55	125	°C
V_{DD}	Supply Voltage	−0.5	7.0	V
V_{IN}	Input Voltage	−0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage	−0.5	V_{DD} + 0.5	V
T_L	Lead Temperature (Soldering 10 seconds maximum)		250	°C
PD	Power Dissipation		800	mW
ESD	ESD Rating (R = 1500, C = 120 pF)		1.5	kV
I_{CD}	Clamp Diode Current	−20	20	mA

DC CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
V_{OL}	Low Output Voltage (I_{OL} = 2.0 mA) (Notes 1, 4)		0.4	Volts
	Low Output Voltage (I_{OL} = 20 µA) (Notes 1, 4)		0.1	Volts
V_{OH}	High Output Voltage (I_{OH} = 2.0 mA) (Notes 1, 4)	3.5		Volts
	High Output Voltage (I_{OH} = 20 µA) (Notes 1, 4)	V_{DD} − 0.1		Volts
V_{IL}	Low Input Voltage (Note 2)		0.8	Volts
	Low Input Voltage for −RACK, −WACK (Note 2)		0.6	Volts
V_{IH}	High Input Voltage (Note 2)	2.0		Volts
	High Input Voltage for −RACK, −WACK (Note 2)	2.7		Volts
V_{LO}	Link Output Voltage (I_{OL} = 16 mA)		0.4	Volts
I_{IL}	Input Leakage Current (V_{IN} = V_{DD} or V_{SS})		±1.0	µA
I_{OZ}	Tristate Output Leakage (V_{OUT} = V_{DD} or V_{SS})		±10	µA
I_{DD}	Power Supply Current (V_{IN} = V_{DD} or V_{SS}) (TXC, RXC, BSCK = 10 MHz) (I_{OUT} = 0 µA) (Note 3)		80	mA
OSCILLATOR CHARACTERISTICS				
V_{IH}	X1 High Input Voltage[5]	2		V
V_{IL}	X1 Low Input Voltage[5]		0.8	V
I_{OSC}	X1 Input Current[6]		3	mA

[1] These levels are tested dynamically using a limited number of functional test patterns. Refer to the *AC Test Conditions* section.

[2] Limited functional test patterns are performed at these input levels. For most functional tests, V_{IH} is performed at 0 V and 3 V. For −RACK and −WACK, V_{IH} is performed at 0 V and 3.2 V.

[3] This is measured with a 0.1µF bypass capacitor between V_{DD} and V_{SS}.

[4] The low-drive, CMOS-compatible V_{OH} and V_{OL} limits are not tested directly. Detailed device characterization guarantees this specification by testing the high-drive, TTL-compatible V_{OH} and V_{OL} specification.

[5] X1 is tied to an oscillator and X2 is tied to V_{SS}.

[6] X2 is tied to V_{SS} and V_{IN} is equal to V_{DD} or V_{SS}.

AUI/TPI DC CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
AUI CHARACTERISTICS				
V_{OD}	Differential Output Voltage (TX)[2]	±550	±1200	mV
V_{OB}	Differenial Output Voltage Imbalance (TX)[2]	Typically 40 mV		
V_U	Undershoot Voltage[1, 2]	Typically 80 mV		
V_{DS}	Differential Squelch Threshold (RX, CD)[1]	−175	−300	mV
V_{CM}	Diff. Input Common Mode Voltage (RX, CD)[1]	0	5.25	Volts
TPI CHARACTERISTICS				
R_{TOL}	TXOD, TXO Low Level Output Resistance[3]		15	Ohms
R_{TOH}	TXOD, TXO High Level Output Resistance[3]		15	Ohms
V_{SRON}	Receive Threshold Turn-On Voltage	±300	±585	mV
V_{SROFF}	Receive Threshold Turn-Off Voltage[1]	±175	V_{SRON}−100	Volts
V_{DIF}	Differential Mode Input Voltage[1, 4]	−3.1	3.1	Volts

[1] This value is guaranteed by design and is not tested.

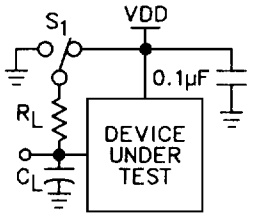
[2] Terminated with 78 and 270 ohm resistance from each to V_{SS}.

[3] I_{OL} = 25mA

[4] V_{DD} = 5V

AC TEST CONDITIONS

Condition	Test Value
Input Pulse Levels	VSS to 3.0 V
Input Rise/Fall Time	5 ns
Input/Output Reference	1.3 V
Input Diff. Pulse Levels	−350 to −1310 mV
Tristate Reference Level	Float (ΔV) ±0.5 V



C_L = 50 pF including scope and jig capacitance.
S1 = Open for timing tests for push-pull outputs.
S1 = V_{DD} for V_{OL} test. S1 = V_{SS} for V_{OH} test.
S1 = V_{DD} for measurements from high impedance to active low, and active low to high impedance.
S1 = V_{SS} for measurements from high impedance to active high, and active high to high impedance.

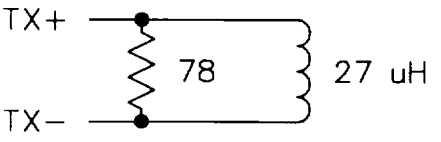
CAPACITANCE

Parameter	Description	Typ	Max	Unit
C_{IN}	Input Cap.	7	15	pF
C_{OUT}	Output Cap.	7	15	pF

Output timing is measured with a purely capacitive load of 50 pF. For loads ≥ 50 pF, add 0.3 ns/pF.

AUI Transmit Loading

The TX+ and TX− signals are tested on the AUI side of the isolation transformer.



AC CHARACTERISTICS

Latched Register Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	Bus clock high duration	6	22.5		ns
2	Bus clock low duration	6	22.5		ns
3	Bus clock cycle time	6	50	1000	ns
4	RA(3:0) setup to ADS0 low	6	10		ns
5	RA(3:0) hold from ADS0 low	6	13		ns
6	ADS0 pulse width	6	15		ns
7	-ACK to AD(7:0) valid	6		55	ns
8	-SRD high to data tristate	6	15	70	ns
9	-SRD low to -ACK low (Notes 1, 2, 3)	6		n*BSCK + 30	ns [4]
10	-SRD high to -ACK high	6		30	ns
11	RA(3:0) to -SRD low (Note 2)	6	10		ns

[1] -ACK is not generated until -CS and -SRD are low and the NCR92C902 has synchronized to the register access. The NCR92C902 inserts bus clock cycles until it has synchronized to the register access. In dual bus systems, additional cycles are added to complete a local or remote Direct Memory Access (DMA). Wait states must be issued to the CPU until -ACK is asserted low.

[2] -CS can be asserted before or after -SRD. If -CS is asserted after -SRD, parameter #9 is referenced from the falling edge of -CS.

[3] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[4] This unit is based on the bus clock cycle.

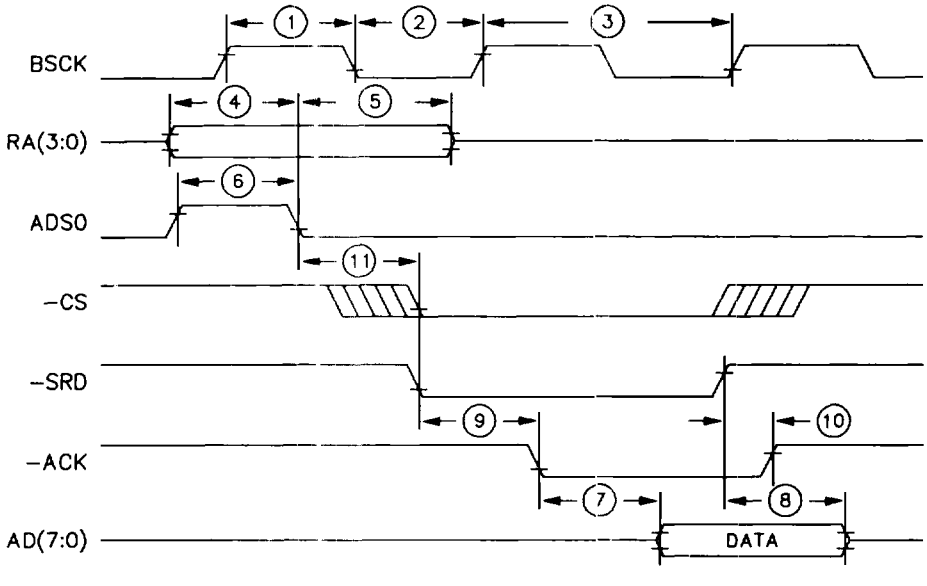


Figure 6 Latched Register Read (ADS0=0)

Unlatched Register Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	RA(3:0) setup time to -SRD (Notes 1, 2)	7	10		ns
2	RA(3:0) hold from -SRD	7	0		ns
3	-ACK low to valid data	7		55	ns
4	-SRD high to data tristate (Note 3)	7	15	70	ns
5	-SRD low to -ACK low (Note 2)	7		n*BSCK + 30	ns [4]
6	-SRD high to -ACK high	7		30	ns

[1] This specification includes flow-through time of the latch.

[2] Since address decode begins when -ACK is asserted, -CS can be asserted before or after -SRD and RA(3:0). If -CS is asserted after -SRD and RA(3:0), parameter #12 is referenced from the falling edge of -CS.

[3] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[4] This unit is based on the bus clock cycle.

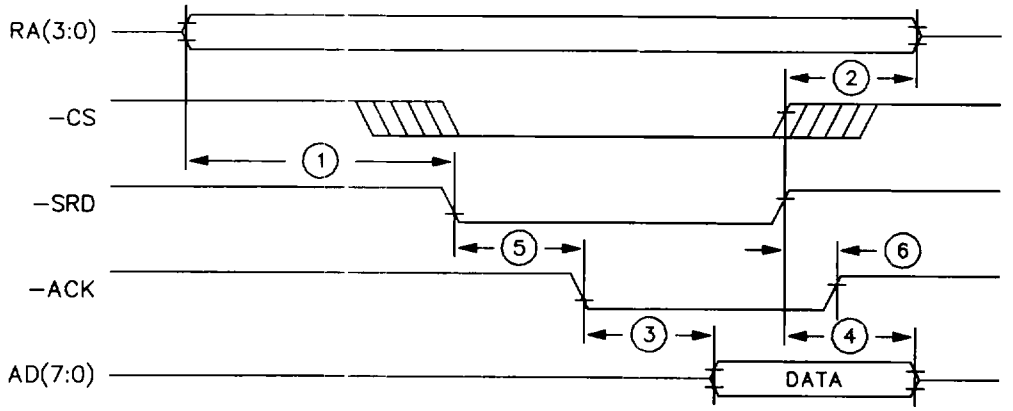


Figure 7 Unlatched Register Read (ADS0=1)

Latched Register Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	RA(3:0) setup to ADS0 low	8	10		ns
2	RA(3:0) hold from ADS0 low	8	17		ns
3	ADS0 pulse width	8	15		ns
4	AD(7:0) setup time to -SWR	8	20		ns
5	AD(7:0) hold time from -SWR	8	21		ns
6	-SWR width from -ACK low	8	50		ns
7	-SWR high to -ACK high	8		30	ns
8	-SWR low to -ACK low (Notes 1, 2)	8		n*BSCK + 30	ns [3]
9	RA(3:0) to -SWR low	8	10		ns

[1] -ACK is not generated until -CS and -SWR are low and the NCR92C902 has synchronized to the register access. In dual bus systems, additional cycles are added to complete a local or remote Direct Memory Access (DMA).

[2] -CS can be asserted before or after -SWR. If -CS is asserted after -SWR, parameter #24 is referenced from the falling edge of -CS.

[3] This unit is based on the bus clock cycle.

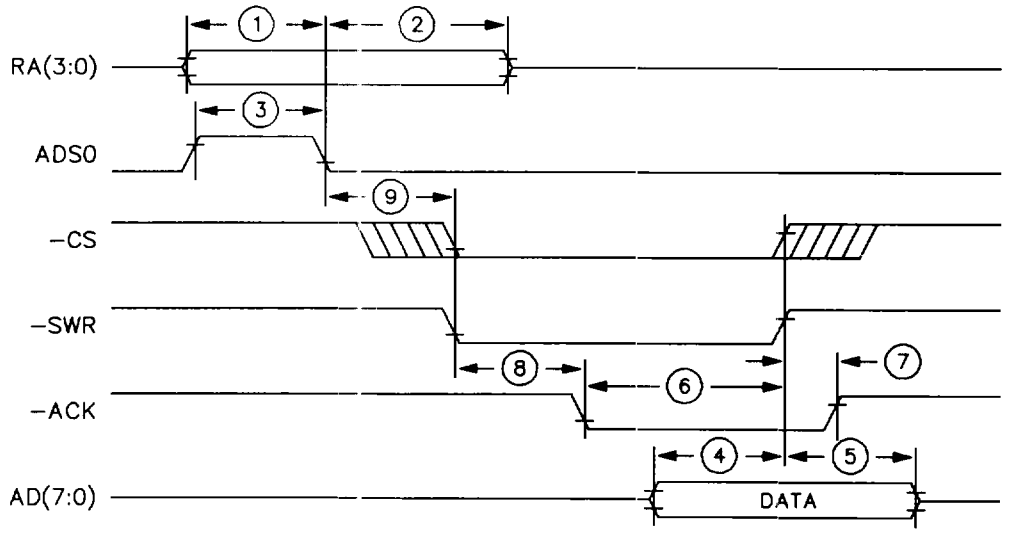


Figure 8 Latched Register Write (ADS0=0)

Unlatched Register Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	RA(3:0) setup time to -SWR (Note 1)	9	15		ns
2	RA(3:0) hold time from -SWR	9	0		ns
3	AD(7:0) setup time to -SWR	9	20		ns
4	AD(7:0) hold time from -SWR	9	21		ns
5	-SWR low to -ACK low (Note 2)	9		n*BSCK + 30	ns [3]
6	-SWR high to -ACK high	9		30	ns
7	-ACK low to -SWR high	9	50		ns

[1] This assumes that ADS0 is high when RA(3:0) is changing.

[2] -ACK is not generated until -CS and -SWR are low and the NCR92C902 has synchronized to the register access. In dual bus systems, additional cycles are added to complete a local or remote Direct Memory Access (DMA).

[3] This unit is based on the bus clock cycle.

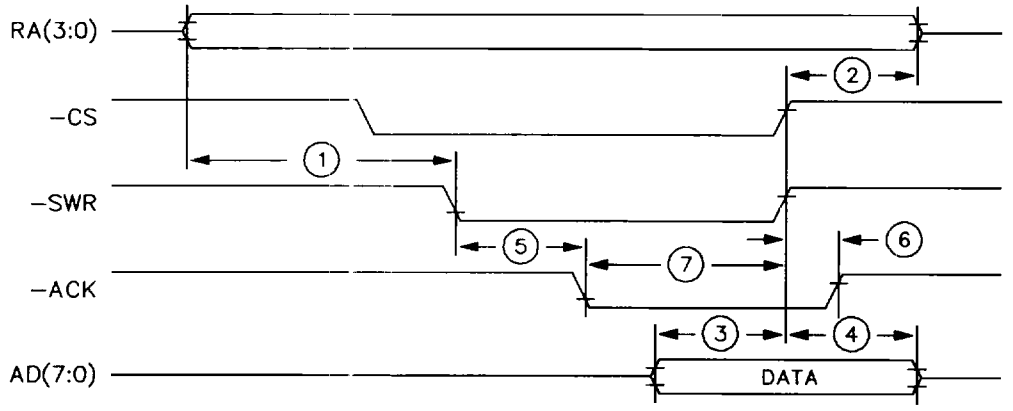


Figure 9 Unlatched Register Write (ADS0=1)

DMA Control Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK to BREQ high for local DMA	10		43	ns
2	BSCK to BREQ high for remote DMA	10		38	ns
3	BSCK to BREQ low	10		55	ns
4	BACK setup to BSCK (Note 1)	10	5		ns
5	BSCK to control enable	10		60	ns
6	BSCK to control release (Notes 2, 3)	10		70	ns

[1] BACK must be setup before T1 after BREQ is asserted. Missing the setup will slip the beginning of the DMA by four bus clocks. This bus latency will influence the allowable FIFO threshold and transfer mode (empty/fill vs. exact burst transfer).

[2] During remote DMA transfers only, a single bus transfer is performed. During local DMA operations, burst transfers are performed.

[3] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

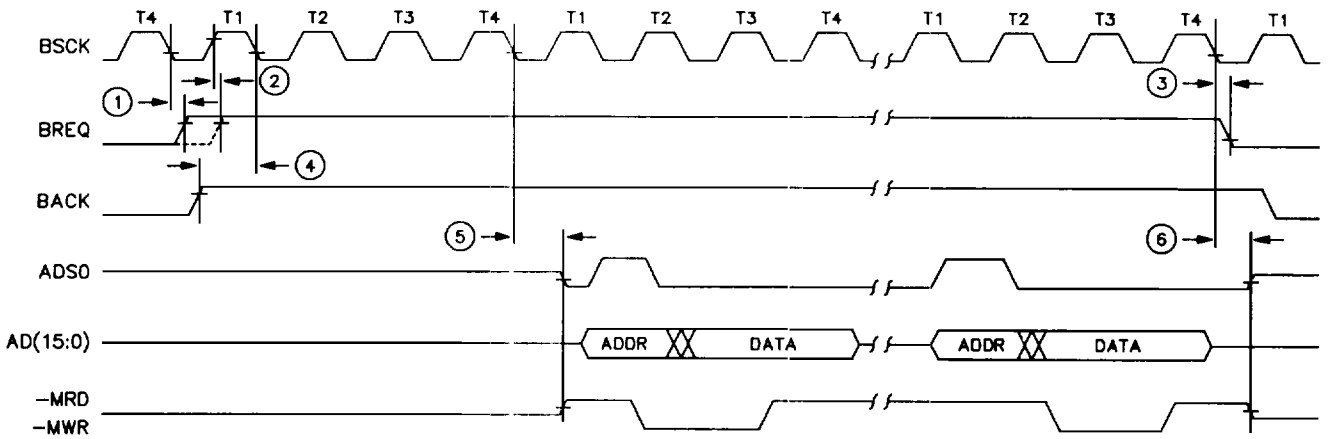


Figure 10 DMA Control – Bus Arbitration

DMA Address Generation (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK period (Note 1)	11	50	1000	ns
2	BSCK high duration	11	22.5		ns
3	BSCK low duration	11	22.5		ns
4	BSCK high to ADS1 high	11		34	ns
5	BSCK low to ADS1 low	11		44	ns
6	ADS1 duration	11	BSCK high duration		ns [3]
7	BSCK high to valid address	11		45	ns
8	BSCK high to address tristate (Note 2)	11	15	55	ns
9	AD(15:0) setup time to ADS0 or ADS1 low	11	BSCK high duration − 15		ns [3]
10	AD(15:0) hold time from ADS0 or ADS1 low	11	BSCK low duration − 5		ns [3]

[1] The rate of the bus clock must be high enough to support transfers to/from the FIFO at a rate greater than the serial network transfers from/to the FIFO.

[2] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[3] This unit is based on the high/low duration of the bus clock cycle.

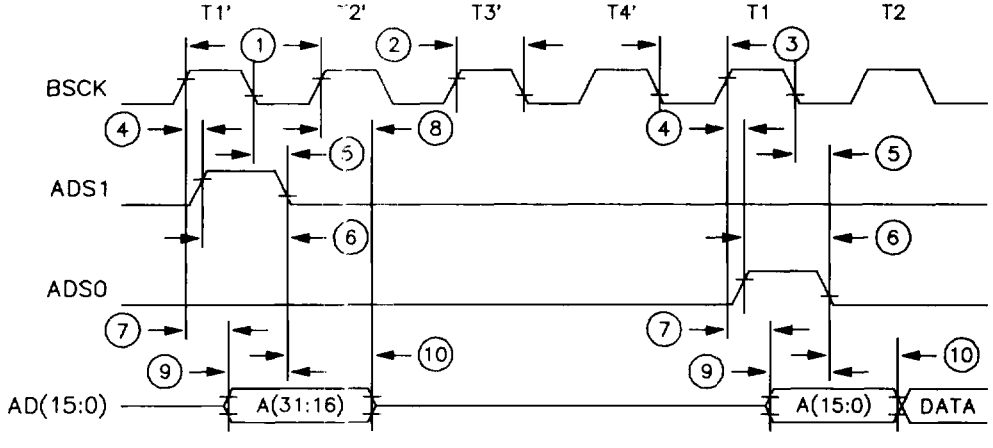


Figure 11 DMA Address Generation

Cycles T1′, T2′, T3′, and T4′ are issued only for the first transfer in a burst when 32-bit mode has been selected.

DMA Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK high to -MRD low	12		43	ns
2	BSCK high to -MRD high	12		40	ns
3	Data setup time to -MRD high	12	25		ns
4	Data hold time from -MRD high	12	0		ns
5	-MRD duration	12	2*BSCK - 15		ns [3]
6	-MRD high to address tristate (Notes 1, 2)	12		BSCK high duration + 40	ns [4]
7	ADS0 low to -MRD low	12		BSCK low duration + 10	ns [4]
8	-MRD high to address active	12	BSCK - 10		ns [3]
9	Address valid to -MRD high	12	3*BSCK - 15		ns [3]

[1] During a burst, A(15:8) are not tristate if byte wide transfers are selected. On the last transfer, A(15:8) are tristate as shown below.

[2] These limits include the RC delay inherent in our test method. These signals typically turn off within the BSCK high duration + 15 ns, enabling other devices to drive these signals without contention.

[3] This unit is based on the bus clock cycle.

[4] This unit is based on the high/low duration of the bus clock cycle.

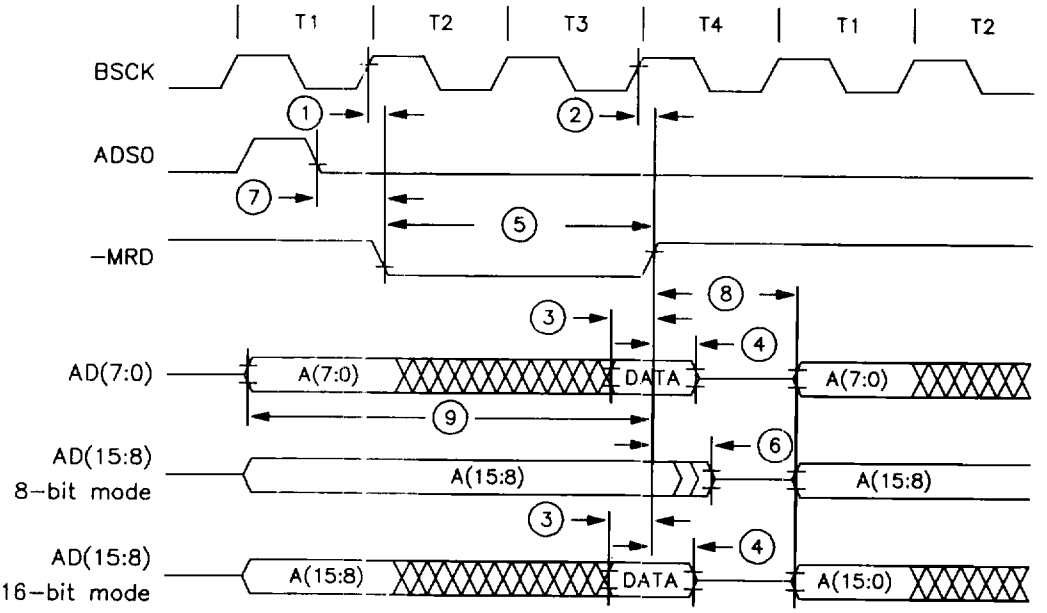


Figure 12 DMA Memory Read

DMA Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK high to -MWR low	13		40	ns
2	BSCK high to -MWR high	13		40	ns
3	Data setup time to -MWR high	13	2*BSCK - 30		ns [3]
4	Data hold time from -MWR high	13	BSCK high duration + 7		ns [4]
5	-MRW high to address tristate (Notes 1, 2)	13		BSCK high duration + 40	ns [4]
6	ADS0 low to -MWR low	13		BSCK low duration + 10	ns [4]
7	ADS0 low to valid data	13		BSCK low duration + 30	ns [4]

[1] When using byte mode transfers, A(15:8) are only tristate on the last transfer; this timing is valid only for the last transfer in a burst.

[2] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[3] This unit is based on the bus clock cycle time.

[4] This unit is based on the high/low duration of the bus clock cycle.

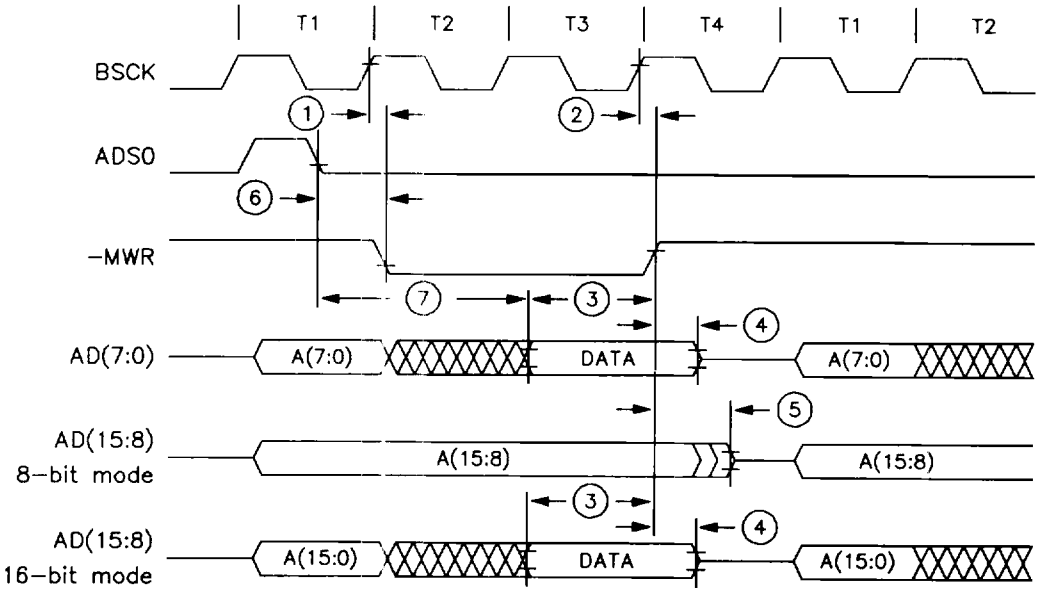


Figure 13 DMA Memory Write

Wait State Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	-READY setup to T3 BSCK low	14	10		ns
2	-READY low to BSCK low (release time) [1]	14	15		ns

[1] The addition of wait states affects the count of deserialized bytes and is limited to a number of bus clock cycles depending on the bus clock and network rates. The allowable wait states are shown in the table below.

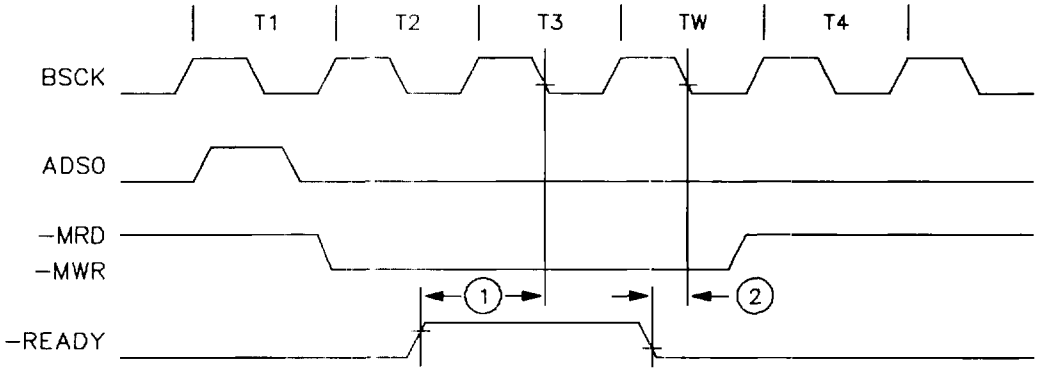


Figure 14 Wait State Insertion

TABLE 1

BSCK (MHz)	Number of Wait States	
	Byte Transfer	Word Transfer
8	0	1
10	0	1
12	1	2
14	1	2
16	1	3
18	2	3
20	2	4

Table 1 assumes a 10 MHz network clock. The number of allowable wait states in byte mode can be calculated using:

$$\#W_{(byte\ mode)} = \left[\frac{8\ tnw}{4.5\ BSCK} - 1 \right]$$

#W = the number of wait states
tnw = the network clock period
BSCK = BSCK period

The number of allowable wait states in word mode can be calculated using:

$$\#W_{(word\ mode)} = \left[\frac{5\ tnw}{2\ BSCK} - 1 \right]$$

Remote DMA Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK to -PWR low	15		43	ns
2	BSCK to -PWR high	15		40	ns
3	-PWR high to PRQ high [1]	15		30	ns
4	PRQ low from -RACK high	15		45	ns
5	-RACK read strobe pulse width	15	20		ns

[1] Start of next transfer is dependent on where -RACK is generated relative to BSCK and whether local DMA is pending.

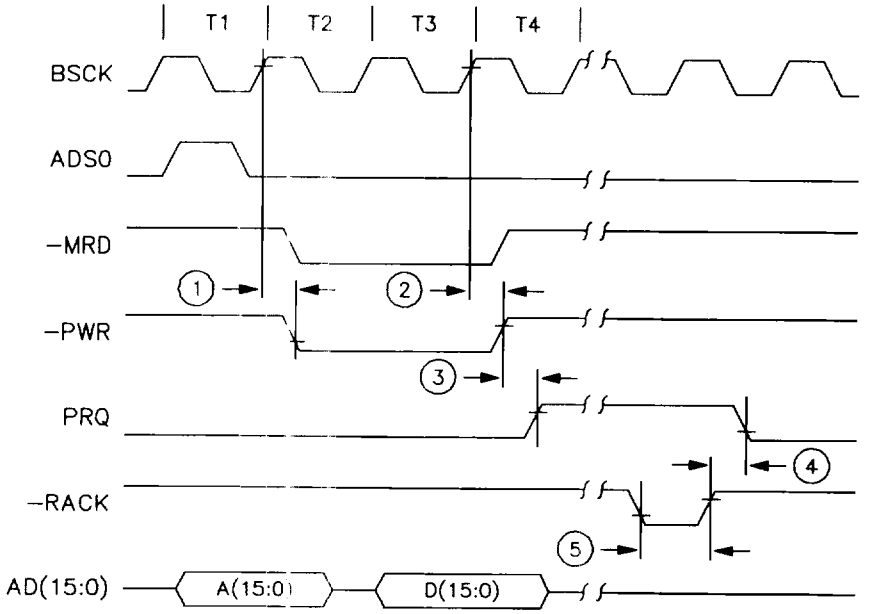


Figure 15 Remote DMA Read

Remote DMA Read Recovery Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK to -PWR low	16		43	ns
2	BSCK to -PWR high	16		40	ns
3	-PWR high to PRQ high (Note 1)	16		30	ns
4	PRQ low from -RACK high	16		45	ns
5	-RACK read strobe pulse width	16	20		ns
6	-RACK high to next port write cycle (Notes 2, 3, 4)	16	11		BSCK[5]

[1] Start of next transfer is dependent on where -RACK is generated relative to BSCK and whether local DMA is pending.

[2] This is not a measured value but it is guaranteed by design.

[3] -RACK must be high for a minimum of seven BSCK cycles.

[4] Assumes no local DMA interleave, no -CS input, and immediate BACK.

[5] This unit is the bus clock period.

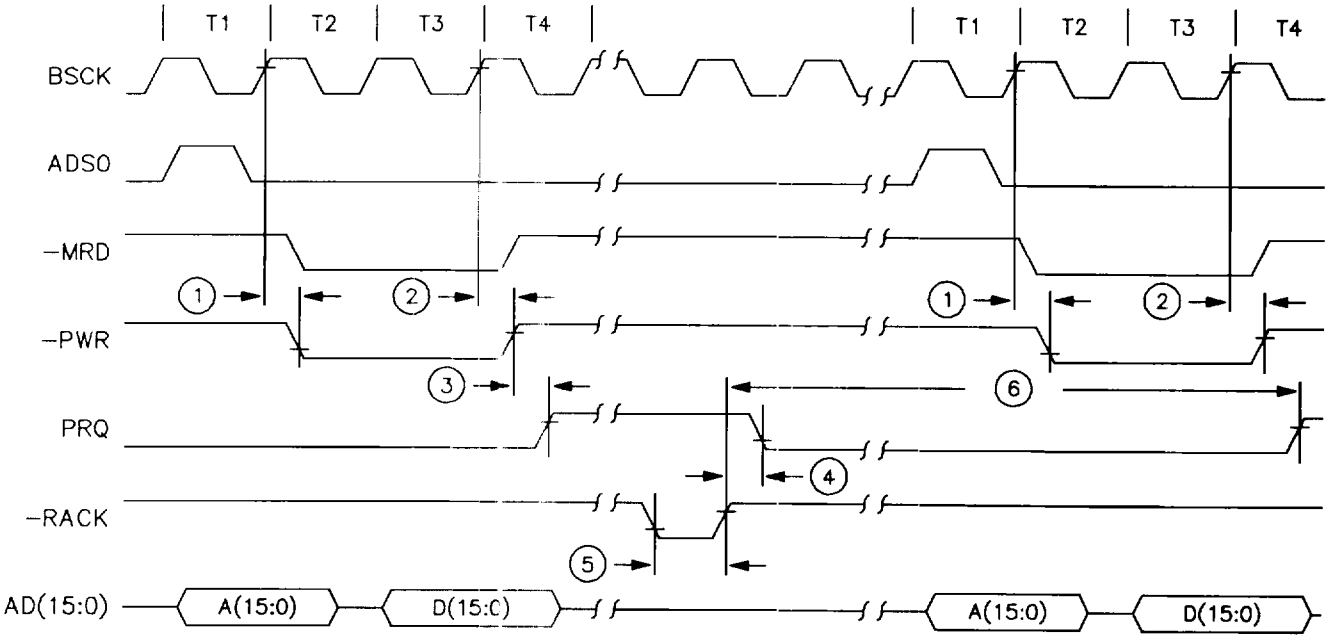


Figure 16 Remote DMA Read Recovery

Remote DMA Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK to PRQ high (Note 1)	17		42	ns
2	-WACK to PRQ low	17		45	ns
3	-WACK pulse width	17	20		ns
4	BSCK to -PRD low (Note 2)	17		40	ns
5	BSCK to -PRD high	17		40	ns

[1] The first port request is issued in response to the remote write command. It is subsequently issued on T1 clock cycles following completion of remote DMA cycles.

[2] The start of the remote DMA write following -WACK is dependent on where -WACK is issued relative to BSCK and whether a local DMA is pending.

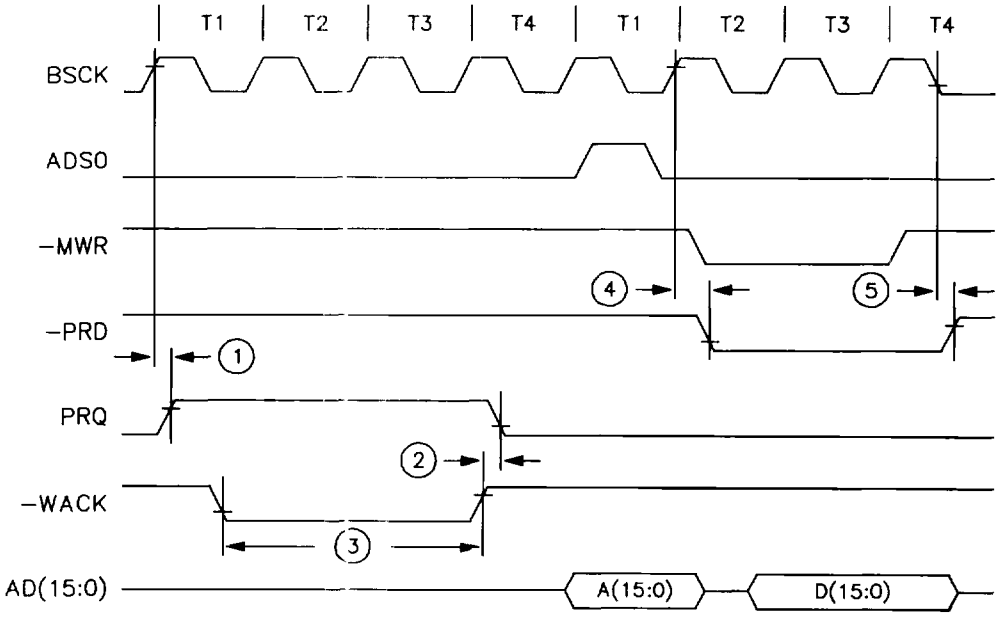


Figure 17 Remote DMA Write

Remote DMA Write Recovery Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	BSCK to PRQ high (Note 1)	18		40	ns
2	-WACK to PRQ low	18		45	ns
3	-WACK pulse width	18	20		ns
4	BSCK to -PRD low (Note 2)	18		40	ns
5	BSCK to -PRD high	18		40	ns
6	Remote write PRQ to PRQ high (Notes 3, 4, 5)	18	12		BSCK[6]

[1] The first port request is issued in response to the remote write command. It is subsequently issued on T1 clock cycles following completion of remote DMA cycles.

[2] The start of the remote DMA write following -WACK is dependent on where -WACK is issued relative to BSCK and whether a local DMA is pending.

[3] This assumes that parameter #76 is less than one BSCK, that there is no local DMA interleave, no -CS input, immediate -BACK, and -WACK goes high before T4.

[4] -WACK must be high for a minimum of seven BSCK cycles.

[5] This is not a measured value but it is guaranteed by design.

[6] This unit is the bus clock period.

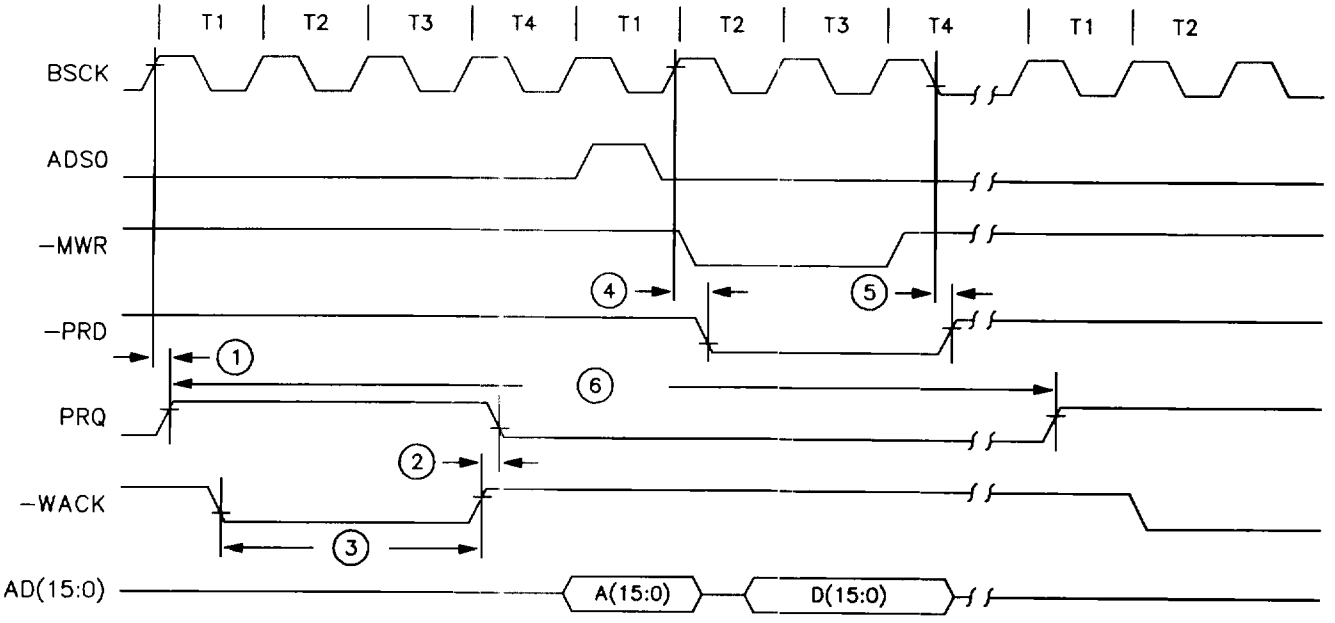


Figure 18 Remote DMA Write Recovery

Reset Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	Reset pulse width[1]	19	8		BSCK or TXC cycles[2]

[1] The RESET pulse requires that BSCK and TXC be stable. At power up, -RESET should not be raised until BSCK and TXC have become stable. Several registers are affected by -RESET.

[2] The slower clock, either BSCK or TSC, will determine the minimum time for the -RESET signal to be low.
If BSCK is less than TXC, then -RESET is eight BSCK cycles. If TSC is less than BSCK, then -RESET is eight TXC cycles.

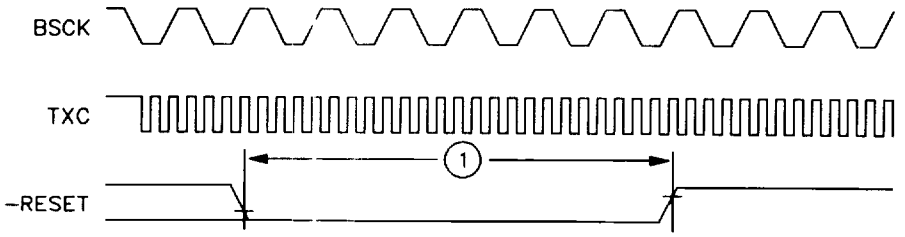


Figure 19 Reset Timing

AUI Transmit Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	TX+/− rise or fall time	20		8	ns
2	TX+/− high before idle (half step)	20	200		ns
3	TX+/− idle time (half step)	20		8	µs

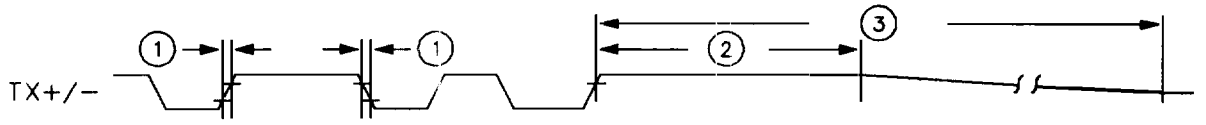


Figure 20 Transmit

TPI Receive Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	End of packet hold time[1]	21	200		ns

[1] This parameter is not measured, but guaranteed by design.

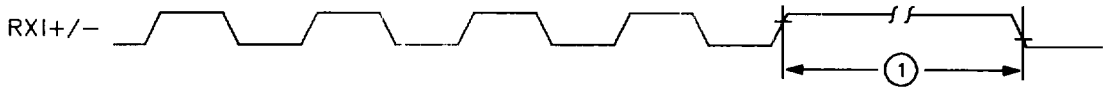


Figure 21 Receive

Link Test Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
1	Link pulse width	22		100		ns
2	Duration between transmitted link pulses	22	8	13	24	ms
3	Duration between received link pulses	22	3		105	ms

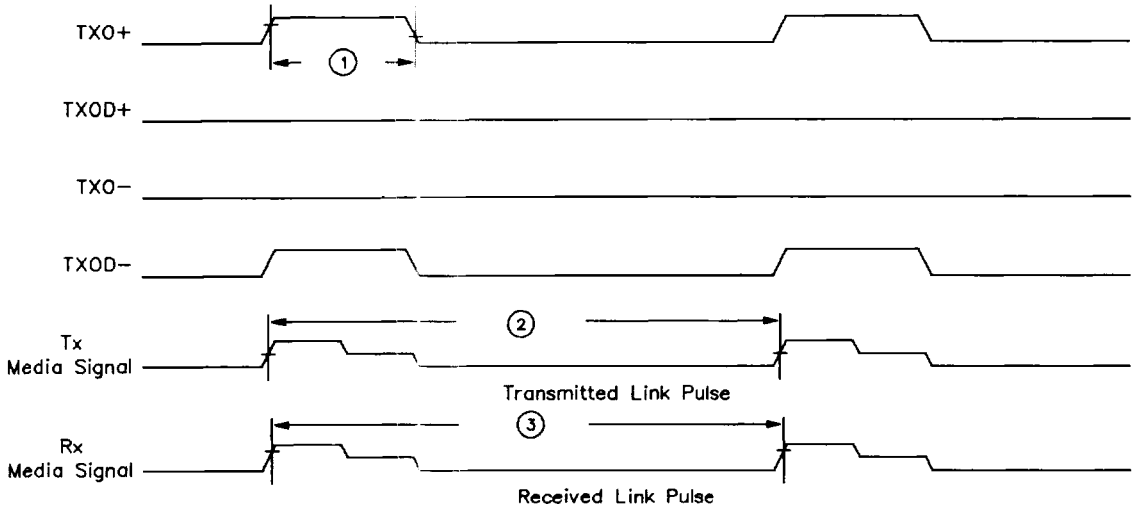


Figure 22 Link Test

Twisted Pair Transmit Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Min.	Typ.	Max.	Units
1	TXO+/− to TXOD+/− delay[1]	23	46		54	ns
2	TXO+/− hold time at end of packet[1]	23	250		400	ns
3	TXOD+/− hold time at end of packet[1]	23	200		350	ns

[1] This parameter is not measured, but guaranteed by design.

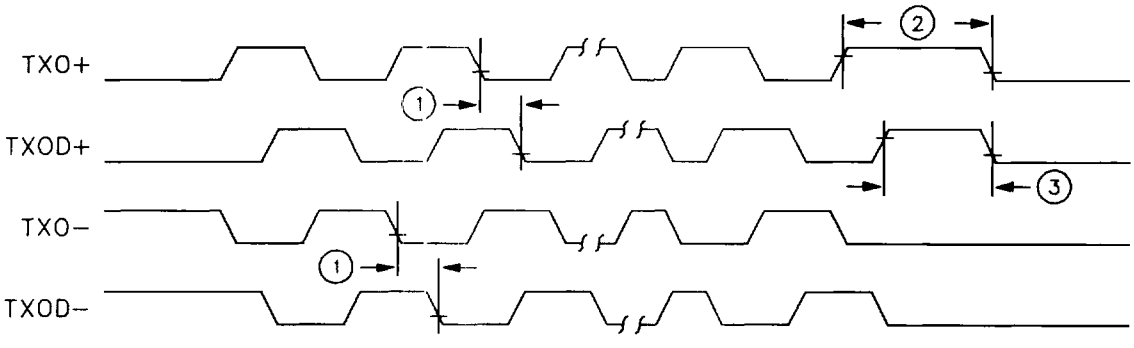


Figure 23 Twisted Pair Transmit

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