

256MB DDR – SDRAM SoDIMM

200PIN SoDIMM

SDN03264C1CF1MT-xxR

256MByte in FBGA Technology

RoHS compliant

Options:

- | | | |
|------------------------------------|---------------|---------|
| ▪ Data Rate / Latency | | Marking |
| DDR 400 MT/s CL3 | | -50 |
| DDR 333 MT/s CL2.5 | | -60 |
| ▪ Module density | | |
| 256MB with 4 dies and 1 rank | | |
| ▪ Standard Grade (T _A) | 0°C to 70°C | |
| Grade E (T _A) | 0°C to 85°C | |
| Grade I (T _A) | -25°C to 85°C | |
| Grade W (T _A) | -40°C to 85°C | |

*) The refresh rate has to be doubled when 85°C < T_C < 95°C

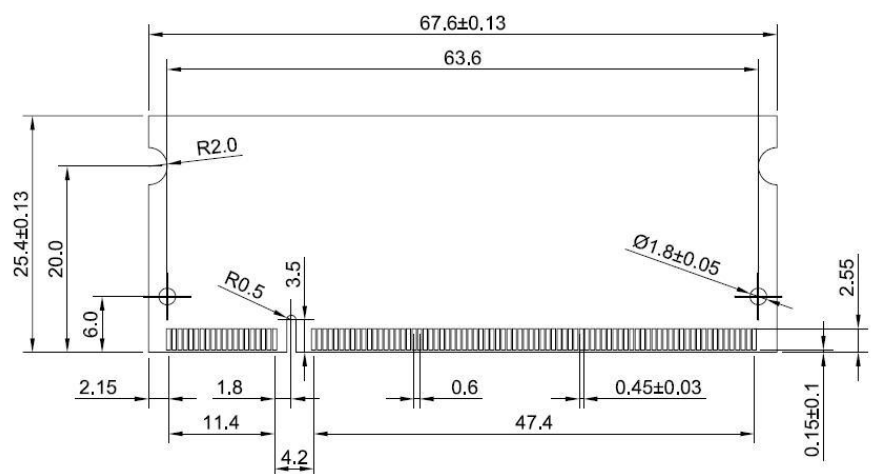
Environmental Requirements:

- Operating temperature (T_A)
 - Standard Grade 0°C to 70°C
 - E-Grade 0°C to 85°C
 - I-Grade -25°C to 85°C
 - W-Grade -40°C to 85°C
- Operating Humidity
10% to 90% relative humidity, noncondensing
- Operating Pressure
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
-55°C to 100°C
- Storage Humidity
5% to 95% relative humidity, noncondensir
- Storage Pressure
1682 PSI (up to 5000 ft.) at 50°C

Features:

- 200-pin 64-bit Small Outline Dual-In-Line module.
Double Date Rate synchronous DRAM Module for industrial applications
- DDR-SDRAM component base: Micron MT46V32M16BN-6:F BGA
- V_{DD} 2.5V ±0.2V, V_{DDQ} 2.5V ±0.2V
- Programmable CAS Latency, Burst Length and Wrap Sequence
- Auto Refresh (CBR) and Self Refresh
- 8k Refresh every 64ms
- 2.5V I/O (SSTL_2 compatible)
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC PC3200 spec. and JEDEC- Standard MO 224.
(see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

Figure: mechanical dimensions¹



This Swissbit module family is industry standard 200-pin 8-byte Double Data rate synchronous SDRAM Small Outline Dual-In-line Memory Modules (SoDIMMs), which are organized as x64 high speed memory arrays designed for use in non-parity applications. SoDIMMs are assembled in FBGA Technology. The passive devices and the EEPROM are SMD components.

The SoDIMM use serial presence detects (SPD) implemented via serial EEPROM using the two-pin-I²C protocol. The first 128 bytes are utilized by the SoDIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit SoDIMMs provide a high performance, flexible 8-byte interface in a 67.60mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

Module Configuration

Organization	DDR SDRAMs used	Row Addr.	Bank Addr.	Column Addr.	Refresh	Module Dimensions in mm
32M x 64	4 x 32M x 16	13	BA0, BA1	10	8k	67,60 x 25,4 max

Product Spectrum

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SDN03264C1CF1MT-50[E/I/W]R	256MB	3.2 GB/s	5.0ns / 400MT/s	3.0-3-3
SDN03264C1CF1MT-60[E/I/W]R	256MB	2.7 GB/s	6.0ns / 333MT/s	2.5-3-3

Pin Name

A0-9, A11 – A12	Address Inputs
A10/AP	Address Input/Auto precharge
BA0, BA1	Bank Selects
DQ0 – DQ63	Data Input/Output
DM0-DM7	Data Masks
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Read / Write Enable
CKE0	Clock Enable
CK0 – CK1	Clock Inputs, positive line
/CK0 – /CK1	Clock Inputs, negative line
DQS0- DQS7	Data strobes

/S0	Chip Select
V _{DD}	Power (2.5V± 0.2V)
V _{DDQ}	Power (2.5V±0.2V)
V _{DDID}	VDD, VDDQ level detection
V _{DDSPD}	SPD Power
V _{REF}	Input/Output Reference
V _{SS}	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
NC	No Connection

Pin Configuration

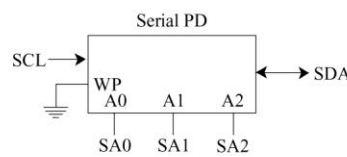
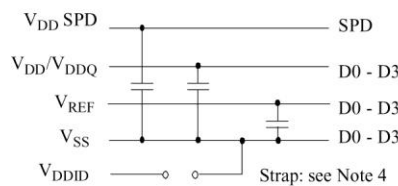
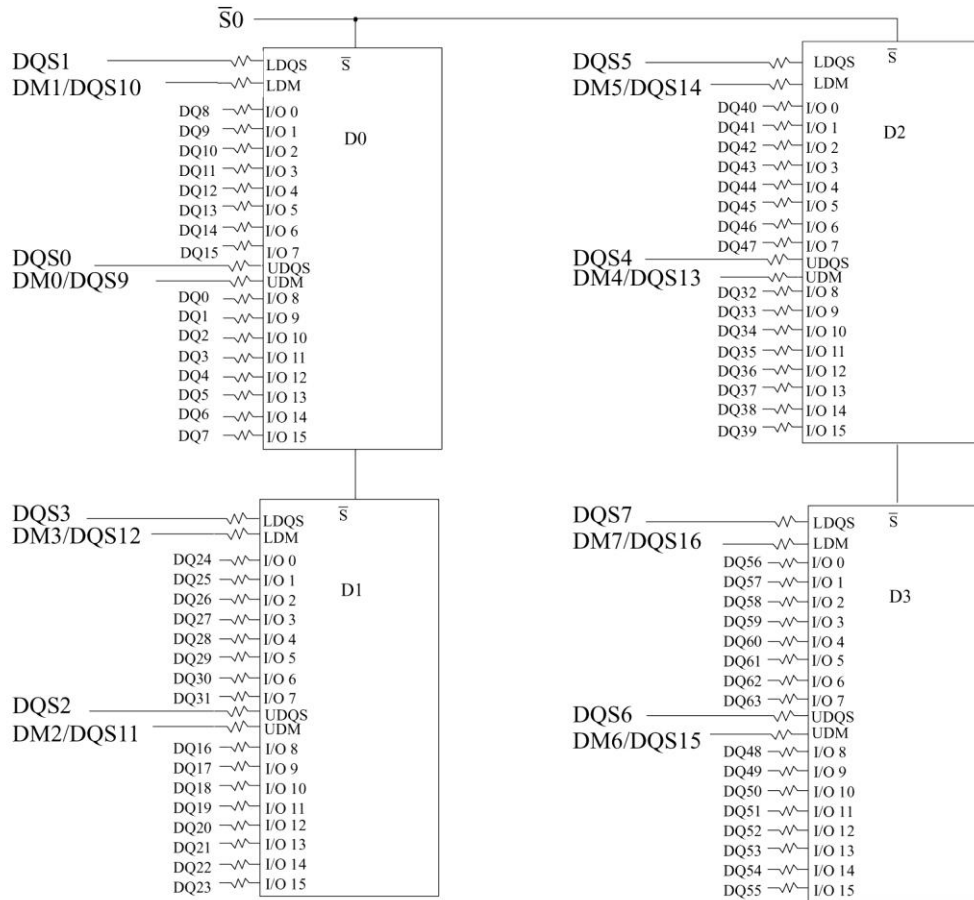
PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	V _{REF}	2	V _{REF}	101	A9	102	A8
3	V _{SS}	4	V _{SS}	103	V _{SS}	104	V _{SS}
5	DQ0	6	DQ4	105	A7	106	A6
7	DQ1	8	DQ5	107	A5	108	A4
9	V _{DD}	10	V _{DD}	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	DQ2	14	DQ6	113	V _{DD}	114	V _{DD}
15	V _{SS}	16	V _{SS}	115	A10/AP	116	BA1
17	DQ3	18	DQ7	117	BA0	118	/RAS
19	DQ8	20	DQ12	119	/WE	120	/CAS
21	V _{DD}	22	V _{DD}	121	/S0	122	NC (/S1)
23	DQ9	24	DQ13	123	NC (A13)	124	NC
25	DQS1	26	DM1	125	V _{SS}	126	V _{SS}
27	V _{SS}	28	V _{SS}	127	DQ32	128	DQ36
29	DQ10	30	DQ14	129	DQ33	130	DQ37
31	DQ11	32	DQ15	131	V _{DD}	132	V _{DD}
33	V _{DD}	34	V _{DD}	133	DQS4	134	DM4
35	CK0	36	V _{DD}	135	DQ34	136	DQ38
37	/CK0	38	V _{SS}	137	V _{SS}	138	V _{SS}
39	V _{SS}	40	V _{SS}	139	DQ35	140	DQ39
41	DQ16	42	DQ20	141	DQ40	142	DQ44
43	DQ17	44	DQ21	143	V _{DD}	144	V _{DD}
45	V _{DD}	46	V _{DD}	145	DQ41	146	DQ45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	DQ18	50	DQ22	149	V _{SS}	150	V _{SS}
51	V _{SS}	52	V _{SS}	151	DQ42	152	DQ46

Signals in brackets are not used on module, but may be connected on the socket

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
53	DQ19	54	DQ23	153	DQ43	154	DQ47
55	DQ24	56	DQ28	155	V _{DD}	156	V _{DD}
57	V _{DD}	58	V _{DD}	157	V _{DD}	158	/CK1
59	DQ25	60	DQ29	159	V _{SS}	160	CK1
61	DQS3	62	DM3	161	V _{SS}	162	V _{SS}
63	V _{SS}	64	V _{SS}	163	DQ48	164	DQ52
65	DQ26	66	DQ30	165	DQ49	166	DQ53
67	DQ27	68	DQ31	167	V _{DD}	168	V _{DD}
69	V _{DD}	70	V _{DD}	169	DQS6	170	DM6
71	NC (CB0)	72	CB4	171	DQ50	172	DQ54
73	NC (CB1)	74	CB5	173	V _{SS}	174	V _{SS}
75	V _{SS}	76	V _{SS}	175	DQ51	176	DQ55
77	DQS8	78	DM8	177	DQ56	178	DQ60
79	NC (CB2)	80	CB6	179	V _{DD}	180	V _{DD}
81	V _{DD}	82	V _{DD}	181	DQ57	182	DQ61
83	NC (CB3)	84	CB7	183	DQS7	184	DM7
85	NC	86	NC (/RESET)	185	V _{SS}	186	V _{SS}
87	V _{SS}	88	V _{SS}	187	DQ58	188	DQ62
89	CK2	90	V _{SS}	189	DQ59	190	DQ63
91	/CK2	92	V _{DD}	191	V _{DD}	192	V _{DD}
93	V _{DD}	94	V _{DD}	193	SDA	194	SA0
95	NC (CKE1)	96	CKE0	195	SCL	196	SA1
97	NC	98	NC (BA2)	197	V _{DDSPD}	198	SA2
99	A12	100	A11	199	V _{DDID}	200	NC

Signals in brackets are not used on module, but may be connected on the socket

FUNCTIONAL BLOCK DIAGRAM 256MB DDR SDRAM SoDIMM 1RANK; NON-ECC



* Clock Wiring	
Clock Input	SDRAMs
*CK0/ $\overline{\text{CK0}}$	NC
*CK1/ $\overline{\text{CK1}}$	2 SDRAMs
*CK2/ $\overline{\text{CK2}}$	2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

- BA0 - BA1 → BA0-BA1: SDRAMs D0 - D3
- A0 - A13 → A0-A13: SDRAMs D0 - D3
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMs D0 - D3
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMs D0 - D3
- CKE0 → CKE: SDRAMs D0 - D3
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: SDRAMs D0 - D3

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. VDDID strap connections (for memory device VDD, VDDQ): STRAP OUT (OPEN): VDD = VDDQ STRAP IN (VSS): VDD ≠ VDDQ
5. BAX, Ax, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ resistors: 7.5 ohms ± 5%

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

 (0°C ≤ T_A ≤ + 70°C; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{DD}	2.3	2.7	V
I/O Supply Voltage	V _{DDQ}	2.3	2.7	V
I/O Reference Voltage	V _{REF}	0.49 x V _{DDQ}	0.51x V _{DDQ}	V
I/O Termination Voltage (system)	V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V
Input High (Logic 1) Voltage	V _{IH(DC)}	V _{REF} + 0.15	V _{DD} + 0.3	V
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.3	V _{REF} - 0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{DD} , V _{REF} pin 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	I _I	-10	10	µA
OUTPUT LEAKAGE CURRENT (DQ _S are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ})	I _{OZ}	-10	10	µA
OUTPUT LEVELS: High Current (V _{OUT} = V _{DDQ} -0.373V, minimum V _{REF} , minimum V _{TT})	I _{OH}	-16.8	-	mA
Low Current (V _{OUT} = 0.373V, maximum V _{REF} , maximum V _{TT})	I _{OL}	16.8	-	mA

AC INPUT OPERATING CONDITIONS

 (0°C ≤ T_A ≤ + 70°C; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	V _{IH(AC)}	V _{REF} + 0.310	-	V
Input Low (Logic 0) Voltage	V _{IL(AC)}	-	V _{REF} - 0.310	V
I/O Reference Voltage	V _{REF(AC)}	0.49 x V _{DDQ}	0.51x V _{DDQ}	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C ₁₀	4.0	5.0	pF
Input Capacitance: Command and Address	C ₁₁	18.0	27.0	pF
Input Capacitance: /S 0,1	C ₁₁	18.0	27.0	pF
Input Capacitance: CK, /CK	C ₁₂	10.0	14.0	pF
Input Capacitance: CKE	C ₁₃	18.0	27.0	pF

I_{DD} Specifications AND CONDITIONS

 (0°C ≤ T_A ≤ + 70°C; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

Parameter & Test Condition	Symb.	max.			
		3200-3033	2700-2533	Unit	
OPERATING CURRENT *) : One device bank; Active-Precharge; t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	620	520	mA	
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; Burst = 2; t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	780	640	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (Min); CKE = (LOW)	I _{DD2P}	20	20	mA	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; t _{CK} = t _{CK} (Min); CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2F}	220	180	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t _{CK} = t _{CK} (Min); CKE = LOW	I _{DD3P}	180	140	mA	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; t _{RC} = t _{RAS} (Max); t _{CK} = t _{CK} (Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	240	200	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (Min); I _{OUT} = 0mA	I _{DD4R}	840	660	mA	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (Min); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	860	780	mA	
AUTO REFRESH CURRENT	t _{RC} = t _{RC} (Min)	I _{DD5}	1380	1160	mA
	t _{RC} = 7.8125μs	I _{DD5A}	44	40	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	I _{DD6}	24	20	mA	
OPERATING CURRENT*): Four device bank interleaving READs (BL = 4) with auto precharge, t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); Address and control inputs change only during Active READ, or WRITE commands	I _{DD7}	1920	1620	mA	

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

AC CHARACTERISTICS		3200-3033		2700-2533		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
Access window of DQ _S CK/CK#	t _{AC}	-0.50	+0.50	-0.70	+0.70	ns
CK high-level width	t _{CH}	0.45	0.55	0.45	0.55	t _{CK}
CK low-level width	t _{CL}	0.45	0.55	0.45	0.55	t _{CK}
Clock cycle time	CL=2.0	t _{ck} (2.0)	7.5	13.0	7.5	13.0
	CL=2.5	t _{ck} (2.5)	6.0	13.0	6.0	13.0
	CL=3.0	t _{ck} (3.0)	5.0	13.0		ns
DQ and DM input hold time relative to DQS	t _{DH}	0.40		0.45		ns
DQ and DM input setup time relative to DQS	t _{DS}	0.40		0.45		ns
DQ and DM input pulse width (for each input)	t _{DIPW}	1.75		1.75		ns
Access window of DQS from CK/CK#	t _{DQSCK}	-0.6	+0.6	-0.6	+0.6	ns
DQS input high pulse width	t _{DQSH}	0.35		0.35		t _{CK}
DQS input low pulse width	t _{DQSL}	0.35		0.35		t _{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}		0.40		0.45	ns
Write command to first DQS latching transition	t _{DQSS}	0.72	1.28	0.75	1.25	t _{CK}
DQS falling edge to CK rising- setup time	t _{DSS}	0.2		0.2		t _{CK}
DQS falling edge from CK rising- hold time	t _{DSH}	0.2		0.2		t _{CK}
Half clock period	t _{HP}	t _{ch} , t _{cl}		t _{ch} , t _{cl}		ns
Data-out high-impedance window from CK/CK#	t _{HZ}		+0.7		+0.7	ns
Data-out low-impedance window from CK/CK#	t _{LZ}	-0.7		-0.7		ns
Address and control input hold time (fast slew rate)	t _{IHF}	0.6		0.75		ns
Address and control input setup time (fast slew rate)	t _{ISF}	0.6		0.75		ns
Address and control input hold time (slow slew rate)	t _{IHS}	0.7		0.8		ns
Address and control input setup time (slow slew rate)	t _{ISS}	0.6		0.8		ns
LOAD MODE REGISTER command cycle time	t _{MRD}	10		12		ns
Adress and control input pulse width (for each input)	t _{IPW}	2.2		2.2		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ns
Data hold skew factor	t _{QHS}		0.5		0.6	ns

AC CHARACTERISTICS		3200-3033		2700-2533		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
ACTIVE to PRECHARGE command	t_{RAS}	40	70.000	42	70.000	ns
ACTIVE to READ with Auto precharge command	t_{RAP}	15		15		ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55		60		ns
AUTO REFRESH command period	t_{RFC}	70		72		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		18		ns
PRECHARGE command period	t_{RP}	15		18		ns
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	10		12		ns
DQS write preamble	t_{WPRE}	0.25		0.25		t_{CK}
DQS write preamble setup time	t_{WPRES}	0		0		ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time	t_{WR}	15		15		ns
Internal WRITE to READ command delay	t_{WTR}	2		1		t_{CK}
Data valid output window	na	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns
REFRESH to REFRESH command interval	t_{REFC}		70.3		70.3	μs
Average periodic refresh interval $0^{\circ}C \leq T_{CASE} \leq 85^{\circ}C$	t_{REFI}		7.8		7.8	μs
$85^{\circ}C < T_{CASE} \leq 95^{\circ}C$	$t_{REFI (IT)}$		3.9		3.9	μs
Terminating voltage delay to V_{DD}	t_{VTD}	0		0		ns
Exit SELF REFRESH to non-READ command	t_{XSNR}	70		75		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		t_{CK}

Note 1: Values for AC timing, IDD, and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

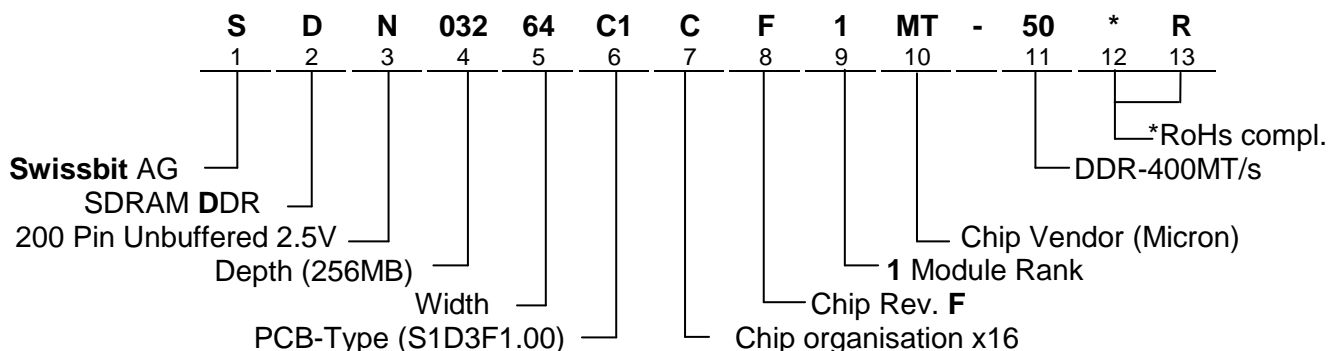
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	3200-3033	2700-2533
0	NUMBER OF SPD BYTES USED		0x80
1	TOTAL NUMBER OF BYTES IN SPD DEVICE		0x08
2	FUNDAMENTAL MEMORY TYPE		0x07
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY		0x0D
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY		0x0A
5	NUMBER OF PHYSICAL BANKS ON DIMM		0x01
6	MODULE DATA WIDTH		0x40
7	MODULE DATA WIDTH (continued)		0x00
8	MODULE VOLTAGE INTERFACE LEVELS (V_{DDQ})		0x04
9	SDRAM CYCLE TIME, (t_{CK}) (CAS LATENCY =2.5 (2700, 2100) ; CL=3* (3200))	0x50	0x60
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) (CAS LATENCY =2.5 (2700, 2100); CL=3* (3200))	0x70	0x70
11	MODULE CONFIGURATION TYPE		0x00
12	REFRESH RATE/ TYPE		0x82
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)		0x10
14	ERROR- CHECKING SDRAM DATA WIDTH		0x00
15	MINIMUM CLOCK DELAY, BACK- TO- BACK RANDOM COLUMN ACCESS		0x01
16	BURST LENGTHS SUPPORTED		0x0E
17	NUMBER OF BANKS ON SDRAM DEVICE		0x04
18	CAS LATENCIES SUPPORTED	0x1C	0x0C
19	CS LATENCY		0x01
20	WE LATENCY		0x02
21	SDRAM MODULE ATTRIBUTES		0x20
22	SDRAM DEVICE ATTRIBUTES: GENERAL		0xC1
23	SDRAM CYCLE TIME, (t_{CK}) (CAS LATENCY=2(2700, 2100) CL=2,5*(3200))	0x60	0x75
24	SDRAM ACCESS FROM CK, (t_{AC}) (CAS LATENCY=2(2700, 2100) CL=2.5*(3200))	0x70	0x70
25	SDRAM CYCLE TIME, (t_{CK}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x75	0x00
26	SDRAM ACCESS FROM CK, (t_{AC}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x75	0x00
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C	0x48
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x28	0x30
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C	0x48
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x28	0x2A
31	MODULE BANK DENSITY		0x40

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	3200-3033	2700-2533
32	ADDRESS AND COMMAND SETUP TIME, (t _{IS})	0x60	0x75
33	ADDRESS AND COOMAND HOLD TIME, (t _{IH})	0x60	0x75
34	DATA/DATA MASK INPUT SETUP TIME, (t _{DS})	0x40	0x45
35	DATA/DATA MASK INPUT HOLD TIME, (t _{DH})	0x40	0x45
36-40	RESERVED	0x00	
41	MIN ACTIVE AUTO REFRESH TIME (t _{RC})	0x37	0x3C
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (t _{RFC})	0x46	0x48
43	SDRAM DEVICE MAX CYCLE TIME (t _{CKMAX})	0x30	0x30
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME (t _{DQSQ})	0x28	0x2D
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR (t _{QHS})	0x50	0x55
46-61	RESERVED	0x00	
62	SPD REVISION	0x10	
63	CHECKSUM FOR BYTES 0-62	0x87	0x19
4	MANUFACTURER`S JEDEC ID CODE	7F	
65	MANUFACTURER`S JEDEC ID CODE	7F	
66	MANUFACTURER`S JEDEC ID CODE	7F	
67	MANUFACTURER`S JEDEC ID CODE (continued)	DA	
72	MANUFACTURING LOCATION	X	
73-90	MODULE PART NUMBER (ASCII)	"SDN03264C1CF1MT-xx"	
91	PCB IDENTIFICATION CODE	x	
92	IDENTIFICATION CODE (continued)	x	
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	x	x
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		

Part Number Code



* optional / additional information

Revision History		
Revision	Changes	Date
1.0	Initial Revision	30.05.2012

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