

## N-channel 800 V, 0.95 $\Omega$ typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFETs in TO-220FP and I<sup>2</sup>PAKFP packages

Datasheet - production data

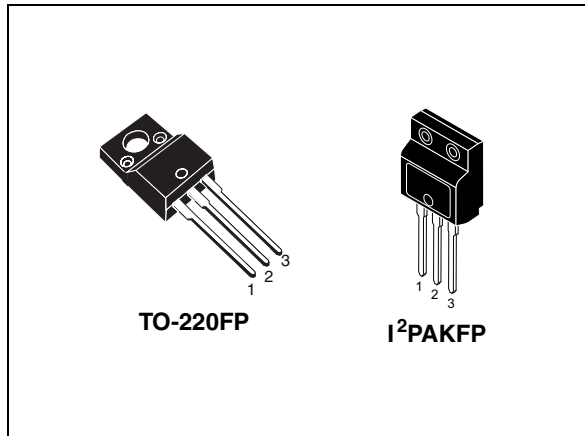
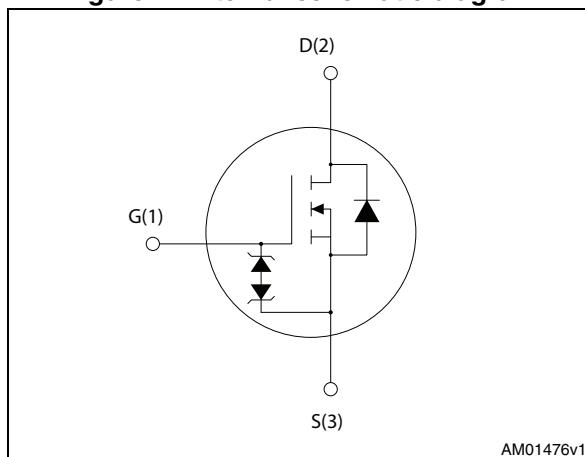


Figure 1. Internal schematic diagram



### Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STF7N80K5	800 V	1.2 $\Omega$	6 A	25 W
STFI7N80K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF7N80K5	7N80K5	TO-220FP	Tube
STFI7N80K5		I <sup>2</sup> PAKFP	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.8 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	24 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ )	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	88	mJ
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}$ ; $T_C=25\text{ }^\circ\text{C}$ )	2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_j$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

- Limited by package
- Pulse width limited by safe operating area.
- $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 800\text{ V}$ $V_{DS} = 800\text{ V}, T_c = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		0.95	1.2	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	360	-	pF
$C_{oss}$	Output capacitance		-	30	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }640\text{ V}$	-	47	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	20	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}, I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	13.4	-	nC
$Q_{gs}$	Gate-source charge		-	3.7	-	nC
$Q_{gd}$	Gate-drain charge		-	7.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	11.3	-	ns
$t_r$	Rise time			8.3		ns
$t_{d(off)}$	Turn-off delay time				23.7	ns
$t_f$	Fall time				20.2	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , (see <a href="#">Figure 16</a> )	-	315		ns
$Q_{rr}$	Reverse recovery charge		-	2.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	480		ns
$Q_{rr}$	Reverse recovery charge		-	3.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	16		A

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

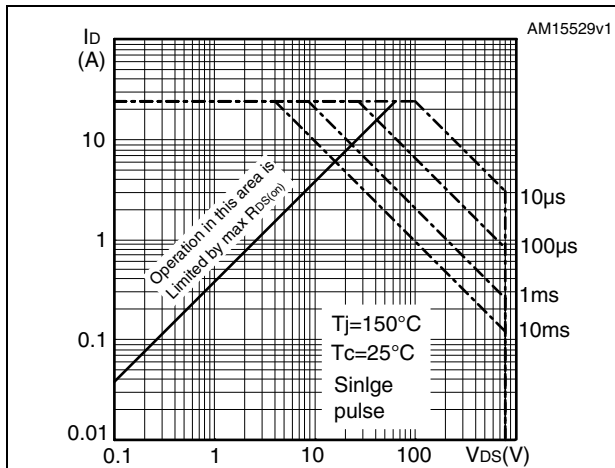


Figure 3. Thermal impedance

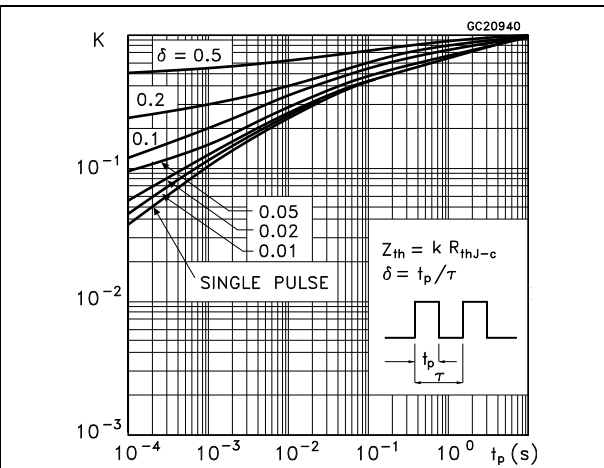


Figure 4. Output characteristics

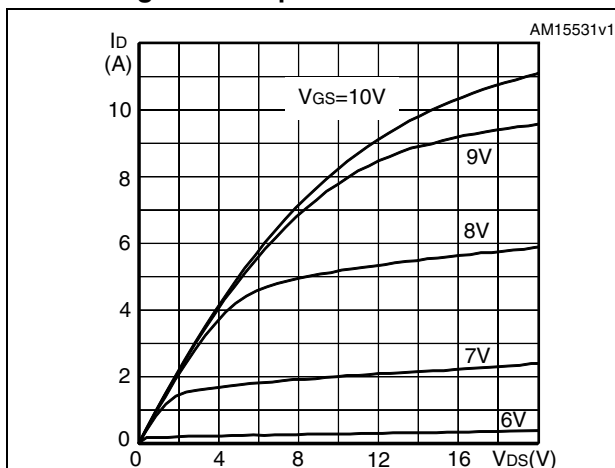


Figure 5. Transfer characteristics

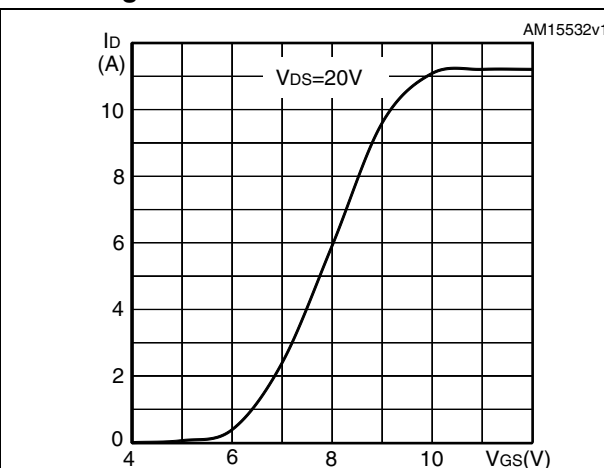


Figure 6. Gate charge vs gate-source voltage

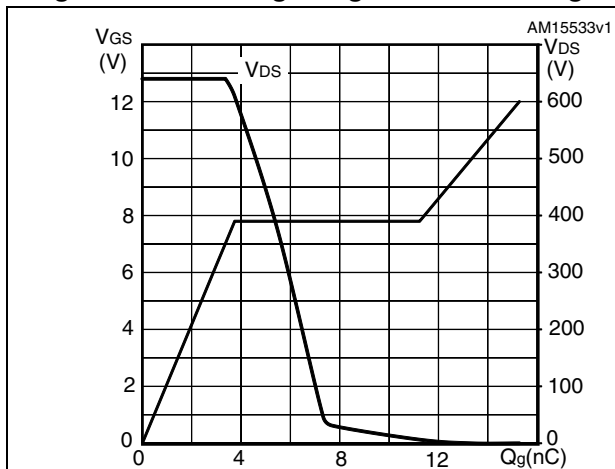


Figure 7. Static drain-source on-resistance

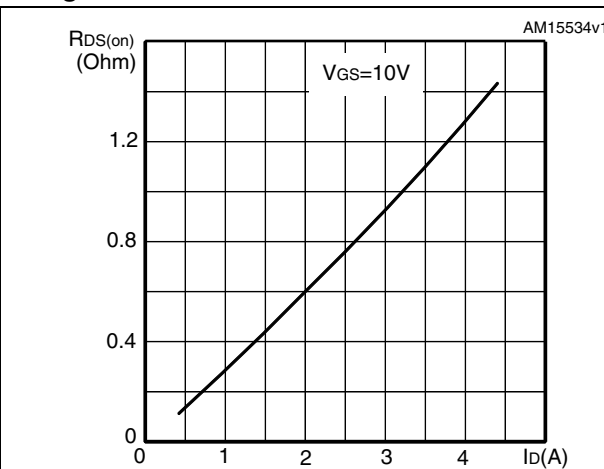


Figure 8. Capacitance variations

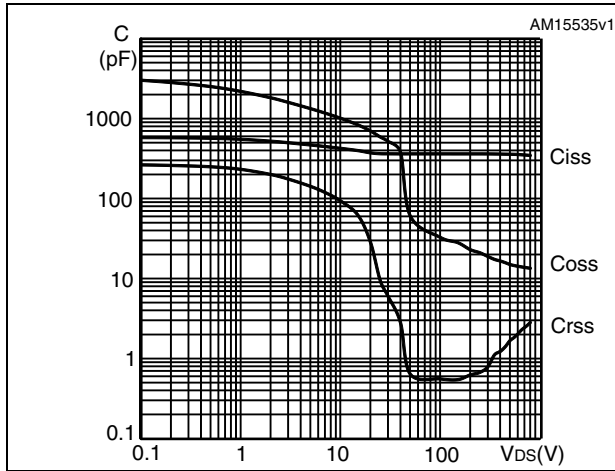


Figure 9. Source-drain diode forward characteristics

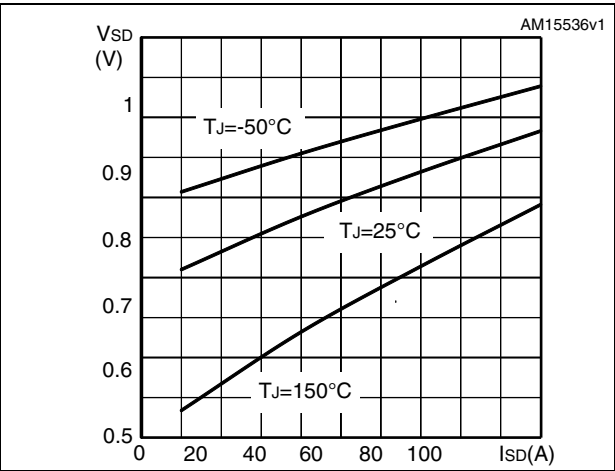


Figure 10. Normalized gate threshold voltage vs temperature

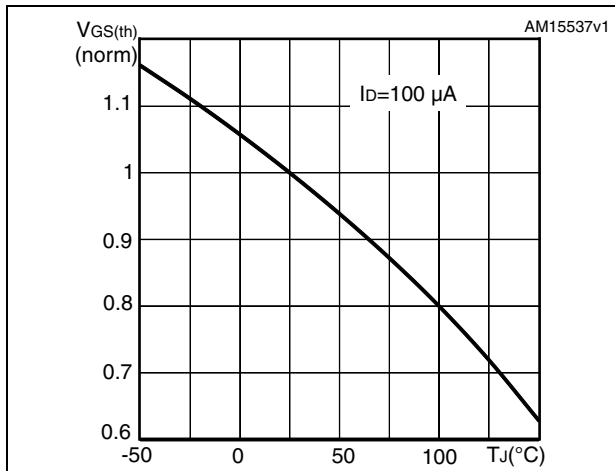


Figure 11. Normalized on-resistance vs temperature

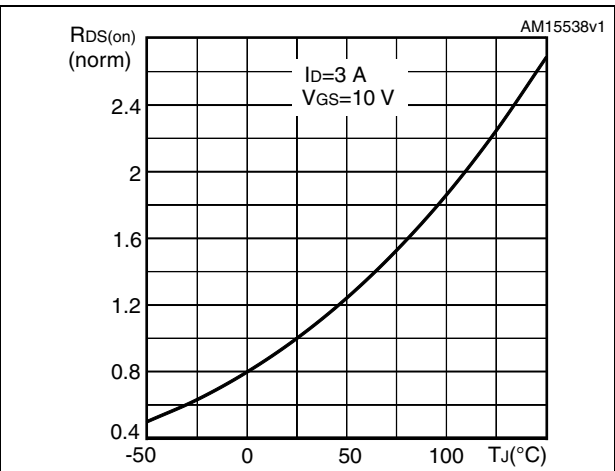


Figure 12. Normalized  $V_{(BR)DSS}$  vs temperature

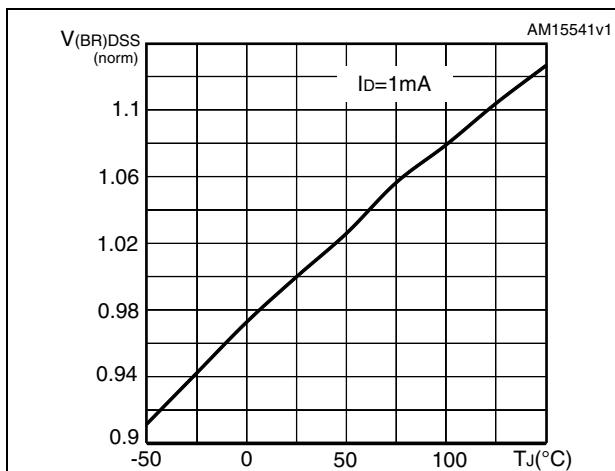
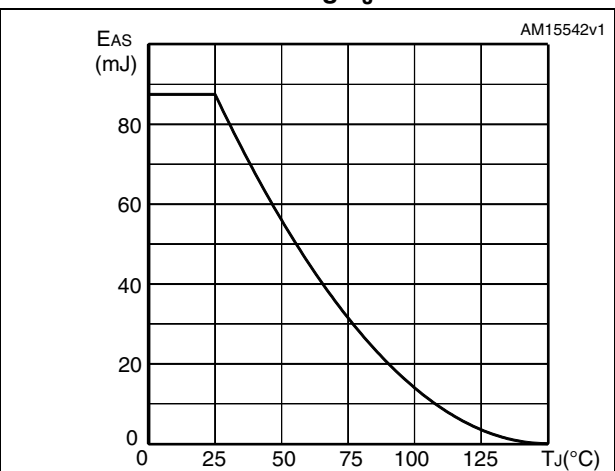


Figure 13. Maximum avalanche energy vs starting  $T_J$



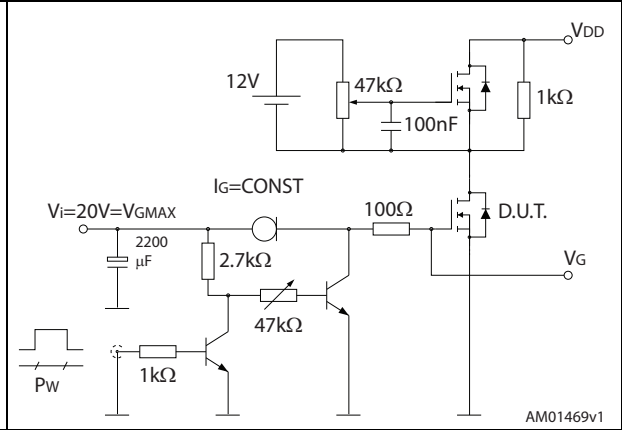
### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**



AM01468v1

**Figure 15. Gate charge test circuit**



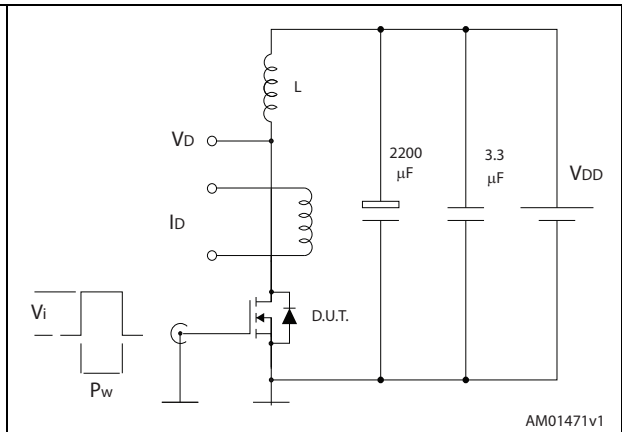
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**Figure 16. Test circuit for inductive load switching and diode recovery times**



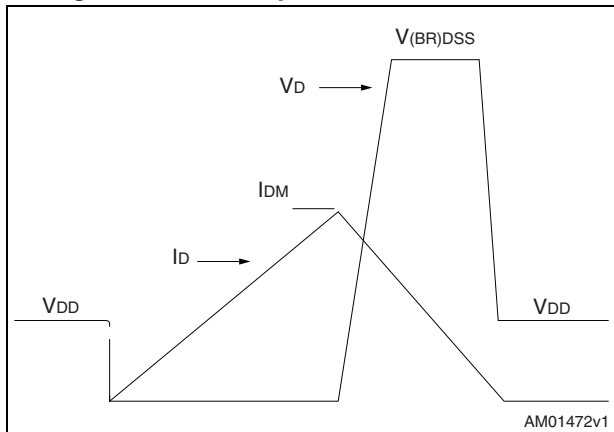
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**Figure 17. Unclamped inductive load test circuit**



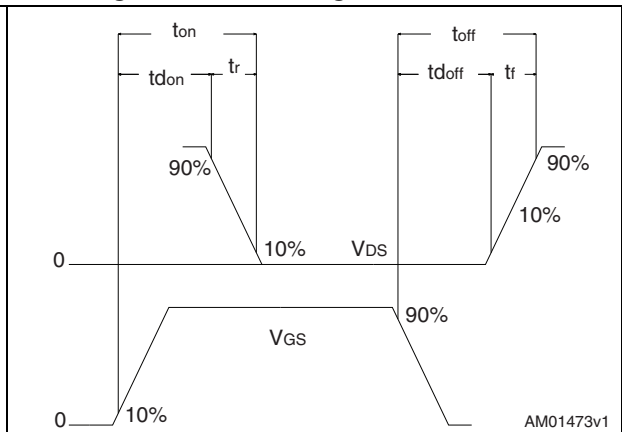
AM01471v1

**Figure 18. Unclamped inductive waveform**



AM01472v1

**Figure 19. Switching time waveform**



AM01473v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 20. TO-220FP drawing

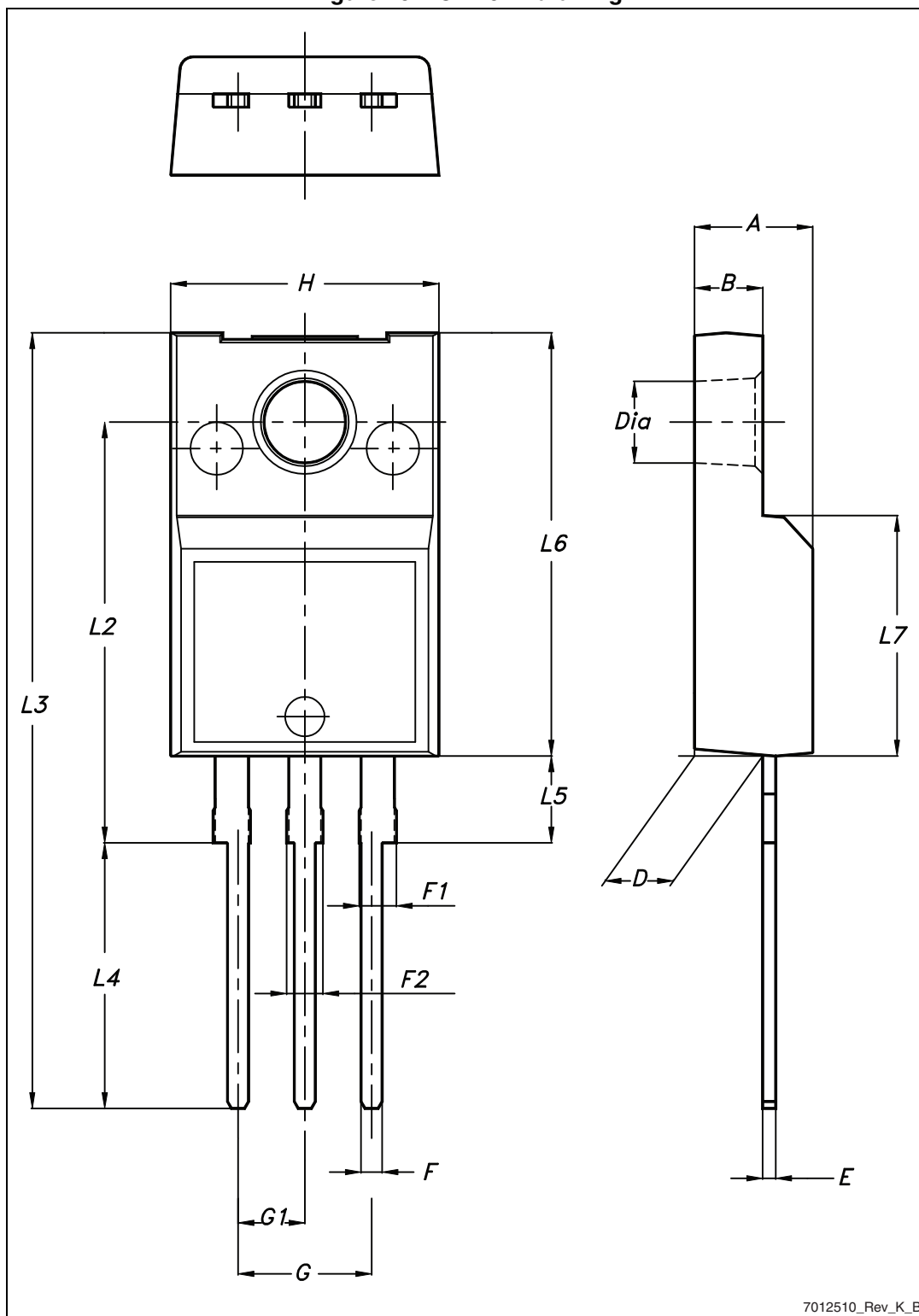
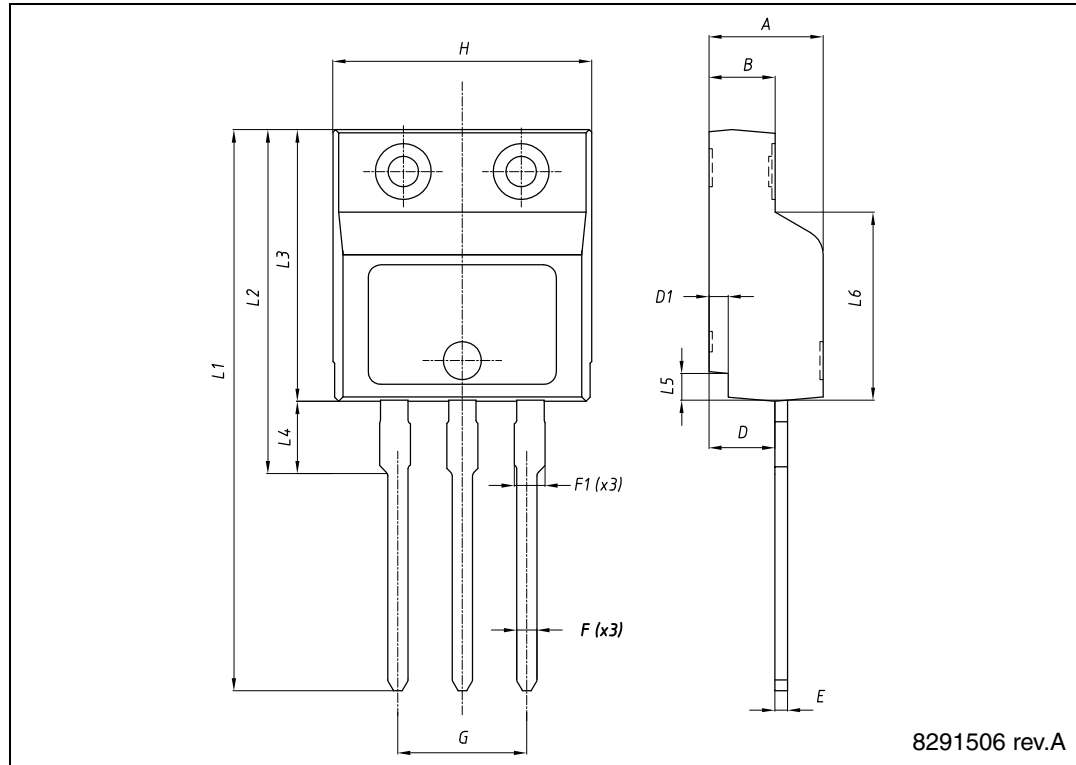


Table 10. I<sup>2</sup>PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I<sup>2</sup>PAKFP (TO-281) drawing



## 5 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
11-Oct-2013	1	First release. Part numbers previously included in datasheet DocID023448

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