



Integrated Device Technology, Inc.

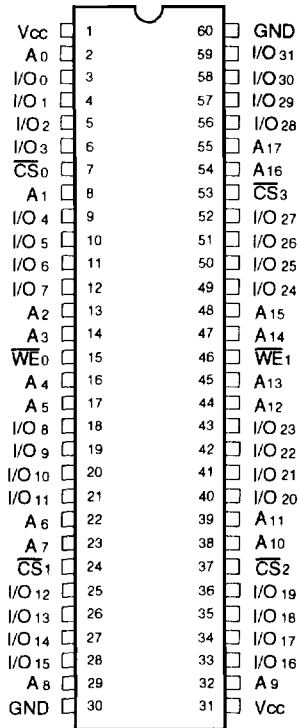
## 256K x 32 CMOS STATIC RAM MODULE

IDT7MB4067

### FEATURES:

- High density 8 megabit static RAM module
- Low profile 60 pin DIP (Dual In-line Package)
- Very fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ( $\pm 10\%$ ) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins and decoupling capacitors for maximum noise immunity

### PIN CONFIGURATION



DIP  
TOP VIEW

2830 drw 01

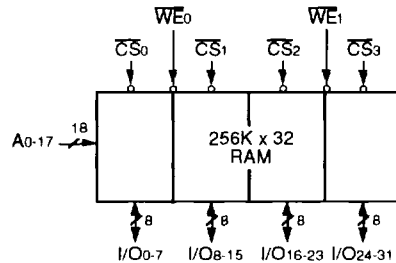
### DESCRIPTION:

The IDT7MB4067 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MB4067 is available with access time as fast as 20ns with minimal power consumption.

The IDT7MB4067 is packaged in a 60 pin DIP (Dual In-line Package). The DIP configuration allows 60 pins to be placed on a package 3.0 inches long and 0.6 inches wide and 0.365 inches tall.

All inputs and outputs of the IDT7MB4067 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

### FUNCTIONAL BLOCK DIAGRAM



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### PIN NAMES

A <sub>0</sub> -A <sub>17</sub>	Addresses
I/O <sub>0</sub> -31	Data Inputs/Outputs
$\overline{CS}_0$	Chip Select for I/O <sub>0</sub> -7
$\overline{CS}_1$	Chip Select for I/O <sub>8</sub> -15
$\overline{CS}_2$	Chip Select for I/O <sub>16</sub> -23
$\overline{CS}_3$	Chip Select for I/O <sub>24</sub> -31
$WE_0$	Write Enable for I/O <sub>0</sub> -15
$WE_1$	Write Enable for I/O <sub>16</sub> -31
GND	Ground
Vcc	Power

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COMMERCIAL TEMPERATURE RANGE

APRIL 1992

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DSC-7083/2

**CAPACITANCE** (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>I/O</sub>	Data I/O Capacitance	V <sub>(IN)</sub> = 0V	15	pF
C <sub>IN(W)</sub>	Input Capacitance (WE)	V <sub>(IN)</sub> = 0V	40	pF
C <sub>IN(C)</sub>	Input Capacitance ( $\overline{CS}$ )	V <sub>(IN)</sub> = 0V	20	pF
C <sub>IN(A)</sub>	Input Capacitance (Address)	V <sub>(IN)</sub> = 0V	75	pF

**NOTE:** 2830 tbi 02  
1. This parameter is guaranteed by design but not tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:** 2830 tbi 03  
1. V<sub>IL</sub> (min) = -2.0V for pulse width less than 10ns.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%

2830 tbi 04

**DC ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7MB4067		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage (Address and Control)	V <sub>CC</sub> = Max.; V <sub>IN</sub> = GND to V <sub>CC</sub>	—	80	μA
I <sub>LI</sub>	Input Leakage (Data)	V <sub>CC</sub> = Max.; V <sub>IN</sub> = GND to V <sub>CC</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage	V <sub>CC</sub> = Max.; $\overline{CS}$ = V <sub>IH</sub> ; V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	10	μA
V <sub>OL</sub>	Output Low	V <sub>CC</sub> = Min.; I <sub>OL</sub> = 8mA	—	0.4	V
V <sub>OH</sub>	Output High	V <sub>CC</sub> = Min.; I <sub>OH</sub> = -4mA	2.4	—	V

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Symbol	Parameter	Test Conditions	7MB4067		Unit
			Min.	Max.	
I <sub>CC</sub>	Dynamic Operating Current	f = f <sub>MAX</sub> ; $\overline{CS}$ = V <sub>IL</sub> ; V <sub>CC</sub> = Max.; Output Open	—	1200	mA
I <sub>SB</sub>	Standby Supply Current	$\overline{CS}$ ≥ V <sub>IH</sub> ; V <sub>CC</sub> = Max.; Outputs Open, f = f <sub>MAX</sub>	—	480	mA
I <sub>SB1</sub>	Full Standby Supply Current	$\overline{CS}$ ≥ V <sub>CC</sub> - 0.2V; f = 0; V <sub>IN</sub> > V <sub>CC</sub> - 0.2V or < 0.2V	—	80	mA

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**TRUTH TABLE**

Mode	$\overline{CS}$	WE	Output	Power
Standby	H	X	Hi-Z	Standby
Read	L	H	Dout	Active
Write	L	L	Din	Active

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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

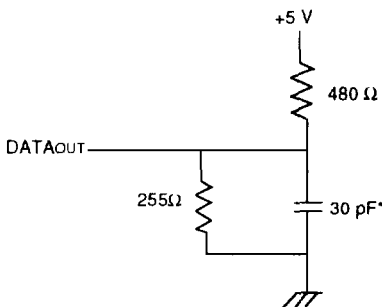
**NOTE:** 2830 tbi 06  
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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**AC TEST CONDITIONS**

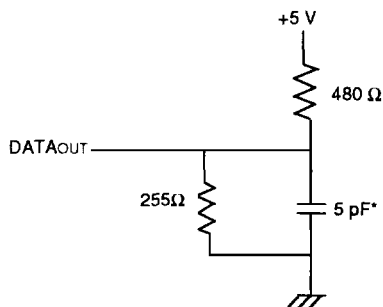
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

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2830 drw 03 \*Includes scope and jig

Figure 1. Output Load



2830 drw 04

Figure 1. Output Load  
(for tCHZ, tCLZ, tWHZ, tOW)

**AC ELECTRICAL CHARACTERISTICS** (VCC = 5V ±10%, TA = 0°C to +70°C)

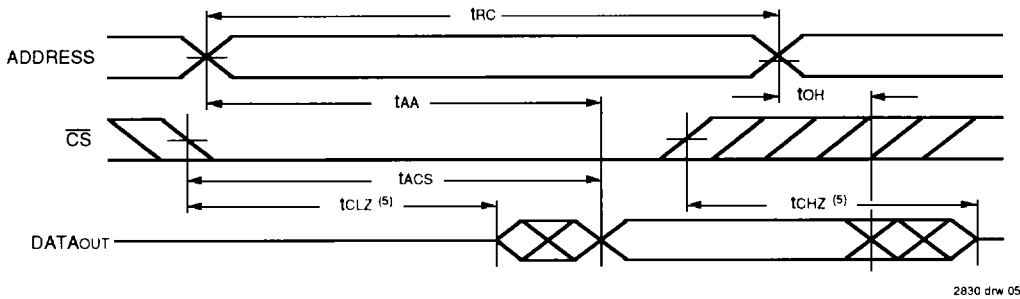
Symbol	Parameter	7MB4067SxxP										Unit
		-20 <sup>(2)</sup>		-25		-30		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ <sup>(1)</sup>	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ <sup>(1)</sup>	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
<b>Write Cycle</b>												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ <sup>(1)</sup>	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW <sup>(1)</sup>	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

**NOTES:**

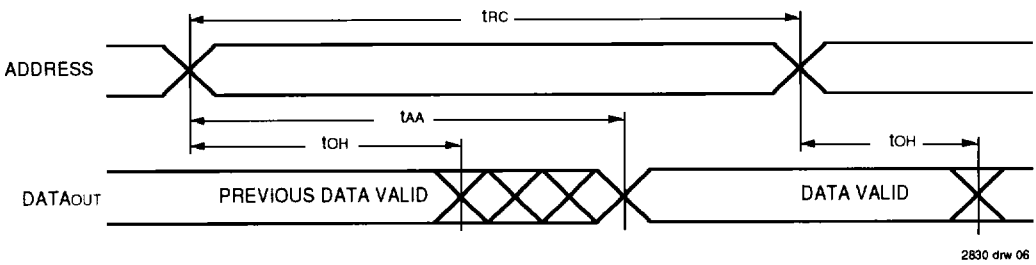
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

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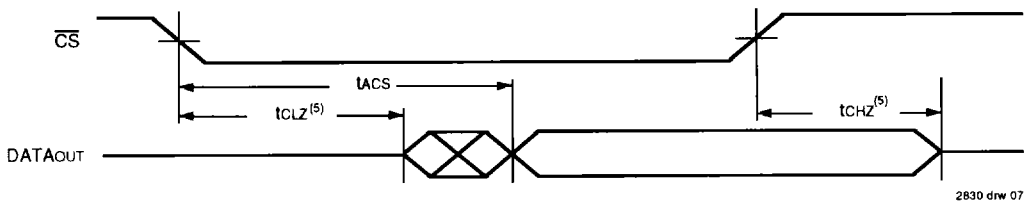
**TIMING WAVEFORM OF READ CYCLE NO. 1 (1)**



**TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)**



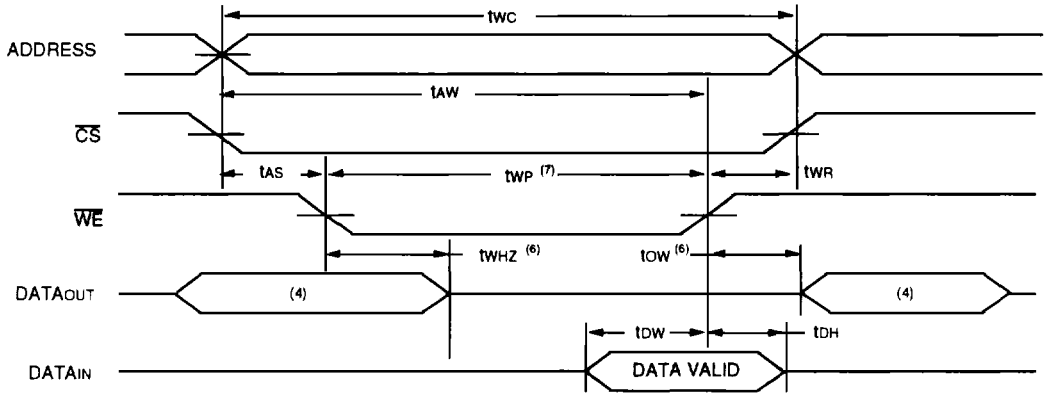
**TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)**



**NOTES:**

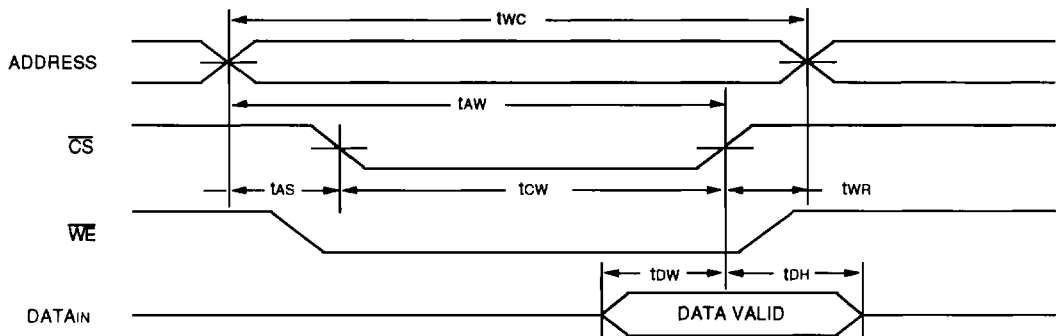
1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected.  $\overline{CS} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CS}$  transition low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 200mV$  from steady state. This parameter is guaranteed by design, but not tested.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING) (1, 2, 3, 7)**



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**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING) (1, 2, 3, 5)**

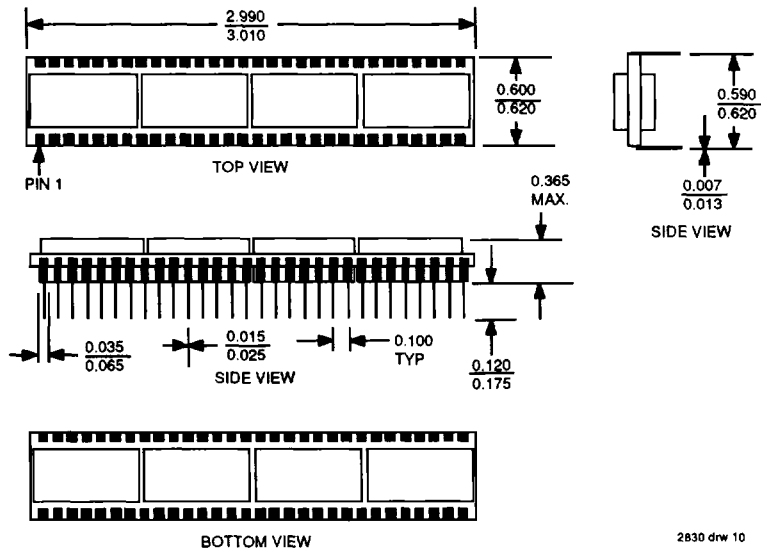


2830 drw 09

**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be high during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  low transition occurs simultaneously with or after the  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. During a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{DW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ .

PACKAGE DIMENSIONS



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