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STCH01

Advanced multi-mode power management controller for zero no-load power consumption

Datasheet - preliminary data

SO16N

Features

- CV/CC regulation with or without optocoupler (OPTO or OPTOLESS version respectively)
- Burst mode operation at no load, with wake-up from secondary side (OPTOLESS version)
- Zero power consumption in no load condition (OPTOLESS version) with excellent dynamic load transient
- Internal high voltage startup
- OVP dedicated pin with sensing from auxiliary winding of transformer
- Dedicated pin for protection purpose (PROT pin with latched or autorestart option)
- Second level OCP (transformer saturation or output rectifier short-circuit)
- Online digital trimming for the highest end product accuracy
- Intelligent frequency jitter for EMI suppression
- Low V_{DD} supply voltage operation
- Two avalanche rated internal power MOSFETs

Applications

- Adapter/plug-in charger: mobile phone, tablet, camcorder, shaver, emergency light, etc.

Description

The STCH01device is a high voltage primary switcher intended for operating directly from the rectified mains with minimum external parts.

Housed in a compact SO16N package,STCH01 embeds controller and two dedicated POWER sections in a unique full integrated solution. The device allows to implement power supplies with extremely low consumption during no-load assuring excellent dynamic load transition response without optocoupler.

The converter utilizes two operating modes:

Forced commutation mode: performed by a high-performance QR PWM controller and a low-side (LS) Power MOSFET, to serve the purpose of power storage and power control.

Self commutation mode: performed by an integrated proprietary scheme and a high-side (HS) MOSFET, to serve the purpose of resonant power release to the load.

Table 1. Device summary

Tube	Tape and reel	Version
STCH01	STCH01TR	OPTOLESS and autorestart
STCH01L	STCH01LTR	OPTOLESS and latched
STCH01NW	STCH01NWTR	OPTOLESS and autorestart
STCH01LNW	STCH01LNWTR	OPTOLESS and latched

Contents

1 Device description

The device implements a current-mode control specifically designed for quasi-resonant flyback converters operating with valley switching , available in two versions: OPTOLOESS and OPTO.

The OPTOLESS version is capable of providing constant output voltage (CV) regulation and constant output current (CC) regulation, using primary-sensing feedback. This eliminates the need for the optocoupler, the secondary voltage reference as well as the current sensor, still maintaining quite accurate regulation.

The OPTO version uses a standard secondary side CV regulation with an optocoupler, while CC regulation is still performed with the primary side sensing.

Quasi-resonant operation is achieved by means of a transformer demagnetization sensing input that triggers the LS MOSFET turn-on. The same input is dedicated also to output voltage monitoring, to perform CV regulation, and input voltage monitoring, to achieve mains independent CC regulation (line voltage feed-forward).

A blanking time after the turn-on is inserted to allow for valley-skipping operation at a medium-light load, assuring in this way high-efficiency over wide range of the output load. At a very light load, the device enters a controlled burst mode operation that, along with the built-in high voltage start-up circuit and the low operating current of the device, helps minimize the residual input consumption.

With the OPTOLESS version, in no load, light load conditions, the controller stops operating (entering a very low consumption state) and remains waiting for a wake-up signal pulse (on ZCD pin) from the secondary side.

During CC regulation, where the flyback voltage generated by the auxiliary winding drops and may be not enough to supply the internal circuits, the chip is able to power itself directly from the rectified mains through the high voltage start-up circuit.

During the burst mode operation the self-supply feature is disabled (due to very stringent no load consumption requirement), and the V_{DD} supply voltage has to be guaranteed by proper application design.

To reduce the EMI noise filtering, the device embeds a proprietary frequency jittering technique.

STCH01 allows to achieve zero power consumption consumption in no load operation thanks to the following features:

- Low operating V_{DD} voltage
- Low operating quiescent current
- Intelligent burst mode operation, with wake-up from secondary side (OPTOLESS version)
- Built-in high voltage active start-up circuit, based on depletion MOSFET

In addition to these functions that optimize power handling under different operating conditions, the device offers protection features with autorestart functionality that considerably increase end product's safety and reliability:

- Thermal shutdown with hysteresis
- Feedback disconnection feature
- Second level OCP against transformer saturation or secondary diode short-circuit

The device allows a system level trimming that improves application performance and manufacturing process.

The parameters that can be adjusted by on line digital trimming are:

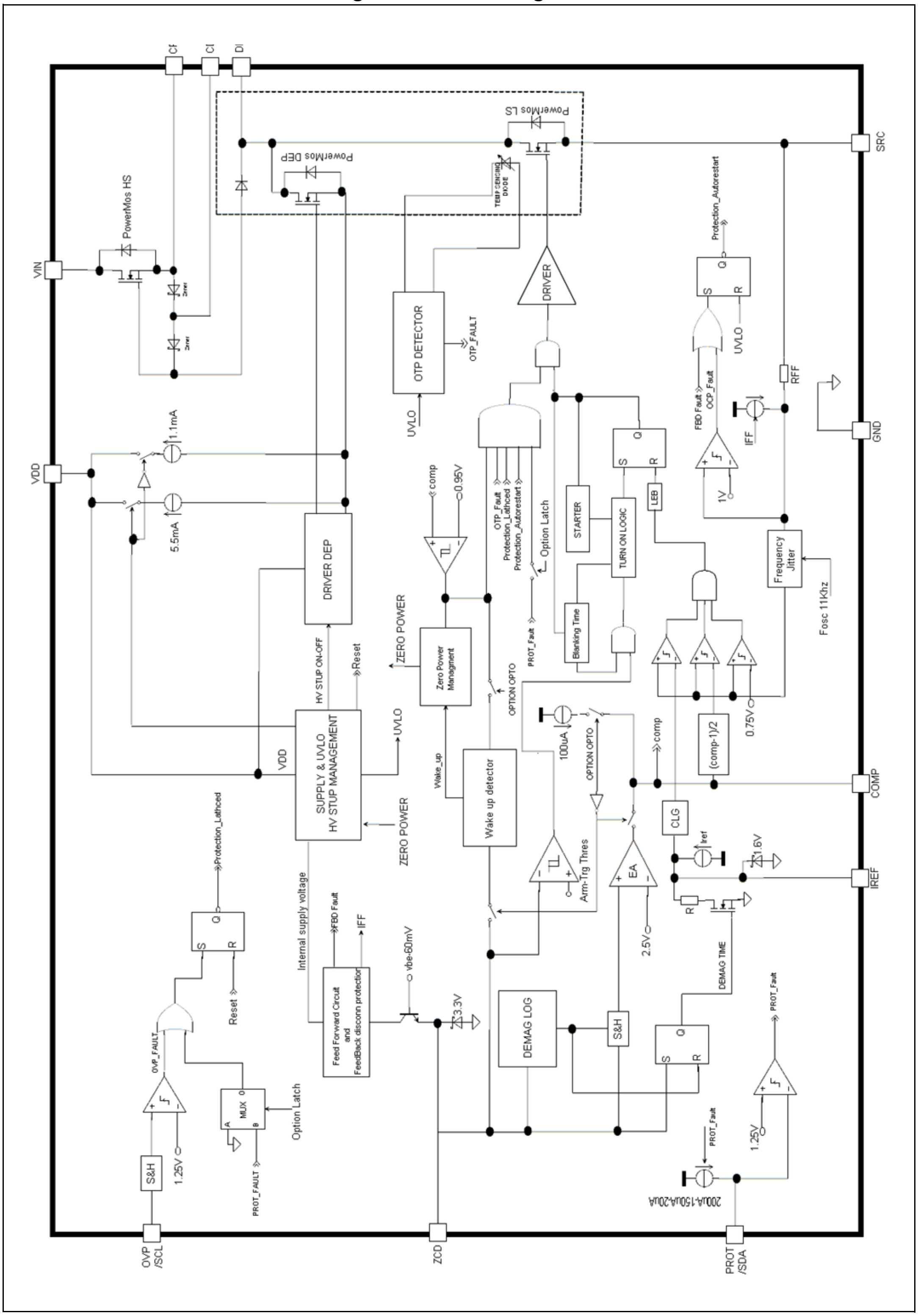
- Output voltage accuracy setting
- Output current accuracy setting
- Voltage feed-forward accuracy setting
- Frequency jitter amplitude

An OVP pin is also provided, with sensing from the auxiliary winding and latched functionality.

Furthermore, the device is equipped with a pin PROT, for a generic user defined protection circuit (like OVP or OTP): this can be the latched type or autorestart, according to the selected bit option. An embedded soft-start procedure and leading edge blanking on the current sense input for greater noise immunity complete the equipment of this device.

2 Block diagram

Figure 1. Block diagram



3 Pin functions and typical power

Table 2. Pin functions

Name	Function
VIN	Input bus voltage (from the rectified mains) connected to the drain of the internal high-side MOSFET. Pins connected to the internal metal frame to facilitate heat dissipation.
DRAIN	Drain connection of the internal low-side Power MOSFET. The internal high voltage start-up generator sinks current from these pins as well. Pins connected to the internal metal frame to facilitate heat dissipation.
CRES	A capacitor connected between this pin and the DRAIN pin sets the resonant frequency occurring after the low-side MOSFET turn-off (during transformer demagnetization).
CDRV	A capacitor connected between this pin and the DRAIN pin allows high-side MOSFET self-driving: this MOSFET is turned-on when DRAIN voltage is higher than VIN voltage and is turned-off when DRAIN voltage is lower than VIN voltage.
SRC	Source connection of the internal low-side MOSFET and input to the PWM and 2nd-OCP comparators. The current flowing in the low-side MOSFET is sensed through a resistor connected between the SRC pin and GND. The resulting voltage is sent to internal comparators to determine the MOSFET's turn-off.
GND	Circuit ground reference and current return for both the signal part of the IC and the gate drive. All ground connections of the bias components should be tied to a trace going to this pin and kept separated from any pulsed current return (sense resistor between the SRC pin and GND).
VDD	Supply voltage of the device. An electrolytic capacitor, connected between this pin and ground, is initially charged by the internal high voltage start-up generator; when the device is running the same generator will keep it charged in case the voltage supplied by the auxiliary winding is not sufficient (for example this may happen during CC regulation). This feature is disabled in case of protection tripping. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
IREF	CC regulation loop reference voltage. An external capacitor connected between this pin and GND is charged by an internal circuit to an appropriate voltage level that is used as the reference for the MOSFET's peak drain current during CC regulation. The voltage is automatically adjusted to keep constant the average output current.

Table 2. Pin functions (continued)

Name	Function
ZCD	The following functions are performed by this pin: – Transformer demagnetization sensing for quasi-resonant operation. A negative going edge falling below the V_{ZCDT} threshold triggers the MOSFET turn-on, provided the internal circuit has been previously armed by a positive going edge exceeding the V_{ZCDA} threshold. – Input voltage feed-forward compensation. By connecting the ZCD pin to the auxiliary winding through a resistor, the current sourced by the pin during the MOSFET on-time is monitored to get an image of the input voltage to the converter. This information is used by the internal circuitry to achieve a CC regulation independent of the mains voltage. – Output voltage sense through a resistive divider connected to the auxiliary winding. The voltage on the low-side resistor of the divider (connected to this pin) is sampled and held right at the end of transformer's demagnetization to get an accurate image of the output voltage to be fed to the inverting input of the internal transconductance type error amplifier. – Sensing of wake-up signal coming from the secondary side during the burst mode, through the transformer auxiliary winding (OPTOLESS version). – Feedback disconnection. If the current sourced by the pin during the low-side MOSFET turn-on does not exceed 50 µA, either a floating pin or an abnormally low input voltage is assumed, the device is stopped and restarted after V_{DD} voltage has dropped below $V_{DD\_restart}$. – Please note that the maximum I_{ZCD} sunk/sourced current has to not exceed the values indicated in the AMR section *Table 4: Absolute maximum ratings* in all the Vin range conditions (88 - 265 Vac). No capacitor is allowed between this pin and the transformer auxiliary winding.
COMP	– OPTOLESS version: output of the internal transconductance error amplifier. The compensation network will be placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop. – OPTO version: control input for duty cycle control. An internal current generator provides a bias current for voltage loop regulation (implemented through secondary side sensing and optocoupler), while the internal transconductance error amplifier is disabled and internally disconnected from the pin. A voltage below the threshold V_{COMPBM} activates the burst mode operation.
OVP/SCL	A multiplexed pin for the overvoltage protection input during the normal operation and online trimming clock input. – Output voltage sense through a resistive divider connected to the auxiliary winding for overvoltage protection purpose: the voltage sensed on this pin is compared with an internal reference V_{OVP} at the time instant when the transformer is demagnetized (and the auxiliary winding voltage is a representative value of the output voltage through the turn ratio); if the internal threshold V_{OVP} is surpassed, then an overvoltage condition is assumed and the circuit enters a latched protection mode. After protection tripping, a mains recycle is necessary for a new restart attempt. – In case OVP function is not used, the pin has to be connected to GND through a resistor (5 kΩ to 30 kΩ). – Clock (SCL) logic input for I^2C serial communication protocol. This pin will be externally pull-up to 3.6 V max. A small internal pull-up is present to prevent false signal detection (the pin is floating during normal operation).
PROT/SDA	A multiplexed pin for a generic protection input during normal operation and online trimming data input. – Generic protection input pin (active LOW): when the voltage on this pin is lower than the V_{PROT} threshold, the protection detection circuit stops device operation (latch type or autorestart mode according to the selected option). If this pin is not used, keep it open (not connected). – Data (SDA) logic input/output for I^2C serial communication protocol. This pin will be externally pull-up to 3.6 V max. A small internal pull-up is present to prevent false signal detection (the pin is floating during normal operation).

Table 3. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
STCH01	12.5W	18W	10W	12.5W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient
2. Maximum continuous power in an open frame design at 50°C ambient with adequate heat sinking

4 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS\_LS\_MOS}$	Low-side MOSFET drain-to-source voltage	650	V
$V_{DS\_HS\_MOS}$	High-side MOSFET drain-to-source voltage	500	V
$E_{AV\text{-}LS\text{-}MOS}$	Single pulse avalanche energy, starting T_J = 25 °C, $I_d = I_{as}$ = 0.7 A (single pulse avalanche current)(1)	20	mJ
$E_{AV\text{-}HS\text{-}MOS}$	Single pulse avalanche energy, starting T_J = 25 °C, $I_d = I_{as}$ = 0.7 A (single pulse avalanche current)(1)	20	mJ
$I_{DRAIN\ (LS\text{-}MOS)}$	Low-side MOSFET drain current (pulsed)	1.5	A
$I_{DRAIN\ (HS\text{-}MOS)}$	High-side MOSFET drain current (pulsed)	1.5	A
$V_{D\text{-}RRM}$	Diode (D) for high-side MOSFET drive repetitive peak reverse voltage	300	V
I_{FD}	Diode (D) for high-side MOSFET drive forward current (pulsed, 200 ns)	0.2	A
$I_{FZD1,2}$	Internal diodes (ZD1, ZD2) forward current (pulsed, 200 ns)	0.2	A
V_{DD}	Device supply voltage (I_{DD} < 25 mA)	-0.3 to self-limited	V
V_{ZCD}	ZCD pin voltage (-3 mA $\leq I_{ZCD} \leq$ +3 mA)	-0.3 to self-limited	V
V_{OVP}	OVP pin voltage (-3 mA $\leq I_{ZCD} \leq$ +3 mA)	-0.3 to self-limited	V
V_{PROT}	Protection pin voltage	-0.3 to 3	V
-	Analog/digital pin voltages	-0.3 to 3.6	V

1. Pulse width limited by T_J = 150 °C.

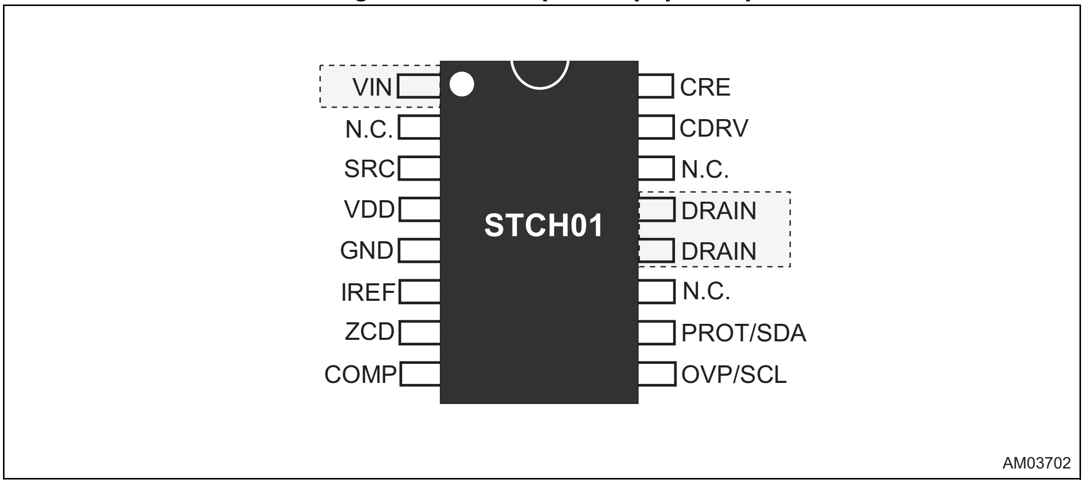
Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions may affect device reliability.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{TH\text{-}AMB}$	Thermal resistance junction ambient(1)	120	°C/W
P_{TOT}	Max. power dissipation at T_{amb} = 50 °C	0.8	W
T_J	Junction temperature range	-40 to 150(2)	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. Mounted on a standard single side FR4 board with 50 mm^2 of Cu (35 µm thick) under DRAIN and VIN pins.
2. Max T_J = 150 °C refers to the embedded MOSFET.

Figure 2. Device pinout (top view)



1. The copper area for heat dissipation has to be designed under the highlighted pins, connected respectively to DRAIN and VIN signals.

5 Electrical characteristics

Table 6. Electrical characteristics
(T_J = -25 °C to 125 °C, V_{DD} = 8 V; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
LOW-SIDE MOSFET						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_{DRAIN} < 100 µA; T_J = 25 °C	650			V
I_{OFF}	Off state drain leakage current	V_{DS} = 650 V; T_J = 125 °C, V_{DD} = 8 V, V_{COMP} < V_{COMPBM}, V_{ZCD} connected to GND			4	µA
$R_{DS(on)}$	Static drain-source ON-resistance	I_D = 1 A; T_J = 25 °C			4	Ω
		I_D = 1 A; T_J = 125 °C			8.8	
$C_{OSSeq.}$	Equivalent output capacitance	V_{DS} = 0 to 480 V; T_J = 25 °C		30		pF
HIGH-SIDE MOSFET						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_{DRAIN} < 100 µA; T_J = 25 °C	500			V
I_{OFF}	Off state drain leakage current	V_{DS} = 500 V; T_J = 125 °C			1	µA
$R_{DS(on)}$	Static drain-source ON-resistance	V_{CDRV} - V_{CRES} = 10 V; I_D = 1 A; T_J = 25 °C			8	Ω
		V_{CDRV} - V_{CRES} = 10 V; I_D = 1 A; T_J = 125 °C			17.6	
$C_{OSSeq.}$	Equivalent output capacitance	V_{DS} = 0 to 480 V; T_J = 25 °C		25		pF
INTERNAL DIODE (D) for high-side MOSFET drive						
V_R	Reverse voltage	I_R < 1 µA	300			V
V_F	Forward drop	I_F = 20 mA; T_J = 25 °C			1	V
INTERNAL ZENER DIODES (ZD1, ZD2) for high-side MOSFET drive						
$V_{ZD1,2}$	ZD1, 2 Zener voltage	I_R = 5 mA; T_J = 25 °C	10	15	20	V
$V_{FZD1,2}$	Zener diode forward drop	I_F = 2 mA; T_J = 25 °C		1.7	1.9	V
$R_{D1,2}$	Dynamic resistance	I_F = 2 to 10 mA; T_J = 25 °C			300	Ω
SUPPLY SECTION						
V_{DS_START}	Drain-source start voltage		55	62	67	V

Table 6. Electrical characteristics
(T_J = -25 °C to 125 °C, V_{DD} = 8 V; unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD_CH}	Start-up charging current	$V_{DRAIN} > V_{DS\_START}$; V_{DD} = 4 V	-3.5	-5.5	-8	mA
		$V_{DRAIN} > V_{DS\_START}$; V_{DD} < 0.6 V (V_{DD} shorted or after protection tripping)	-0.7	-1.1	-1.72	mA
V_{DD}	Operating voltage range	After turn-on	5.75		23.5	V
V_{DD_clamp}	V_{DD} clamp voltage	I_{DD} = 5 mA	23.5			V
V_{DD_on}	V_{DD} turn-on threshold	V_{DRAIN} = 120 V	10	11(1)	12	V
V_{DD_off}	V_{DD} shutdown threshold		4.75	5.25(1)	5.75	V
$V_{DD\_restart}$	V_{DD} (falling) restart voltage	Normal operation	5	5.5 (1)	6	V
		After AUTORESTART or LATCH protection	4.5	5(1)	5.5	V
$I_{DD\_st\text{-}up}$	Before start-up current	$V_{DRAIN} > V_{DS\_START}$;			250	µA
I_{DDo}	Quiescent current (not switching between bursts)	$V_{COMP} = V_{COMPL}$ (no OPTO) $V_{DD} = V_{DD\_on}$ - 0.2 V			50	µA
		$V_{COMP} = V_{COMPL}$, (with OPTO)			350	µA
I_{DD}	Operating supply current	V_{DS} = 120 V; F_{SW} = 100 kHz		1.3		mA
I_{DD_fault}	Operating supply current with protection tripping	PROT open			350	µA
		PROT shorted			550	µA
CONTROLLER SECTION						
Zero current detection						
I_{ZCD_bias}	Input bias current	V_{ZCD} = 0.1 to 3 V			1	µA
V_{ZCD_H}	Upper clamp voltage	I_{ZCD} = 1 mA		3.3		V
V_{ZCD_L}	Lower clamp voltage	I_{ZCD} = -1 mA		-60		mV
$V_{ZCD\_A\_TH}$	Arming voltage threshold	Positive going edge		110		mV
$V_{ZCD\_T\_TH}$	Trigger voltage threshold	Negative going edge		60		mV
I_{ZCD_ON}	Minimum source current during MOSFET on-time		-25	-50	-75	µA
T_{BLANK}	Blanking time after turn-on	V_{COMP} > 1.3 V		6		µs
		V_{COMP} < 0.9 V		30		µs
T_{D_ZCD}	Fixed turn-on delay after ZCD triggering			450		ns
Wake-up pulse detection (OPTOLESS version)						
$V_{ZCDwupTH}$	Wake-up threshold on ZCD pin (for burst-mode exiting)	Positive going edge	0.6	0.7	0.8	V
T_{WUP_min}	Min wake-up pulse width above wake-up threshold		1.2			µs

Table 6. Electrical characteristics (T_J = -25 °C to 125 °C, V_{DD} = 8 V; unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{WUP_mask}	Wake-up masking time after burst-mode entering		46	50	54	µs
Transconductance error amplifier						
V_{REF}	Voltage reference	(1)V_{DD} within supply range	2.45	2.5	2.55	V
gm	Transconductance	ΔI_{COMP} = ±10 µA V_{COMP} = 1.65 V		1		mS
Gv	Voltage gain	Open loop		70		dB
GB	Gain-bandwidth product			0.5		MHz
I_{COMP}	Source current	V_{ZCD} = 2.3 V, V_{COMP} = 1.65 V	70	100		µA
		OPTO bit option	70	100	130	µA
	Sink current	V_{ZCD} = 2.7 V, V_{COMP} = 1.65 V	550	750		µA
V_{COMPH}	Upper COMP Voltage	V_{ZCD} = 2.3 V		2.7		V
V_{COMPL}	Lower COMP Voltage	V_{ZCD} = 2.7 V		0.7		V
V_{COMPBM}	Burst mode threshold	Voltage falling		0.95		V
Hys	Burst mode hysteresis	Voltage rising		50		mV
Current reference						
V_{IREFx}	Maximum value	(1)$V_{COMP} = V_{COMPL}$	1.5	1.6	1.7	V
G_I	Current loop gain	(2)$V_{COMP} = V_{COMPH}$		0.5		
V_{CREF}	Current reference voltage			0.4		V
$G_I * V_{CREF}$			190	200	210	mV
Current sense						
V_{CSx}	Max. clamp value	(1)dVcs/dt = 200 mV/µs	0.7	0.75	0.8	V
V_{CSdis}	Hiccup mode OCP level		0.92	1	1.08	V
T_D	Propagation delay			250		ns
T_{LEB}	Leading edge blanking			250		ns
T_{ON_min}	Minimum on-time			500		ns
Input voltage feed-forward						
R_{FF}	Equivalent FF resistor	I_{ZCD} = -1 mA	54	60	66	Ω
Frequency jittering						
F_M	Modulation frequency		10	11	12	kHz
Duty	Modulation duty cycle			50		%
ΔIpk	Peak current change	(default BIT option)		5		%
Starter						
$T_{STARTER}$	Starter period	ZCD not armed		180		µs

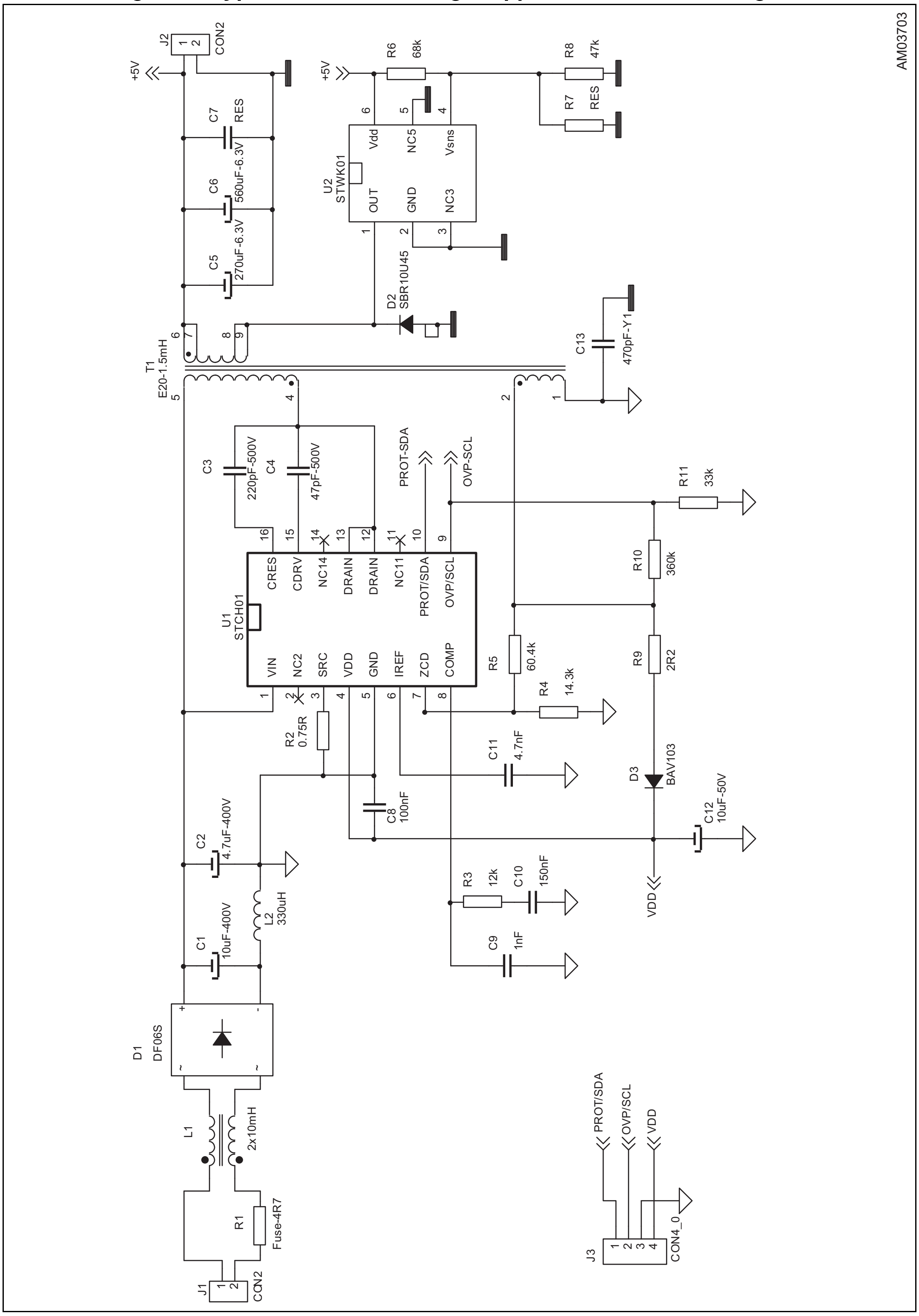
Table 6. Electrical characteristics
(T_J = -25 °C to 125 °C, V_{DD} = 8 V; unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OVP function						
V_{OVP}	Overvoltage threshold	(1) V_{DD} within supply range	1.204	1.254	1.304	V
V_{OVP_H}	Upper clamp voltage	I_{ZCD} = 1 mA		3.3		V
V_{OVP_L}	Lower clamp voltage	I_{ZCD} = -1 mA		-60		mV
Protection pin						
V_{PROT_SD}	Shutdown threshold		1.204	1.254	1.304	V
I_S	Source current	V_{PROT} = 1.24 V	-165	-200	-225	µA
I_{S_FAULT}	Source current	V_{PROT} = 0 V, V_{DD} rising from $V_{DD\_restart}$ to 11 V autorestart option	-125	-150	-175	µA
		V_{PROT} = 0 V, V_{DD} rising from $V_{DD\_restart}$ to 11 V LATCH option		-20		µA
$V_{PROT-CLP}$	Clamp voltage	Pin open	3			V
C_{max}	Max external capacitance				13	pF
Trimming functions						
V_{SCL_LOW}	SCL input low level				0.8	V
V_{SCL_HI} (2)	SCL input high level		2		3.45	V
C_{SCL}	SCL input capacitance				5	pF
f_{SCL}	SCL frequency				100	KHz
V_{SDA_LOW}	SDA input low level				0.8	V
V_{SDA_HI} (2)	SDA input high level		2		3.45	V
C_{SDA}	SDA input capacitance				5	pF
V_{DDzap}	PROM zapping voltage		17		20	V
I_{ZAP}	PROM zapping current	V_{DD}= 19 V		50	90	mA
t_{ZAP}	PROM zapping time	V_{DD} = 19 V		34	45	ms
V_{REF}	Trimming range (5 bits)	Referred to 0% trimming	-9		9	%
ΔV_{REF}	Trimming step			0.6		%
$G_I * V_{CREF}$	Trimming range (4 bits)	Referred to 0% trimming	-10.5		10.5	%
$\Delta G_I * V_{CREF}$	Trimming step			1.5		%
R_{FF}	Trimming range (3 bits)	Referred to 0% trimming	-17.5		17.5	%
ΔR_{FF}	Trimming step			2.5		%
ΔIpk	Frequency jitter amplitude levels:% of peak current change	No jitter		0		%
		Default value. For the other values, refer to *Table 19*.		5		%

1. All voltages in tracking.
2. SDA and SCL inputs are connected to an internal bus at 3.3 V even if they are protected to V_{DD} as AMR.

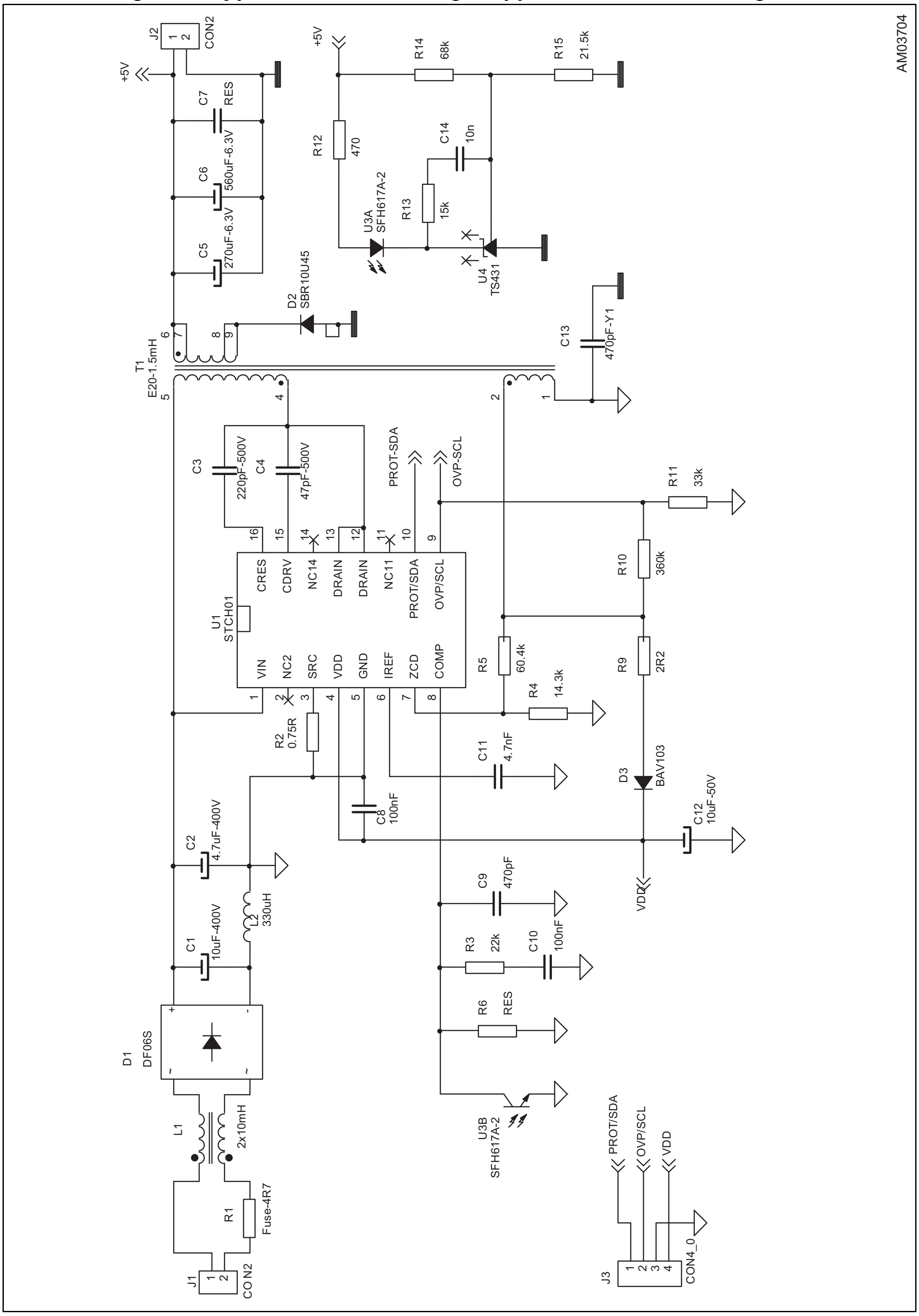
6 Typical application - OPTOLESS version

Figure 3. Typical +5 V -8 W charger application electrical diagram



7 Typical application - OPTO version

Figure 4. Typical +5 V -8 W charger application electrical diagram



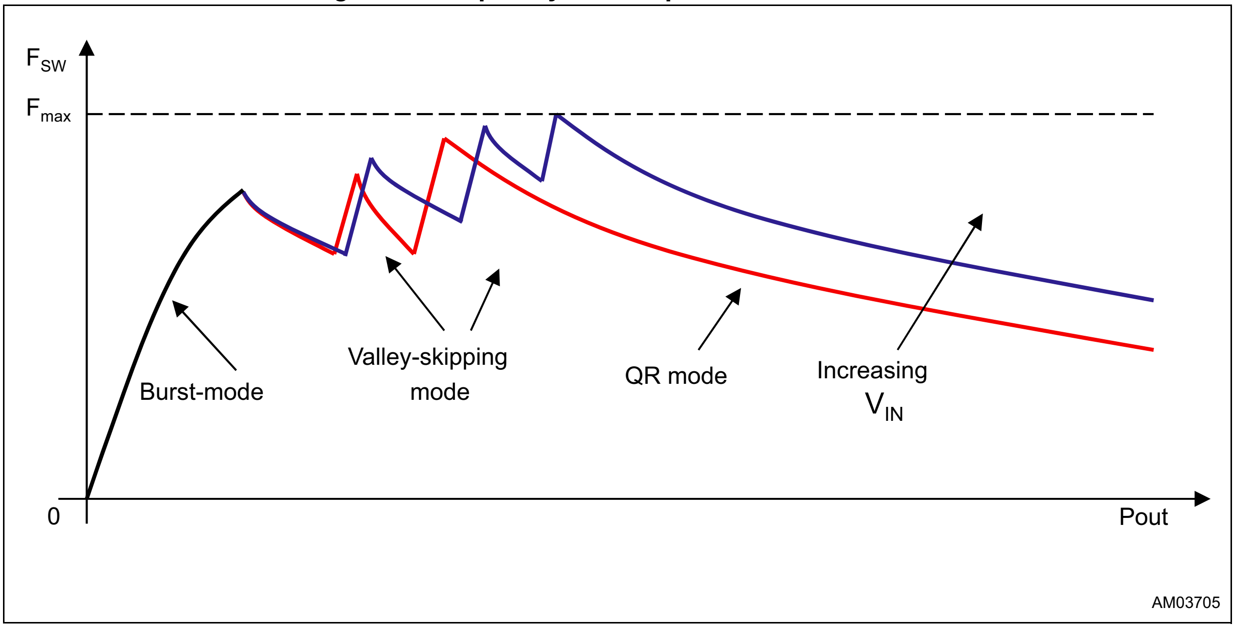
8 Operation description

The STCH01device is a high-performance switching regulator, specific for off-line QR flyback topology; it combines a low-voltage PWM controller with two avalanche rugged Power MOSFETs in the same package: the low-side one is the main switch of the topology, the high-side one is used for controlling the resonant frequencies. In the OPTOLESS version, the controller includes the current mode PWM logic and the ZCD circuit for QR operation, and regulates the output voltage and current, basing on primary-sensing feedback. The auxiliary winding voltage is sampled by a sample and hold circuit just at the end of transformer demagnetization, when its voltage is proportional to the output voltage through the transformer turn ratio, triggered by the demagnetization sensing circuit. The sensed voltage is then sent to the error amplifier and its output to the constant voltage PWM comparator. The demagnetization circuit also allows obtaining a reference voltage (proportional to the output current) for the constant current PWM comparator. In the OPTO version, the internal error amplifier is disabled and a current generator provides to the COMP pin the required feedback current, allowing to regulate the output voltage (sensed at the secondary side) through the optocoupler connected to the COMP pin.

The device provides protection features with autorestart functionality that increases the end product safety and reliability, like the feedback disconnection protection, the second level OCP circuit (suitable for detection of transformer saturation or output diode short-circuit) and the thermal shutdown with hysteresis. A dedicated protection pin (PROT) is also available for a generic user defined protection (like OTP or OVP), that can be autorestart or latched, according to the selected device version. Other features, like an embedded soft-start, frequency jitter for EMI reduction and leading edge blanking on the current sense input, complete the device equipment, giving the user flexibility and ease of use in designing an end product very robust and performing, with high-efficiency and extremely low no load consumption as well and, above all, with a very low component count.

The PWM logic works in the QR mode at the nominal load, in the valley-skipping mode at a lighter load and in the burst mode with a very low load or no load. In the QR mode the controller turns on the low-side Power MOSFET at the end of the transformer demagnetization, by detecting the resulting negative going edge of the voltage across the auxiliary winding of the transformer. The MOSFET turn-off is instead decided by the PWM comparator when the drain current reaches the peak value needed for the output voltage or the output current regulation; therefore the operating switching frequency will be different for different line and load conditions. At lower load levels, the valley-skipping mode is activated. In fact, depending on the COMP pin voltage, a blanking time from the turn-on instant (increasing with decreasing COMP voltage) is internally set, limiting the maximum operating frequency. As a consequence, the MOSFET turn-on will not any more occur on the first valley but on the second one, the third one and so on. In this way a "frequency clamp" effect is achieved (see *Figure 5*).

Figure 5. Frequency mode operation versus load



While reducing the load, the COMP pin voltage progressively reduces: at no load or a very light load, it goes below the threshold V_{COMPBM} and consequently the controller stops operation and reduces its consumption. With the OPTO version, the operation restarts as soon as the COMP pin, due to feedback reaction at the operation stop, increases above the V_{COMPBM} level plus the burst mode hysteresis (Hys).

In case of the OPTOLESS version, instead, once stopped the operation, the controller remains in a very low consumption state waiting for a wake-up signal pulse (on ZCD pin). A dedicated IC at the secondary side (STWK01 companion of the primary controller OPTOLESS version) detects the primary side operation stop and starts monitoring the output voltage: when this decreases (due to the residual output consumption) below a user defined voltage threshold, the STWK01 IC releases a wake-up pulse via the transformer windings, that is sensed by the ZCD pin through the resistive divider connected to the auxiliary transformer winding; consequently the STCH01controller resumes operation (see *Section 8.9: Burst mode operation (OPTOLESS version) on page 30*.

8.1 Low-side POWER SECTION and gate driver

The low-side POWER SECTION guarantees safe avalanche operation within the specified energy rating as well as high dv/dt capability.

The Power MOSFET gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize the common mode EMI. Under UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the Power MOSFET cannot be turned on accidentally. The driver is also provided with a voltage clamp to limit the gate charge to the MOSFET in case of higher V_{DD} supply.

8.2 High-side POWER SECTION and resonant frequency control

The device integrates also a high-side POWER SECTION to control resonant frequencies. The high-side MOSFET connects and disconnects a capacitor Cr (placed between CRES and DRAIN pins) in parallel to the primary winding of the power transformer. In this way the converter operates at two different resonant frequencies: a high resonant frequency when Cr is disconnected and a lower resonant frequency when Cr is connected to the transformer primary inductance. The energy stored in the circuit during the two portions of resonant cycles in principle may provide ZVS ("Zero Voltage Switching") operation for both low and high-side Power MOSFETs, thus increasing the overall converter efficiency.

The MOSFET is automatically driven ON and OFF depending on the external circuit operation; only
a capacitor (47 - 100 pF) is needed, connected between the CDRV and DRAIN pins. In particular the high-side MOSFET is ON when the drain voltage across the low-side MOSFET is higher than the input voltage and is OFF when the drain voltage is lower than VIN.

8.3 High voltage startup generator

Based on a depletion MOSFET embedded into the low-side MOSFET structure, the HV current generator is supplied through the DRAIN pin and is enabled only if the input bulk capacitor voltage is higher than the V_{DS_START} threshold. When the HV current generator is ON, the I_{DD_CH} current is delivered to the capacitor on the V_{DD} pin. As the voltage across the V_{DD} capacitor reaches the start-up threshold V_{DD_on}, the UVLO signal is asserted high and enables the low-side MOSFET switching, while the HV current generator is turned off. The IC is powered by the energy stored in the V_{DD} capacitor until the self-supply circuit (from an auxiliary winding of the transformer) develops a voltage high enough to sustain the operation.

The chip is able to power itself directly from the rectified mains through the HV start-up circuit: when the voltage on the V_{DD} pin falls below $V_{DD\_restart,}$ during each MOSFET's off-time, the HV current generator is turned on and charges the supply capacitor until it reaches the V_{DD_on} threshold again. In this way, the self-supply circuit develops a voltage high enough to sustain the operation of the device. This feature is useful especially during CC regulation, when the flyback voltage generated by the auxiliary winding alone may be not enough to keep V_{DD} above $V_{DD\_restart}$.

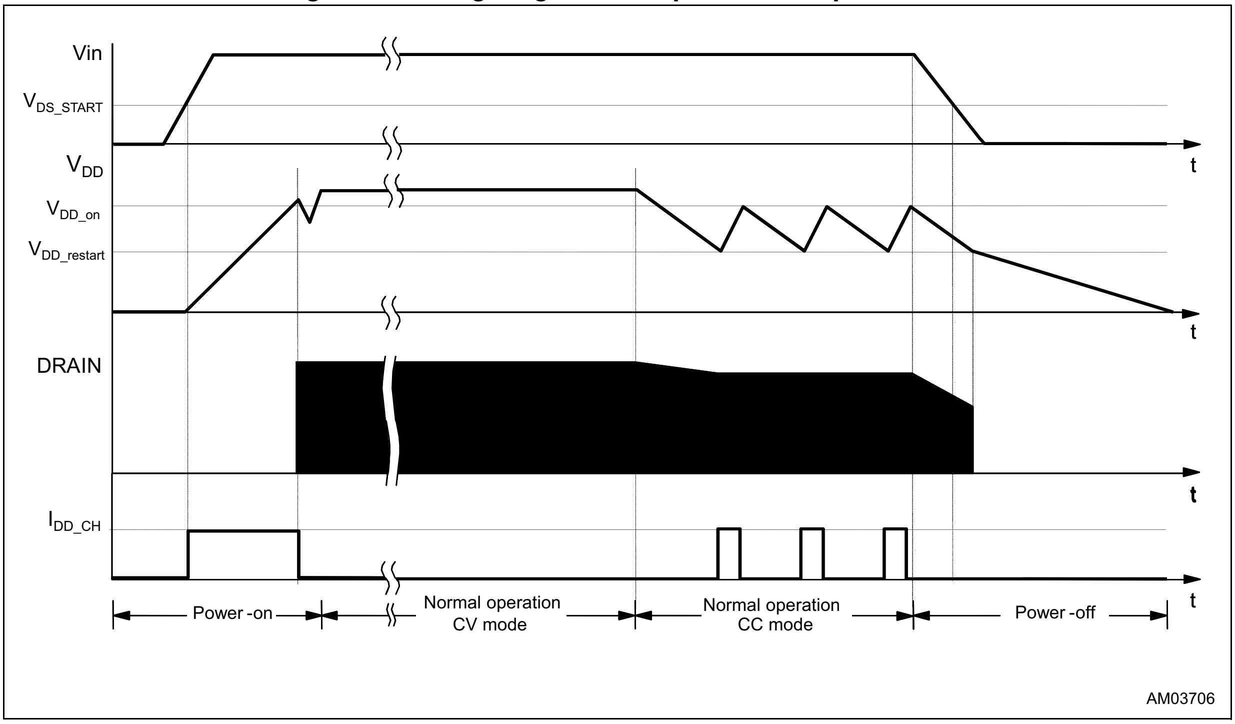
After an autorestart type protection tripping, the $V_{DD\_restart}$ value is reduced (below V_{DD_off}) and the HV generator provides only about 20% of I_{DD_CH} full value, allowing for a lower repetition rate of restart attempts (reduced input power consumption and depletion MOSFET stress).

When at no load or a very light load the controller stops operating and remains waiting for the wake-up signal, the VDD is not controlled and the HV start-up generator is not restarted in case the $V_{DD\_restart}$ is reached. Therefore, during the burst mode operation the VDD voltage has to be always higher than V_{DD_off} by a proper design of the transformer auxiliary winding turns and of the capacitor value on the V_{DD} pin.

Figure 6 shows the time diagram during the various operating conditions, from power-on to power-off, with the typical restart during CC regulation, when the transformer auxiliary winding is not enough to sustain the device supply voltage. At converter power-down the system will lose regulation as soon as the input voltage falls below V_{DS_START}. This prevents converter's restart attempts and ensures monotonic output voltage decay at system power-down.

In order to avoid overheating of the HV current generator in case of a short-circuit on V_{DD}, the full current I_{DD_CH} is delivered only if the V_{DD} voltage is detected higher than a V_{be} threshold, otherwise it is reduced to about 20% of I_{DD_CH} full value.

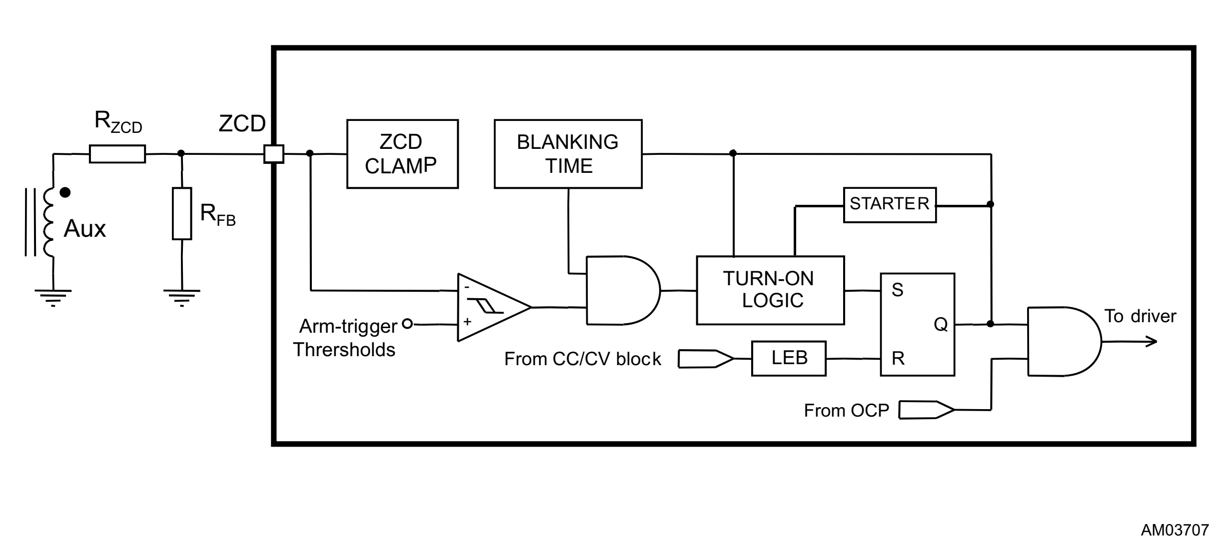
Figure 6. Timing diagram from power-on to power-off



8.4 Zero current detection circuit

The quasi-resonant operation is accomplished through the zero current detection (ZCD) circuit, which allows the turn-on of the power section at the end of the transformer demagnetization. The input signal for the ZCD pin is obtained from the transformer auxiliary winding, the same used to get the V_{DD} supply voltage of the controller (*Figure 7*).

Figure 7. ZCD circuit and turn-on logic



The voltage on the ZCD pin is both top and bottom limited by a double clamp: the upper clamp V_{ZCD_H} (positive) and the lower clamp V_{ZCD_L} (negative). The interface between the ZCD pin and the auxiliary winding is a resistor divider. The resistance ratio as well as the individual resistance values have to be properly chosen (see *Section 8.5: Constant voltage regulation (OPTOLESS version) on page 24* and *Section 8.6: Constant voltage regulation (OPTO version) on page 25* and *Section 8.8: Voltage feed-forward block on page 28*).

When the triggering circuit senses a negative going edge of the signal applied to the ZCD pin going below the $V_{ZCD\_T\_TH}$ threshold, the internal low-side MOSFET is turned on, after a fixed delay that helps to achieve the minimum drain-source voltage, resonating after the demagnetization. However, to enable the MOSFET turn-on, the triggering circuit has to be previously armed by a positive going edge of the ZCD pin voltage exceeding the $V_{ZCD\_A\_TH}$ threshold.

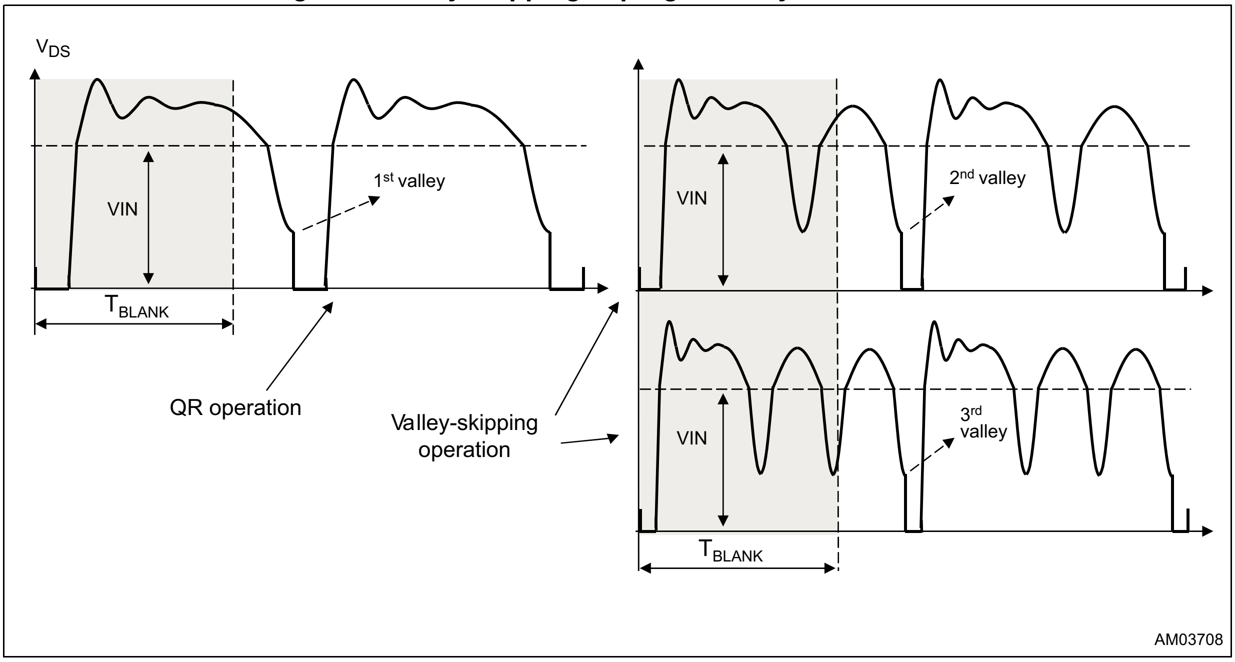
A starter block allows to turn on the MOSFET during the converter power-up, when no or a too small signal is available on the ZCD pin. After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes large enough to arm the ZCD circuit, the MOSFET's turn-on will start to be locked to transformer demagnetization, hence setting up QR operation. The starter is activated also when the IC is in CC regulation and the output voltage is not high enough to allow the ZCD triggering.

After the MOSFET turn-on, a blanking time is inserted, whose value depends on the COMP pin voltage: it is T_{BLANK} = 30 µs for V_{COMP} = 0.9 V, and decreases almost linearly down to T_{BLANK} = 6 µs for $V_{COMP} \geq 1.3$ V. This blanking time has two aims; the first is to prevent erroneous triggering due to the noise generated after the demagnetization of the transformer leakage inductance; the second is to avoid the operating frequency may increase above certain limits that would impair system efficiency, especially in medium and light load operation and high input voltage.

As a consequence of the blanking time, the MOSFET turn-on may occur not on the first valley but on the second one, the third one and so on, depending on the operating condition, leading to a valley-skipping mechanism that progressively reduces the operating frequency and improves system efficiency.

Figure 8 shows the valley-skipping mechanism: if the demagnetization completes - hence a negative going edge appears on the ZCD pin - after a time exceeding time T_{BLANK} from the previous turn-off, the MOSFET will be turned on again, (with a fixed delay to ensure minimum voltage at turn-on). If, instead, the negative going edge appears before T_{BLANK} has elapsed, it will be ignored and only the first negative going edge after T_{BLANK} will turn-on the MOSFET. In this way one or more drain ringing cycles will be skipped and the switching frequency will be prevented from exceeding 1 / T_{BLANK}.

Figure 8. Valley-skipping at progressively reduced load



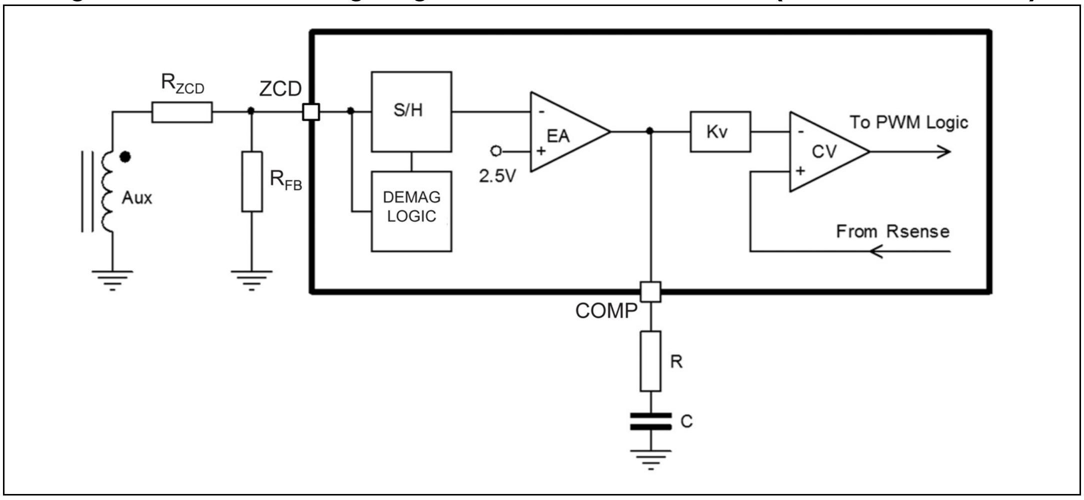
When the system operates in the valley-skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance could fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. This mechanism is natural and there is no appreciable effect on the converter's performances and on its output voltage.

8.5 Constant voltage regulation (OPTOLESS version)

The IC is internally configured to work in the primary side regulation mode: the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode. *Figure 9* shows the internal schematic of the constant voltage regulation circuitry and the external connections.

Due to the parasitic wires resistance, the auxiliary voltage is representative of the output just when the secondary current becomes zero. For this purpose, the signal on the ZCD pin is sampled and held at the end of transformer's demagnetization to get an accurate image of the output voltage and it is compared to the error amplifier internal reference.

Figure 9. Constant voltage regulation: internal schematic (OPTOLESS version)



During the MOSFET's OFF-time the leakage inductance resonates with the total capacitance across the MOSFET drain-source, and a damped oscillation is superimposed on the reflected voltage. The S/H logic is able to discriminate such oscillations from the real transformer's demagnetization.

When the ZCD logic detects the transformer's demagnetization, the sampling process stops, the information is frozen and compared with the error amplifier internal reference.

The internal error amplifier is a transconductance type and delivers an output current proportional to the input voltage unbalance: its output generates the control voltage that is compared to the voltage across the sense resistor, thus modulating the cycle-by-cycle peak drain current.

The COMP pin is used for the frequency compensation: usually, an RC network, which stabilizes the overall voltage control loop, is connected between this pin and ground. Further capacitor between the COMP and GND may be used to set a high frequency pole in the circuit compensation.

The output voltage V_{OUT} can be set by fixing R_{ZCD} and choosing the resistor R_{FB} according to *Equation 1*.

Equation 1

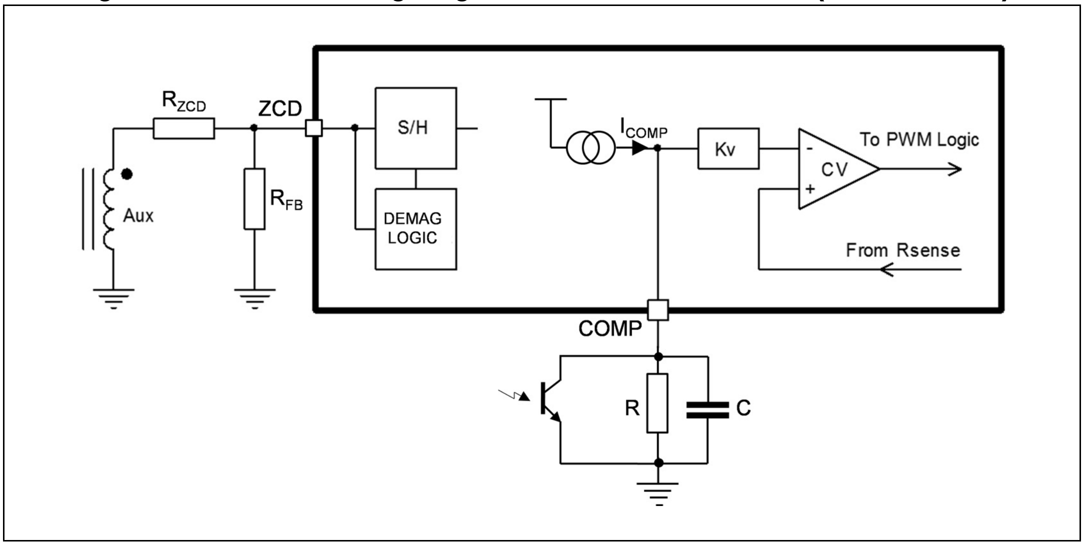
$$R_{FB} = \frac{V_{REF}}{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT} - V_{REF}} \cdot R_{ZCD}$$

where N_{SEC} and N_{AUX} are the secondary and auxiliary turn number respectively. The R_{ZCD} value can be defined depending on the application parameters (see *Section 8.8: Voltage feed-forward block on page 28*).

8.6 Constant voltage regulation (OPTO version)

The IC is internally configured to work in secondary side regulation (the internal transconductance error amplifier is disabled and disconnected from the COMP pin); the output voltage is sensed through a voltage partition across the output capacitor, and the feedback signal obtained at the output of the error amplifier (also located at secondary side), is sent to the primary side through an optocoupler connected to the COMP pin. *Figure 10* shows the internal schematic of the constant voltage regulation circuitry and the external connections for the OPTO version.

Figure 10. Constant voltage regulation: internal schematic (OPTO version)



An internal current generator connected on the COMP pin provides the required feedback current to the optocoupler transistor, allowing to regulate the output voltage.

A resistor and a capacitor between the COMP and GND may be used to set a high frequency pole in the circuit compensation. A further resistor and capacitor series connected and placed between the COMP and GND may be used for adapting the required loop compensation gain and obtaining the proper system dynamic behavior.

The demagnetization logic block, not necessary for voltage regulation, is still necessary for constant current regulation; therefore the external resistive divider (R_{ZCD} - R_{FB}) is still necessary and has to be properly set: for R_{ZCD} selection refer to *Section 8.8: Voltage feed-forward block*, while for R_{FB} selection *Equation 1* is still valid.

8.7 Constant current regulation

Figure 11 presents the basic principle used for controlling the average output current of a flyback converter. The auxiliary winding voltage is used by the demagnetization block to generate the control signal for the switch Q1.

The flip-flop output is high as long as the transformer delivers the current on the secondary side (i.e. during transformer demagnetization). During the time period where the switch Q1 is open, the reference current I_{ref} flows through the external capacitor C_{REF} on the IREF pin; during the ON time of the switch Q1, the resistor R absorbs a current V_C/R, where V_C is the voltage developed across the capacitor C_{REF}. This current balance is shown in *Figure 12*.

Figure 11. Constant current regulation: internal schematic

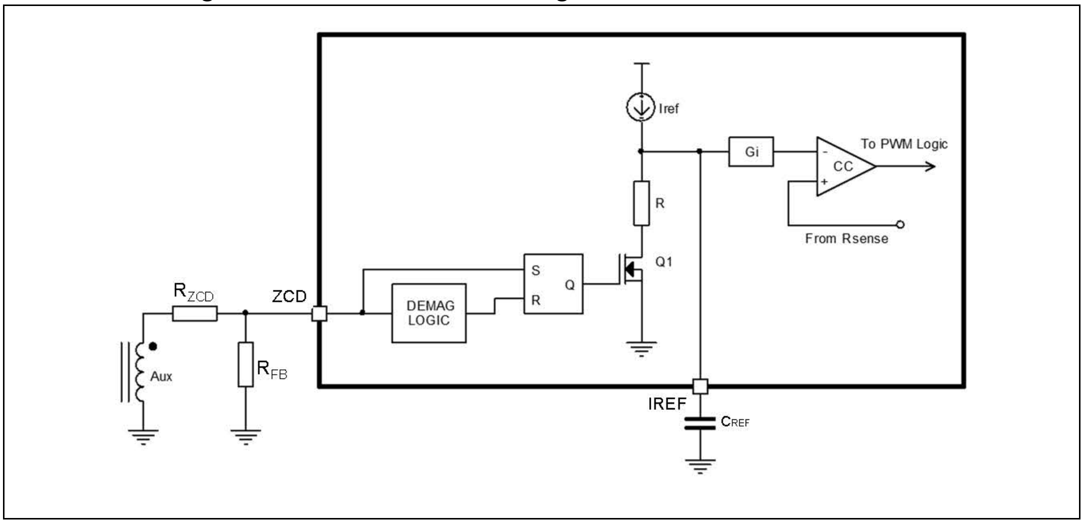
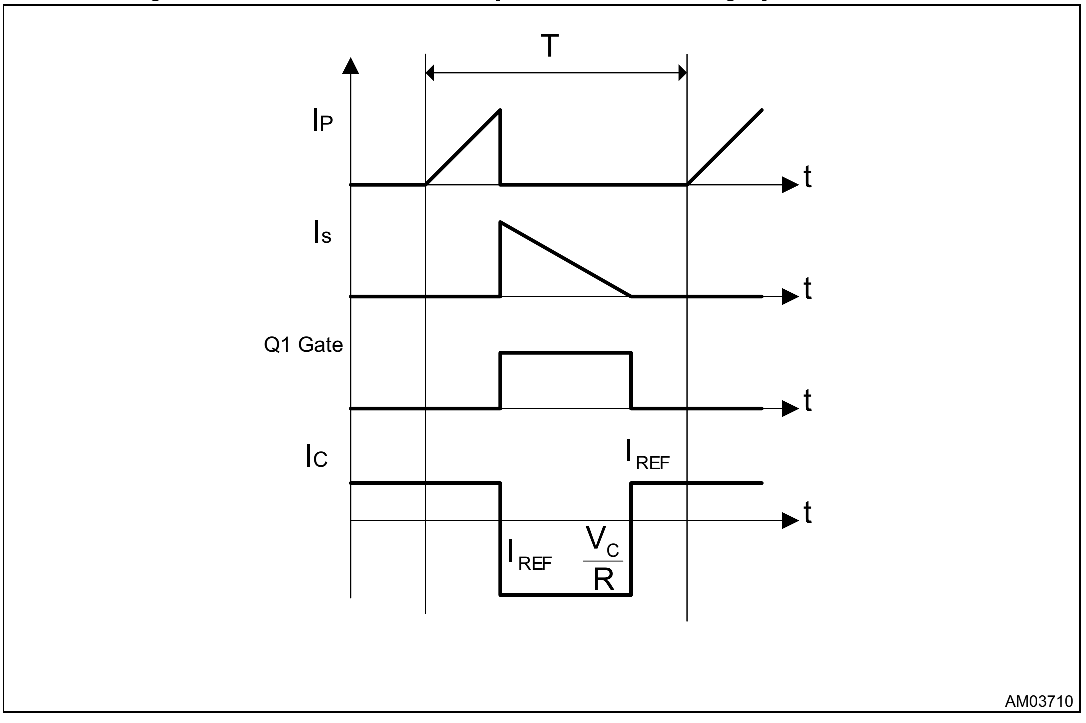


Figure 12. Constant current operation: switching cycle waveforms



The capacitor value has to be chosen so that its voltage V_C can be considered constant. Since it is charged and discharged by currents in the range of some ten µA at the switching frequency rate,
a capacitance value in the range 4.7 - 10 nF is suitable for switching frequencies in the ten kHz.

The average output current can be expressed as:

Equation 2

$$I_{OUT} = \frac{I_S}{2} \cdot \left(\frac{T_{ONSEC}}{T}\right)$$

where I_S is the secondary peak current, T_{ONSEC} is the conduction time of the secondary side and T is the switching period.

Taking into account the transformer ratio $n = N_{PRIM} / N_{SEC}$ between the primary and secondary side,
I_S can also be expressed as a function of the primary peak current I_P:

Equation 3

$$I_S = n \cdot I_P$$

As in steady state the average current I_C through the external capacitor C_{REF} on the IREF pin has to be zero:

Equation 4

$$I_{REF} \cdot (T - T_{ONSEC}) = -\left(I_{REF} - \frac{V_C}{R}\right) \cdot T_{ONSEC}$$

the following expression is found for V_C:

Equation 5

$$V_C = V_{CREF} \cdot \frac{T}{T_{ONSEC}}$$

where $V_{CREF} = R \cdot I_{REF}$. As V_C is fed to the CC comparator, the primary peak current can be expressed as:

Equation 6

$$I_P = \frac{G_I \cdot V_C}{R_{SNS}}$$

Combining *Equation 2*, *Equation 3*, *Equation 5* and *Equation 6*, the expression of the output current is found:

Equation 7

$$I_{OUT} = \frac{n}{2} \cdot \frac{G_I \cdot V_{CREF}}{R_{SNS}}$$

This formula shows that the average output current does not depend anymore on the input or the output voltage, neither on transformer inductance values. The external parameters defining the output current are the transformer ratio n and the sense resistor R_{SNS}.

The current loop gain G_I and current reference voltage V_{CREF} are internally defined. G_I can be trimmed in order to provide an accurate CC set point.

The soft-start feature is automatically implemented by the constant current regulation circuit, as the primary peak current is limited by the voltage on the C_{REF} capacitor.

During the startup, as the output voltage is zero, the IC will start in the CC mode with no high peak current operations. In this way the voltage on the output capacitor will increase slowly and the soft-start feature will be ensured.

Actually the C_{REF} value is not relevant to define the soft-start time, as its duration depends on other circuit parameters, like the transformer ratio, sense resistor, output capacitors and load. The user will define the best appropriate value by experiments.

8.8 Voltage feed-forward block

The current control circuit uses the voltage V_C to define the output current, according to *Equation 7*. Actually, the CC comparator will be affected by an internal propagation delay T_D, which will switch off the MOSFET at a peak current higher than the foreseen value.

This current overshoot is calculated through *Equation 8*:

Equation 8

$$\Delta I_P = \frac{V_{IN} \cdot T_D}{L_P}$$

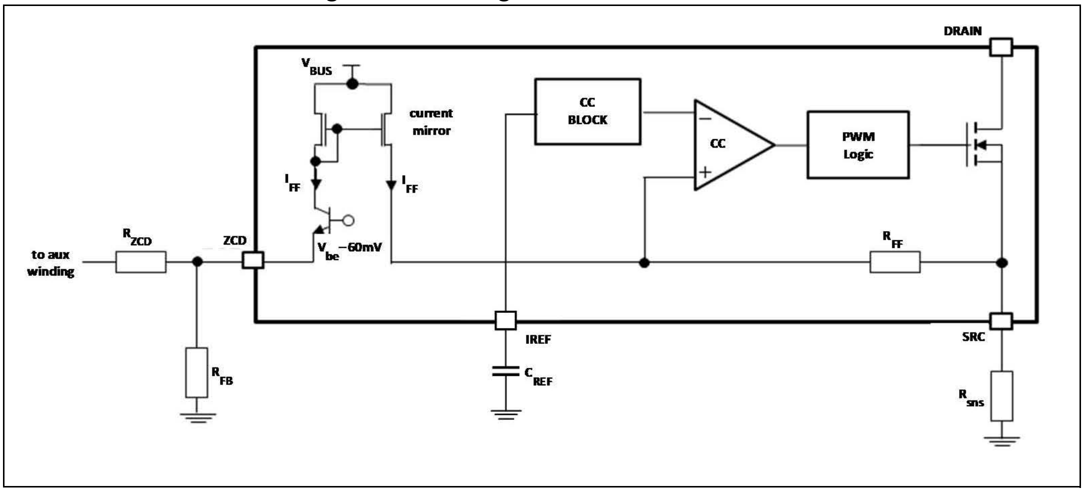
It introduces an error on the calculated CC set point, depending on the input voltage, according to *Equation 9*:

Equation 9

$$I_{OUT\_ERR} = \frac{n \cdot V_{CREF}}{2 \cdot V_C} \cdot \frac{V_{IN} \cdot T_D}{L_P}$$

The device implements a line feed-forward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation. The internal schematic is shown in *Figure 13*.

Figure 13. Voltage feed-forward circuit



During the MOSFET ON-time the current sourced from the ZCD pin is mirrored in order to provide
a feed-forward current I_{FF} proportional to the input voltage according to *Equation 10*:

Equation 10

$$I_{FF} = \frac{V_{IN}}{m \cdot R_{ZCD}}$$

where *m* is the primary-to-auxiliary turns ratio (N_{PRIM} / N_{AUX}). According to the schematic in *Figure 13*, the voltage on the non inverting pin of CC comparator will be:

Equation 11

$$V^{(+)} = R_{SNS} \cdot I_D + (R_{FF} + R_{SNS}) \cdot I_{FF}$$

The offset introduced by the feed-forward compensation will be:

Equation 12

$$V_{OFFSET} = \frac{V_{IN}}{m \cdot R_{ZCD}} \cdot (R_{FF} + R_{SNS})$$

As $R_{FF} >> R_{SNS}$, the previous one can be simplified as:

Equation 13

$$V_{OFFSET} = \frac{V_{IN} \cdot R_{FF}}{m \cdot R_{ZCD}}$$

This offset is proportional to V_{IN} and is used to compensate the current overshoot, according to:

Equation 14

$$\frac{V_{IN} \cdot T_d}{L_P} \cdot R_{SNS} = \frac{V_{IN} \cdot R_{FF}}{m \cdot R_{ZCD}}$$

Finally, the R_{ZCD} resistor can be calculated as follows:

Equation 15

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRIM}} \cdot \frac{L_P \cdot R_{FF}}{T_d \cdot R_{SNS}}$$

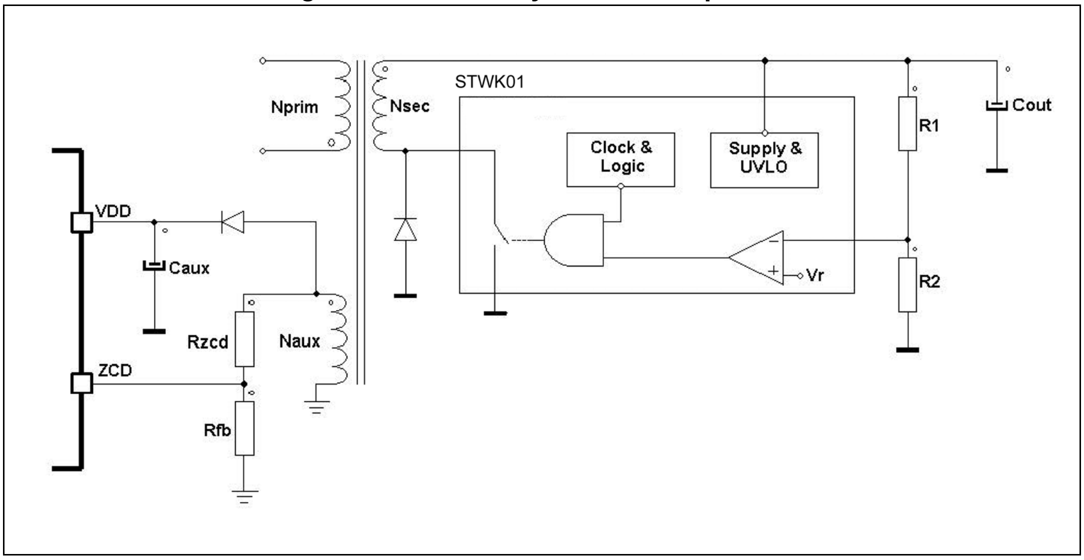
In this case the peak drain current does not depend on input voltage anymore.

One more consideration concerns the R_{ZCD} value: during the MOSFET's ON-time, the current sourced by the ZCD pin, I_{ZCD}, is compared with an internal reference current I_{ZCDON}. If $I_{ZCD} < I_{ZCDON}$, the brownout function is activated and the IC is shut down. This feature is especially important when the auxiliary winding is accidentally disconnected or the ZCD pin is short-circuited to GND ($I_{ZCD} = 0$ that means a feedback loop disconnection occurs) and considerably increases the end product's safety and reliability.

8.9 Burst mode operation (OPTOLESS version)

With decreasing load levels, when the voltage at the COMP pin falls below the threshold V_{COMPBM}, the IC is disabled with the MOSFET kept in OFF state and its consumption reduced at a very low value to minimize V_{DD} capacitor discharge: in this state only few IC blocks are kept alive, dropping the device consumption to few tens µA. The device will resume operation only after a wake-up signal, coming from the secondary side via the transformer, is sensed on the ZCD pin. For this purpose, as shown in *Figure 14*, STWK01at the secondary side senses the output voltage and when it falls below a threshold set by the resistive divider (R1, R2), a switch across the output diode is turned on for a fixed time (about 1 µs), transferring a pulse train from the secondary winding to the auxiliary winding and hence to the ZCD pin. The STWK01 logic enables the check on the output voltage only after it has detected the switching operation stop: this is to avoid wake-up pulses during the switching activity that would cause a short-circuit across the secondary winding of the flyback transformer.

Figure 14. Secondary side wake-up circuit



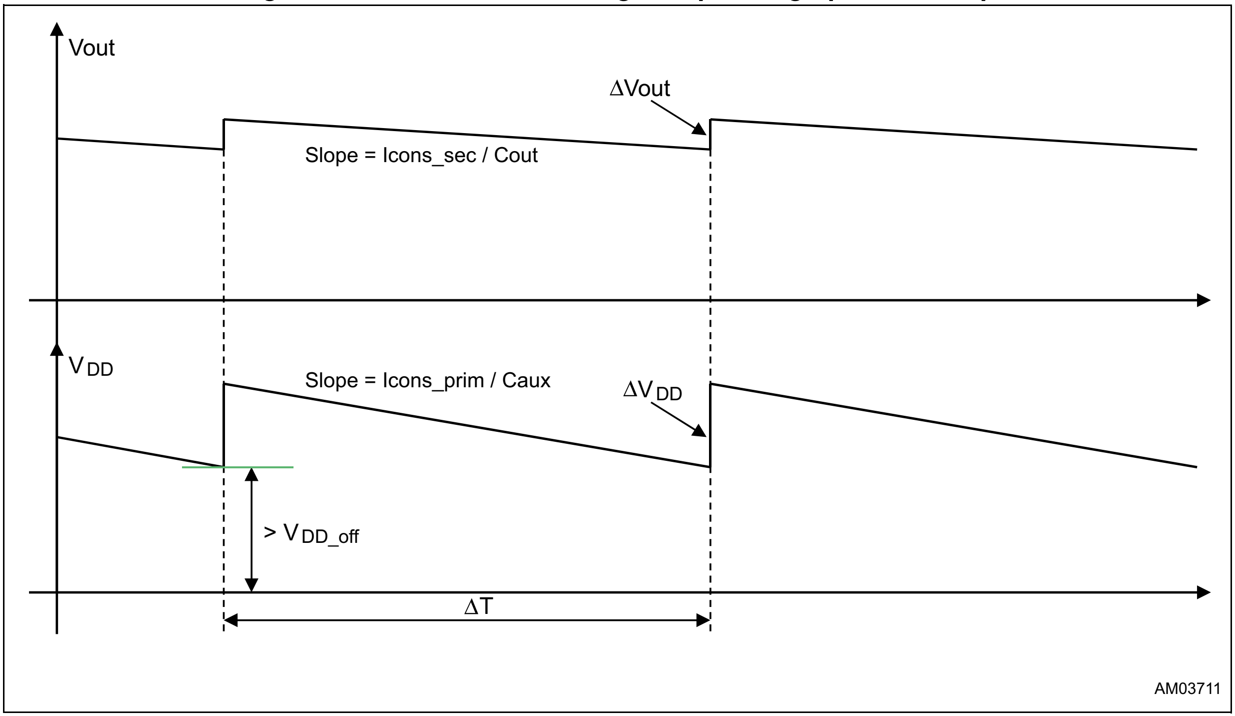
As a result of the energy delivery stop, the output voltage across the capacitor C_{out} and the V_{DD} voltage across the capacitor C_{aux} decreases linearly, due to the consumption of the STWK01 and of the primary device respectively. Referring to the time diagram in *Figure 15* the following relationship can be written:

Equation 16

$$\Delta T = \frac{C_{out}}{I_{cons\_prim}} \cdot \Delta V_{out} = \frac{C_{aux}}{I_{cons\_sec}} \cdot \Delta V_{DD} \qquad => \qquad \Delta V_{DD} = \frac{C_{out}}{C_{aux}} \cdot \frac{I_{cons\_prim}}{I_{cons\_sec}} \cdot \Delta V_{out}$$

where I_{cons_prim} and I_{cons_sec} represent the residual consumption at the primary and secondary side respectively. It is clear from the time diagram that the minimum voltage across the capacitor on the V_{DD} pin has to be greater than the off threshold V_{DD_off} (because the HV start-up generator is not active during the burst mode operation). This V_{DD} supply voltage constraint has to be assured from an application design point of view, by a proper choice of C_{aux} and of the number of turns N_{AUX} of the transformer auxiliary winding.

Figure 15. Vout and VDD voltage drop during operation stop



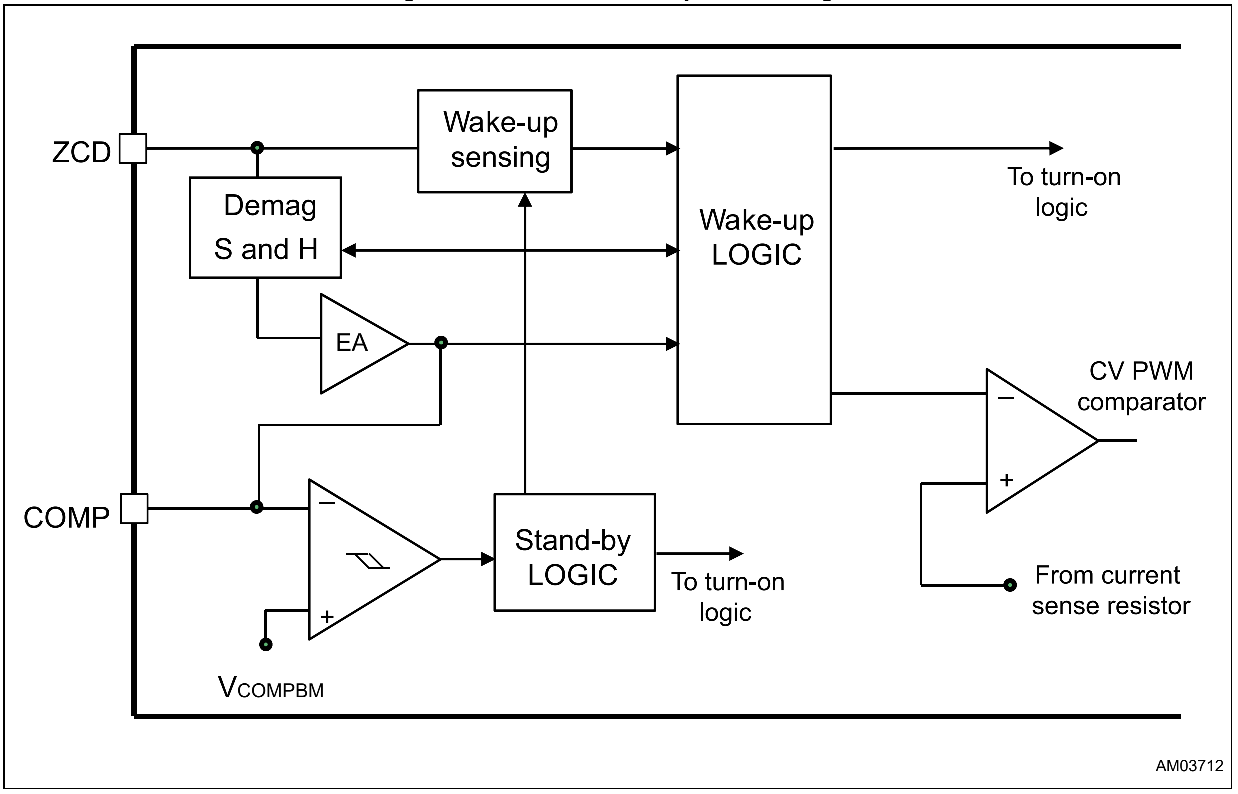
After detecting the wake-up signal on the ZCD pin, all the internal blocks are reactivated; then the primary side controller refreshes the sample and hold voltage (lost during the long stop period), while keeping the COMP in high impedance, and starts delivering low energy pulses at the controlled peak current (progressively increased): this prevents audible noise from the transformer. When the sampled and held voltage is well correlated to the output voltage, the control is passed again to the feedback loop, relying on the COMP voltage information.

After the output capacitor charge has been refreshed, if the load is not changed, the COMP voltage will again decrease below the threshold V_{COMPBM} with a consequent operation stop: in this way the converter will work in the burst mode until the load is increased.

Figure 16 shows a block diagram of the burst mode entering and exiting logic.

The wake-up pulse, in order to be correctly sensed on ZCD pin, needs to have amplitude higher than the wake-up threshold $V_{ZCDwupTH}$ for a period longer than T_{WUP_min}. Because after the last switching cycle before entering burst-mode a ringing takes place on the auxiliary winding of the transformer (and hence on the ZVD pin as well), a false wake-up event could be triggered: to avoid this, a masking time T_{WUP_mask} is inserted (starting from the end of last transformer demagnetization) so that this ringing may fade up below the wake-up threshold $V_{ZCDwupTH}$ within T_{WUP_mask}

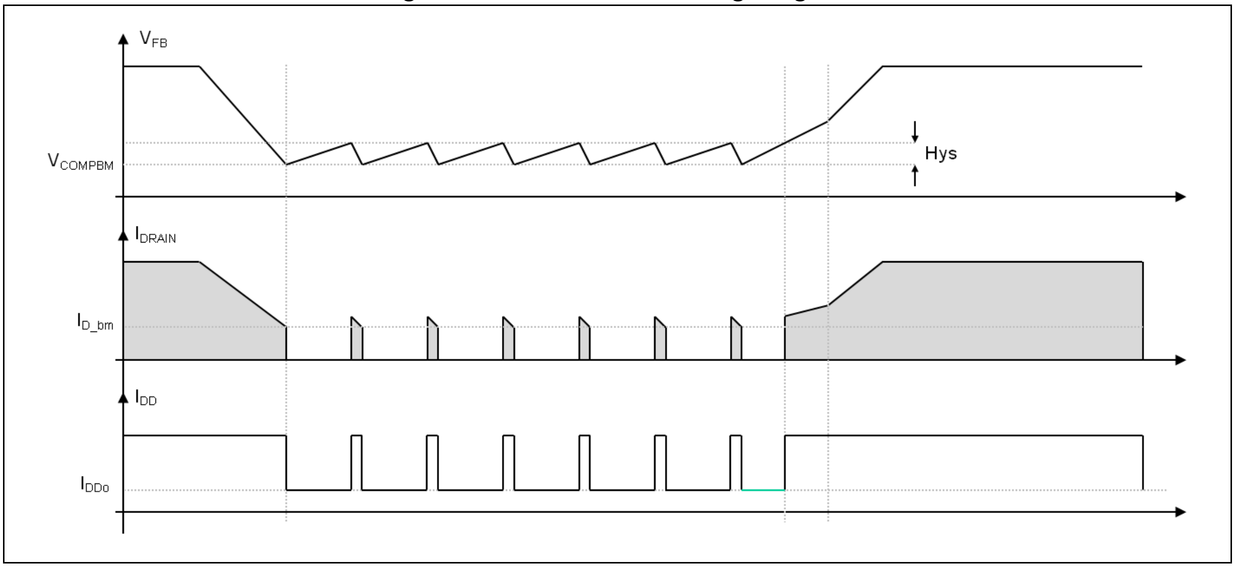
Figure 16. Burst mode operation logic



8.10 Burst mode operation (OPTO version)

When the load decreases, the feedback loop reacts lowering the COMP pin voltage. If it falls below the burst mode threshold, V_{COMPBM}, the controller stops switching. Then, as a result of the feedback reaction to the energy delivery stop, the COMP voltage increases; when it exceeds the level, V_{COMPBM} + Hys, the Power low-side MOSFET starts switching again. The systems alternates period of time where the Power MOSFET is switching to the period of time where the Power MOSFET is not switching (burst mode operation: see *Figure 17*).

Figure 17. Burst mode timing diagram



The power delivered to output during switching periods exceeds the load power demand; the excess of power is balanced from a not switching period, where no power is processed. The advantage of the burst mode operation is an average switching frequency much lower than the normal operation working frequency, up to some hundred of hertz, minimizing all frequency related losses.

8.11 Frequency jitter for EMI reduction

In order to reduce the EMI filtering, a proprietary frequency jitter technique is implemented in the controller, based on the injection of a modulating signal at 11 kHz (above the feedback loop bandwidth) with a 50% duty cycle on the current sense signal: this signal is a square waveform that modulates the amplitude of the peak primary current. The percentage of this amplitude is set as a default at 5% and can be changed with online trimming by the user. As the peak current reduces with decreasing load levels, the effect of this modulation automatically attenuates at lower loads, where the energy of EMI noise is highly reduced.

8.12 OVP function

A dedicated OVP pin allows for overvoltage protection: through a resistive divider sensing the auxiliary winding, a sample of the output voltage is sensed and compared with the internal reference V_{OVP}; in case the threshold is surpassed, a latched protection trip occurs. The sampling of the sensed voltage is operated at the end of transformer demagnetization (contextually to the feedback sensing on ZCD pin), where the sample is a representative value of the output voltage.

By choosing the value of the low-side resistor of OVP divider (R_{OVP_L}), the high-side resistor (R_{OVP_H}) can be calculated as follows:

Equation 17

$$R_{OVP\_H} = \frac{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT\_PROT} - V_{OVP}}{V_{OVP}} \cdot R_{OVP\_L}$$

where V_{OVP} is the internal voltage threshold of the OVP comparator and V_{OUT_PROT} is the output voltage level where the protection will trigger.

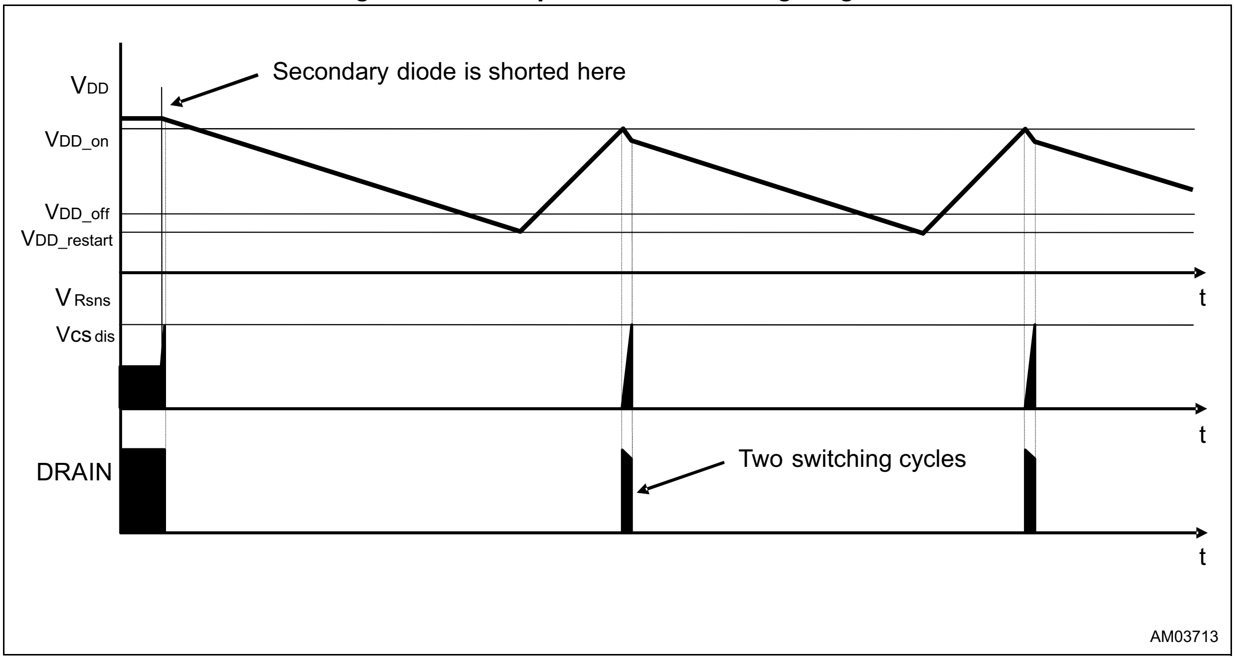
8.13 Hiccup mode OCP

The device is also protected against a short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard saturation of the flyback transformer. A comparator monitors continuously the voltage on the R_{SENSE} and activates a protection circuitry if this voltage exceeds the threshold V_{CSdis}.

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped, the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator will be tripped again a real malfunction is assumed and the device will be stopped.

This condition is latched as long as the device is supplied. While it is disabled, however, no energy is coming from the self-supply circuit; hence the voltage on the V_{DD} capacitor will decay and cross the off threshold V_{DD_off} after some time, which clears the latch. The internal start-up generator is still off, then the V_{DD} voltage still needs to go below its restart threshold $V_{DD\_restart}$ before the capacitor on the V_{DD} pin is charged again and the device restarted (at a reduced charging current I_{DD_CH}). Ultimately, this will result in a low-frequency intermittent operation (hiccup mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 18*.

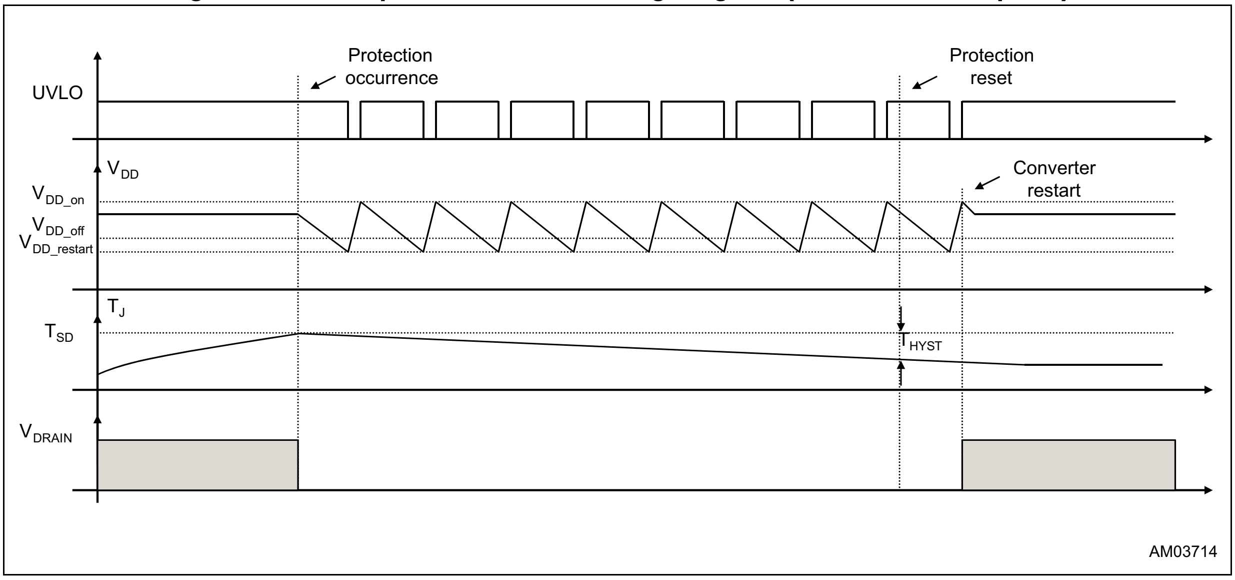
Figure 18. Hiccup mode OCP: timing diagram



8.14 Generic protection pin (PROT)

The PROT pin is the input pin for a user defined protection circuit (for example secondary side OVP or OTP): if the voltage on the pin is kept below the V_{PROT} threshold, the device stops operating. The internal pull-up circuit keeps the pin voltage higher than the threshold without any external component. If the protection function is not used, the PROT pin has to be left open. Thanks to the stable current source capability of the PROT pin, a thermal protection can be realized by simply connecting a NTC thermistor to the pin. This protection can be, according to the selected option, autorestart or latched type.

Figure 19. PROT pin intervention timing diagram (autorestart bit option)



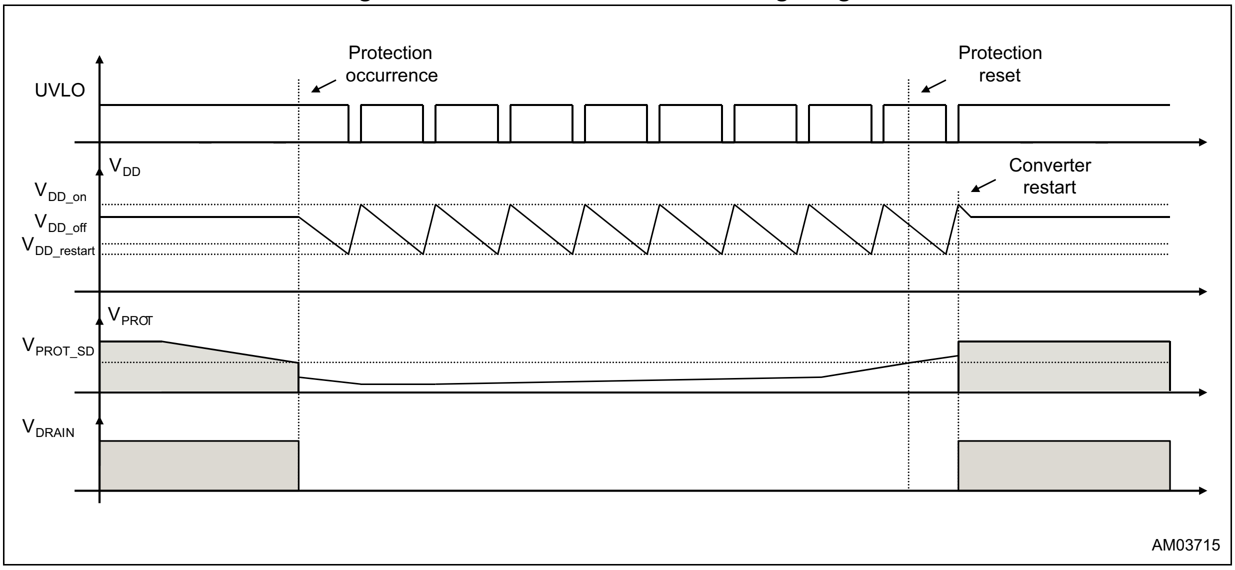
In the case of latch bit option, once the protection trips, a V_{DD} on/off cycle is needed to attempt a new restart. In the autorestart bit option case, after protection trip, when the pin voltage increases above the shutdown threshold, the operation resumes at the first UVLO signal rising edge, as depicted in *Figure 19*.

It is worth pointing out that in the autorestart case, the pin current capability is reduced after protection tripping, confirming in this way the protection occurrence and providing a current hysteresis to the protection logic, for a correct and safe operation.

8.15 Thermal shutdown

The thermal sensor is implemented inside the low-side MOSFET device and senses its junction temperature; when this reaches the shutdown threshold T_{SD} (typ. 150 °C, min. 130 °C), the controller stops the operation, allowing the MOSFET cool down. The operation resumes when the junction temperature decreases of T_{HYST} (typ. 30 °C), at the next positive going edge of the UVLO signal, according to the autorestart procedure (see *Figure 20*).

Figure 20. Thermal shutdown timing diagram



9 Online trimming

9.1 General features

The embedded digital trimming allows the user to adjust and permanently store via software, all the parameters included in *Table 7* during the production test of the end product, compensating the tolerance of the external components and the error due to their discretization values.

Table 7. Adjustable parameter list

Parameter	Description
V_{REF}	Output voltage accuracy setting
$G_I * V_{CREF}$	Output current accuracy setting
R_{FF}	Voltage feed-forward accuracy setting
ΔIpk	Jitter amplitude option

The device provides a non-volatile memory (NVM) based on an OTP (one-time-programmable memory) and a volatile memory.

The volatile memory is used to adjust the value of all the parameters in *Table 7*: once the optimal values have been found the user can permanently store them in the OTP memory.

At device power-on, the parameter values depend on the OTP status:

- If the IC has never been burnt (i.e. no value was permanently stored in OTP memories), the parameters are initialized at default values (refer to *Table 13*, *Table 15*, *Table 17* and *Table 19*.
- If the IC was already burnt (i.e. values stored in the OTP) the parameter values are the ones selected and stored by the user during the trimming process.

The device is provided with an I^2C slave only interface that requires only two pins for the communication: SDA and SCL.

The I^2C interface allows the user to access the device in a simple way, via the I^2C -bus, assuring robust data communication integrity also thanks to an additional parity check control.

Two wires, SDA and SCL, carry information between the devices connected to the I^2C bus.

The device can operate only as I^2C slave, i.e. it needs to be addressed by a master (a micro, industrial PC, ATE, etc.) that initiates a data transfer on the bus and generates the SCL signal to permit that transfer.

Generation of SCL signals on the I^2C bus is always the responsibility of the master.

The device can operate as either a receiver or transmitter (transmitter-slave), depending on the command received from the master.

Serial SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor: the device has an internal pull-up on the pin SDA and SCL in order to pull HIGH the pins when they are floating, but the user has to implement an adequate pull-up of the lines via external pull-up resistors.

When the bus is free, both lines are HIGH.

The data on the SDA line must be stable during the HIGH period of the SCL. The HIGH or LOW state of the SDA line can only change when the SCL signal on the SCL line is LOW.

Within the procedure of the I^2C bus, unique situations arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while the SCL line is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master.

The bus is considered to be busy after the START condition. The bus is considered to be free again
a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.

Every byte put on the SDA line is 8 bits long.

Each byte is followed by an acknowledge bit.

Data is transferred with the most significant bit (MSB) first.

Data transfer with acknowledge is obligatory.

The acknowledge related SCL pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge SCL pulse.

The receiver pulls down the SDA line during the acknowledge SCL pulse so that it remains stable LOW during the HIGH period of this SCL pulse. Of course, setup and hold time must also be taken into account.

When the device is addressed, it generates an acknowledge after the address byte has been received.

When the device doesn't acknowledge the address, the SDA line is left HIGH by the device. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start
a new transfer.

If a device receiver does acknowledge the address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the device generating the not acknowledge on the bytes to follow. The device leaves the SDA line HIGH and the master generates a STOP or a repeated START condition.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the SDA line to allow the master to generate a STOP or repeated START condition.

Data transfers have the following format: after the START condition (S), a slave address is sent. This address is 7 bits long followed by an eight bit which is a data direction bit (R/W) - a “zero” indicates
a transmission (WRITE), a “one” indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master

still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address the slave without first generating a STOP condition.

9.2 Device address

The device is provided with the following fixed 7-bit address (corresponding to < 58 > Hex), while the 8th bit is the data direction (R/W):

Table 8. Device address register

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	0	0	0	1/0

9.3 Device commands

The commands are implemented with one byte word including a bit for a parity check (LSB):

Table 9. Device commands register

MSB							LSB
C7	C6	C5	C4	C3	C2	C1	C0

The parity check on bit ***C0*** has the following structure:

C0 = C7 ⊕ C6 ⊕ C5 ⊕ C4 ⊕ C3 ⊕ C2 ⊕ C1,(⊕ is the XOR operator)

The possible commands are summarized in *Table 10*: if the device receives a command not specified in this table or in case of a parity check failure, no command is executed and a fail flag is internally activated.

Table 10. Command mapping

(*C0* = parity check bit)	**Command code**							
	C7	C6	C5	C4	C3	C2	C1	C0
Emulate/read V_{REF}	0	0	0	1	0	0	1	0
Emulate/read G_I * V_{CREF}	1	1	0	0	0	0	1	1
Emulate/read R_{FF}	1	0	0	1	1	0	1	0
Emulate/read ΔIpk	0	1	0	1	0	0	1	1
Reset Volatile memory to default	1	1	0	1	0	1	1	1
Write NVM	0	1	0	1	0	1	0	1

Data strings

The data are implemented with one byte word including a bit for a parity check (LSB).

Table 11. Data strings register

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

The parity check on bit ***D0*** has the following structure:

D0 = D7 ⊕ D6 ⊕ D5 ⊕ D4 ⊕ D3 ⊕ D2 ⊕ D1,(⊕ is the XOR operator)

In case the parity bit check is not correct the data is not acquired, the parameter value (depending on the command) will be not updated: an internal parity fail flag is activated and it is no possible to execute any command before a read command.

9.4 Emulation commands

It is possible to change all adjustable parameter values writing the volatile memory (in the various parameter registers) before deciding to permanently store the values in the device.

The user is only allowed to toggle default bit value per each bit in each parameter once. Thus after
a toggle 0 → 1 (or 1 → 0) of the generic parameter bit, to revert it to its default value a reset operation is needed as described further ahead.

The change of each parameter is done in independent way.

9.5 Emulate V_{REF}

The emulate V_{REF} command writes data in the volatile V_{REF} instruction: it is a write type command and corresponds to the code reported in *Table 12: Emulate V_{REF} instruction*:

Table 12. Emulate V_{REF} instruction

	Start /stop	byte1 (address, write type)								ack	byte2: command								ack	byte3: write data				ack	Start /stop
Emulate V_{REF}	S	A6	A5	A4	A3	A2	A1	A0	0	0	0	0	0	1	0	0	1	0	0	0	0	V_{REF} 5 data Bits	pck	0	P

x	x	Sent by slave (device)		x	x	x	Sent by master

The value of V_{REF} is changed according to the data sent (see *Table 13*). LSB is the parity check bit.

Table 13. V_{REF} values

Data bits					Trim step [%]	V_{REF} value [V]
D4	D3	D2	D1	D0		
1	0	0	0	0	-9.6%	2.260
1	0	0	0	1	-9.0%	2.275
1	0	0	1	0	-8.4%	2.290
1	0	0	1	1	-7.8%	2.305
1	0	1	0	0	-7.2%	2.320
1	0	1	0	1	-6.6%	2.335
1	0	1	1	0	-6.0%	2.350
1	0	1	1	1	-5.4%	2.365
1	1	0	0	0	-4.8%	2.380
1	1	0	0	1	-4.2%	2.395
1	1	0	1	0	-3.6%	2.410
1	1	0	1	1	-3.0%	2.425
1	1	1	0	0	-2.4%	2.440
1	1	1	0	1	-1.8%	2.455
1	1	1	1	0	-1.2%	2.470
1	1	1	1	1	-0.6%	2.485
0	0	0	0	0	0.0%	2.500 default(1), (2)
0	0	0	0	1	0.6%	2.515
0	0	0	1	0	1.2%	2.530
0	0	0	1	1	1.8%	2.545

Table 13. V_{REF} values (continued)

Data bits					Trim step [%]	V_{REF} value [V]
D4	D3	D2	D1	D0		
0	0	1	0	0	2.4%	2.560
0	0	1	0	1	3.0%	2.575
0	0	1	1	0	3.6%	2.590
0	0	1	1	1	4.2%	2.605
0	1	0	0	0	4.8%	2.620
0	1	0	0	1	5.4%	2.635
0	1	0	1	0	6.0%	2.650
0	1	0	1	1	6.6%	2.665
0	1	1	0	0	7.2%	2.680
0	1	1	0	1	7.8%	2.695
0	1	1	1	0	8.4%	2.710
0	1	1	1	1	9.0%	2.725

1. Please note: the device is initialized with the default value of 00000 (i.e. the 0% trim value for V_{REF}); in case the device is already burnt, the default value is the one stored in the OTP.
2. Please note: The 0% trim value was assumed 2.5 V as an example but this value can be in the range [2.48 V, 2.52 V]. The trimming range is proportional to the trimming value [-9.6%, + 9%] with a trimming step of 0.6% referred to the 0% trim value.

In case of a parity check fail (command or data) the command is not executed (V_{REF} register doesn't change) and an internal *parity fail flag* is activated: if the parity *fail flag* is activated from the previous communication, the command is not executed even if the parity check is OK; the *parity fail flag* is reset by the first read command.

If the parity check is OK, the V_{REF} is changed accordantly to the V_{REF} register content with a direct change from the old to the new value.

9.6 Emulate G_I * V_{CREF}

The emulate G_I * V_{CREF} command writes data in the volatile G_I * V_{CREF} instruction: it is a write type command and corresponds to the code reported in *Table 14: Emulate GI * VCREF instruction*.

Table 14. Emulate G_I * V_{CREF} instruction

	Start/stop	byte1 (address, write type)								ack	byte2: command								ack	byte3: write data					ack	Start/stop
Emulate G_I * V_{CREF}	S	A6	A5	A4	A3	A2	A1	A0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	G_I * VC_{REF}4 data bits	pck	0	P

x	x	Sent by slave (device)	x	x	x	Sent by master	

The value of G_I * V_{CREF} is changed according to the data sent (see *Table 15*). LSB is the parity check bit.

Table 15. G_I * V_{CREF} values

Data bits				Trim step [%]	G_I * V_{CREF} value [mV]
D3	D2	D1	D0		
1	0	0	0	-12.0%	0.176
1	0	0	1	-10.5%	0.179
1	0	1	0	-9.0%	0.182
1	0	1	1	-7.5%	0.185
1	1	0	0	-6.0%	0.188
1	1	0	1	-4.5%	0.191
1	1	1	0	-3.0%	0.194
1	1	1	1	-1.5%	0.197
0	0	0	0	0.0%	0.200 default[1], [2]
0	0	0	1	1.5%	0.203
0	0	1	0	3.0%	0.206
0	0	1	1	4.5%	0.209
0	1	0	0	6.0%	0.212
0	1	0	1	7.5%	0.215

Table 15. $G_I * V_{CREF}$ values (continued)

Data bits				Trim step [%]	$G_I * V_{CREF}$ value [mV]
D3	D2	D1	D0		
0	1	1	0	9.0%	0.218
0	1	1	1	10.5%	0.221

1. Please note: the device is initialized with the default value of 0000 (i.e. 0% trim value of $G_I * V_{CREF}$); in case the device is already burnt, the default value is the one stored in the OTP.
2. Please note: The 0% trim value was assumed 0.2 V as an example but this value can be in the range [0.19 V, 0.21 V]. The trimming range is proportional to the trimming value [-12% ; +10.5%] with a trimming step of 1.5% referred to the 0% trim value.

In case of a parity check fail (command or data) the command is not executed ($G_I * V_{CREF}$ register doesn't change) and an internal *parity fail flag* is activated: if the *parity fail flag* is activated from the previous communication, the command is not executed even if the parity check is OK; the *parity fail flag* is reset by the first read command.

If a parity check is OK, the $G_I * V_{CREF}$ is changed accordantly to the $G_I * V_{CREF}$ register content with a direct change from the old to the new value.

9.7 Emulate R_{FF}

The emulate R_{FF} command writes data in the volatile R_{FF} instruction: it is a write type command and corresponds to the code reported in *Table 16*.

Table 16. Emulate R_{FF} instruction

	Start/stop	byte1 (address, write type)								ack	byte2: command								ack	byte3: write data					ack	Start/stop
Emulate R_{FF}	S	A6	A5	A4	A3	A2	A1	A0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	R_{FF}4 data Bits	pck	0	P

x	x	Sent by slave (device)	x	x	x	Sent by master

The value of R_{FF} is changed according to the data sent (see*Table 17*). LSB is the parity check bit.

Table 17. R_{FF} values

Data bits				Trim step [%]	R_{FF} value [Ω]
D3	D2	D1	D0		
1	0	0	0	-20%	48.00
1	0	0	1	-17.5%	49.50
1	0	1	0	-15%	51.00
1	0	1	1	-12.5%	52.50
1	1	0	0	-10%	54.00
1	1	0	1	-7.5%	55.50
1	1	1	0	-5%	57.00
1	1	1	1	-2.5%	58.50
0	0	0	0	0%	60.00 default(1)(2)
0	0	0	1	2.5%	61.50
0	0	1	0	5%	63.00
0	0	1	1	7.5%	64.50
0	1	0	0	10%	66.00
0	1	0	1	12.5%	67.50

Table 17. R_{FF} values (continued)

Data bits				Trim step [%]	R_{FF} value [Ω]
D3	D2	D1	D0		
0	1	1	0	15%	69.00
0	1	1	1	17.5%	70.50

1. Please note: the device is initialized with the default value of 0000 (i.e. 0% trim value of R_{FF}); in case the device is already burnt, the default value is the one stored in the OTP.
2. Please note: The 0% trim value was assumed 25 Ω as an example but this value can be in the range [54 Ω, 66 Ω]. The trimming range is proportional to the trimming value [-20% +17.5%] with a trimming step of 2.5% referred to the 0% trim value.

In case of a parity check fail (command or data) the command is not executed (R_{FF} register doesn't change) and an internal *parity fail flag* is activated: if the *parity fail flag* is activated from the previous communication, the command is not executed even if the parity check is OK; the *parity fail flag* is reset by the first read command.

If the parity check is OK, the R_{FF} is changed accordantly to the R_{FF} register content with a direct change from the old to the new value.

9.8 Emulate ΔIpk

The emulate ΔIpk command writes data in the volatile ΔIpk instruction: it is a write type command and corresponds to the code reported in *Table 18*.

Table 18. Emulate ΔIpk instruction

	Start/stop	byte1 (address, write type)								ack	byte2: command								ack	byte3: write data						ack	Start/stop
Emulate ΔIpk	S	A6	A5	A4	A3	A2	A1	A0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0	ΔIpk3 data Bits	pck	0	P

	x	x	Sent by slave (device)		x	x	x	Sent by master	

The value of ΔIpk is changed according to the data sent (see *Table 19*). LSB is the parity check bit.

Table 19. ΔIpk values

Data bits			ΔIpk% value
D2	**D1**	**D0**	
0	1	1	0% (no jitter)
0	1	0	3%
0	0	1	4%
0	0	0	5% default(1)
1	1	1	6.5%
1	1	0	8%
1	0	1	10%
1	0	0	12%

1. Please note: the device is initialized with the default value of 000 (i.e. 5% trim value of ΔIpk); in case the device is already burnt, the default value is the one stored in the OTP.

In case of a parity check fail (command or data) the command is not executed (*ΔIpk register* doesn't change) and an internal *parity fail flag* is activated: if the *parity fail flag* is activated from the previous communication, the command is not executed even if the parity check is OK; the *parity fail flag* is reset by the first read command.

If the parity check is OK, the ΔIpk is changed accordantly to the *ΔIpk register* content with a direct change from the old to the new value.

9.9 Read commands

It is possible to read the content of the volatile memory and also the status of the NVM memory that indicates if the NVM is virgin or burnt, or if an error occurred during the trimming process (*status register*) (see *Table 20*).

Table 20. Status register

Status register	Description	Value
M1	NVM write residual possibility	0 OTP not yet programmed 1 OTP programmed
M0	Parity fail flag	0 parity success 1 parity failed

The reading command of the volatile memory can be used to check the value written in the volatile memory before to permanently store it, increasing the robustness of trimming process; as described in *Section 9.4: Emulation commands on page 40*, the reading of the non-volatile memory is necessary to reset the internal parity fail flag eventually activated by a communication error during the trimming process.

9.9.1 Read V_{REF}

The command *read* V_{REF} command reads data of the volatile *V_{REF} register* and the OTP *status register*: it is a write/read type command and corresponds to the code reported in *Table 21*.

Once the device receives the command *emulate/read V_{REF}*, in order to perform a reading it is necessary to send a repeated start (Sr) and address as read type, i.e. with the LSB (R/W) set at "one"; the device will send on the SDA line an 8-bit word, where the first two bits are the status register bit M1 and M0 and the following 6 bits are the value of V_{REF} with a parity check as LSB.

Table 21. Read V_{REF} instruction

	Start/stop	byte1 (address, write type)								ack	byte2: command								ack	Start/stop	byte3 (address, read type)								ack	byte 4: read data				Nack	Start/stop
Read V_{REF}	S	A6	A5	A4	A3	A2	A1	A0	0	0	0	0	0	1	0	0	1	0	0	Sr	A6	A5	A4	A3	A2	A1	A0	1	0	M1	M0	V_{REF} 5 data Bits	pck	1	P
	x	x	Sent by slave (device)		x	x	x	Sent by master																											

In case of a communication error the content of the *status register* is <11>, and it means that the internal *parity flag fail* is activated: after a reading command is executed, the *parity flag fail* is reset and a new command can be executed by the device.

9.9.2 Read G_I * V_{CREF}

The command *read* G_I * V_{CREF} command reads data of the volatile G_I * V_{CREF} *register* and the OTP *status register*: it is a write/read type command and corresponds to the code reported in *Table 22*.

Once the device receives the command *emulate/read* G_I * V_{CREF}, in order to perform a reading it is necessary to send a repeated start (Sr) and address as read type, i.e. with the LSB (R/W) set at "one"; the device will send on the SDA line an 8-bit word, where the first two bits are the status register bit M1 and M0 and the following 6 bits are the value of V_{REF} with a parity check as LSB.

Table 22. Read G_I * V_{CREF} instruction

	Start/stop	byte1 (address, write type)	ack	byte2: command	ack	Start/stop	byte3 (address, read type)	ack	byte 4: read data	Nack	Start/stop
Read G_I * V_{CREF}	S	A6 A5 A4 A3 A2 A1 A0	0	0 1 1 0 0 0 0 1 1	0	Sr	A6 A5 A4 A3 A2 A1 A0 1	0	M1 M0 0 G_I * V_{CREF} 4 data bits pck	1	P

x x Sent by slave (device) x x x Sent by master

In case of a communication error the content of the *status register* is <11>, and it means that the internal *parity flag fail* is activated: after a reading command is executed, the *parity flag fail* is reset and a new command can be executed by the device.

9.9.3 Read R_{FF}

The command *read* R_{FF} command reads data of the volatile R_{FF} *register* and the OTP *status register*: it is a write/read type command and corresponds to the code reported in *Table 23*.

Once the device receives the command *emulate/read* R_{FF}, in order to perform a reading it is necessary to send a repeated start (Sr) and address as read type, i.e. with the LSB (R/W) set at “one”; the device will send on the SDA line bus an 8-bit word, where the first two bits are the status register bit M1 and M0 and the following 6 bits are the value of R_{FF} with a parity check as LSB.

Table 23. Read R_{FF} instruction

	Start/stop	byte1 (address, write type)							ack	byte2: command									ack	Start/stop	byte3 (address, read type)								ack	byte 4: read data					Nack	Start/stop
Read R_{FF}	S	A6	A5	A4	A3	A2	A1	A0	0	0	1	0	0	1	1	0	1	0	0	Sr	A6	A5	A4	A3	A2	A1	A0	1	0	M1	M0	0	R_{FF}4 data bits	pck	1	P
	x	x	Sent by slave (device)					x	x	x	Sent by master																									

In case of a communication error the content of the *status register* is <11>, and it means that the internal *parity flag fail* is activated: after a reading command is executed, the *parity flag fail* is reset and a new command can be executed by the device.

9.9.4 Read ΔIpk

The command *read* ΔIpk command reads data of the volatile ΔIpk *register* and the OTP *status register*: it is a write/read type command and corresponds to the code reported in *Table 24*.

Once the device receives the command *emulate/read* ΔIpk, in order to perform a reading it is necessary to send a repeated start (Sr) and address as read type, i.e. with the LSB (R/W) set at “one”; the device will send on the SDA line bus an 8-bit word, where the first two bits are the status register bit M1 and M0 and the following 6 bits are the value of ΔIpk with a parity check as LSB.

Table 24. Read ΔIpk instruction

<table>
<tr><th></th><th>Start/stop</th><th colspan="8">byte1 (address, write type)</th><th>ack</th><th colspan="8">byte2: command</th><th>ack</th><th>Start/stop</th><th colspan="8">byte3 (address, read type)</th><th>ack</th><th colspan="6">byte 4: read data</th><th>Nack</th><th>Start/stop</th></tr>
<tr><td>Read ΔIpk</td><td>S</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Sr</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>1</td><td>0</td><td>M1</td><td>M0</td><td>0</td><td>0</td><td>ΔIpk 3 data Bits</td><td>pck</td><td>1</td><td>P</td></tr>
</table>

	x	x	Sent by slave (device)		x	x	x	Sent by master	

In case of a communication error the content of the *status register* is <11>, and it means that the internal *parity flag fail* is activated: after a reading command is executed, the *parity flag fail* is reset and a new command can be executed by the device.

9.10 Reset command

It is possible to reset all adjustable parameter values written in the volatile memory (in the various parameter registers).

The reset command acts on all parameters simultaneously.

9.11 Reset volatile memory

The reset volatile memory command resets data in the volatile *registers*: it is a write type command and corresponds to the code reported in*Table 25*:

Table 25. Reset volatile memory instruction

	Start/ stop	byte1 (address, write type)								ack	byte2: command								ack	Start/ stop
Emulate V_{REF}	S	A6	A5	A4	A3	A2	A1	A0	0	0	1	1	0	1	0	1	1	1	0	P
	x	x	Sent by slave (device)					x	x	x	Sent by master									

9.12 Write NVM (OTP)

After the various parameters have been trimmed to the desired level, the user can confirm their values and store them permanently.

This is a virtually real-time trim-and-test without switching off the supply. It is important that during all the process the supply voltage of the IC never falls below its UVLO level, otherwise, the settings stored in the volatile memory will be lost and the IC comes back to the default setting; it is also necessary that the burnt instruction is executed with a V_{DD} = 19 V with a current capability of 90 mA.

In case that the research of the best parameter value is done with a V_{DD} value lower than 19 V, the user has to pay attention that during the step-up of V_{DD} before the burning of the NVM a negative ringing on V_{DD} will cause a drop below the UVLO of the IC.

The user can eventually decide to perform the research of the best parameter value, store these values in an external memory (ATE, industrial PC, etc.), then increase the V_{DD} to 19 V wait to have a stable V_{DD} level and send again the selected parameter values stored in the external memory before to send the burn NVM command.

All the values written in the various parameter registers (volatile memory) are permanently stored into the NVM (OTP) in a single step.

Sending the burnt command reported (write type) in *Table 26* followed a data byte with the same codification of burn command, it is possible burn the NVM.

Table 26. Write NVM (OTP) instruction

	Start/stop	byte1 (address, write type)								ack	byte2: command								ack	byte3 (data)								ack	Start/stop
Write NVM	S	A6	A5	A4	A3	A2	A1	A0	0	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	P
	x	x	Sent by slave (device)					x	x	x	Sent by master																		

It is important to provide a zapping time of at least 45 msec and to have the V_{DD} = 19 V of the IC, with a current capability of 90 mA, in order to ensure a correct blowing of the antifuse cells.

To protect the NVM memory from wrong writing, if the *parity fail flag* is activated, i.e. an error occurred during the trimming process, the burn command is not executed.

After the stop (P) the device doesn't acknowledge any I^2C communication for about 45 ms in order to perform the burning of the NVM.

Please note that after a write NVM command the status register is not automatically updated. It must be updated by turning off and on again the IC. Once the update is performed, the I^2C bus is no more available.

9.13 Multiplexed SCL and SDA inputs

The SCL and SDA inputs are multiplexed with OVP and PROT functionalities respectively; for this reason, before the online trimming procedure, the OVP and PROT functions are not active; only after the online trimming procedure, when all internal parameters have been fixed and stored in the non-volatile-memory, the OVP and PROT functions are activated.

After the online trimming process is over, further access through the I^2C bus is not any longer allowed and consequently the internal non-volatile-memory cannot be accessible for reading.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 21. SO16N package outline

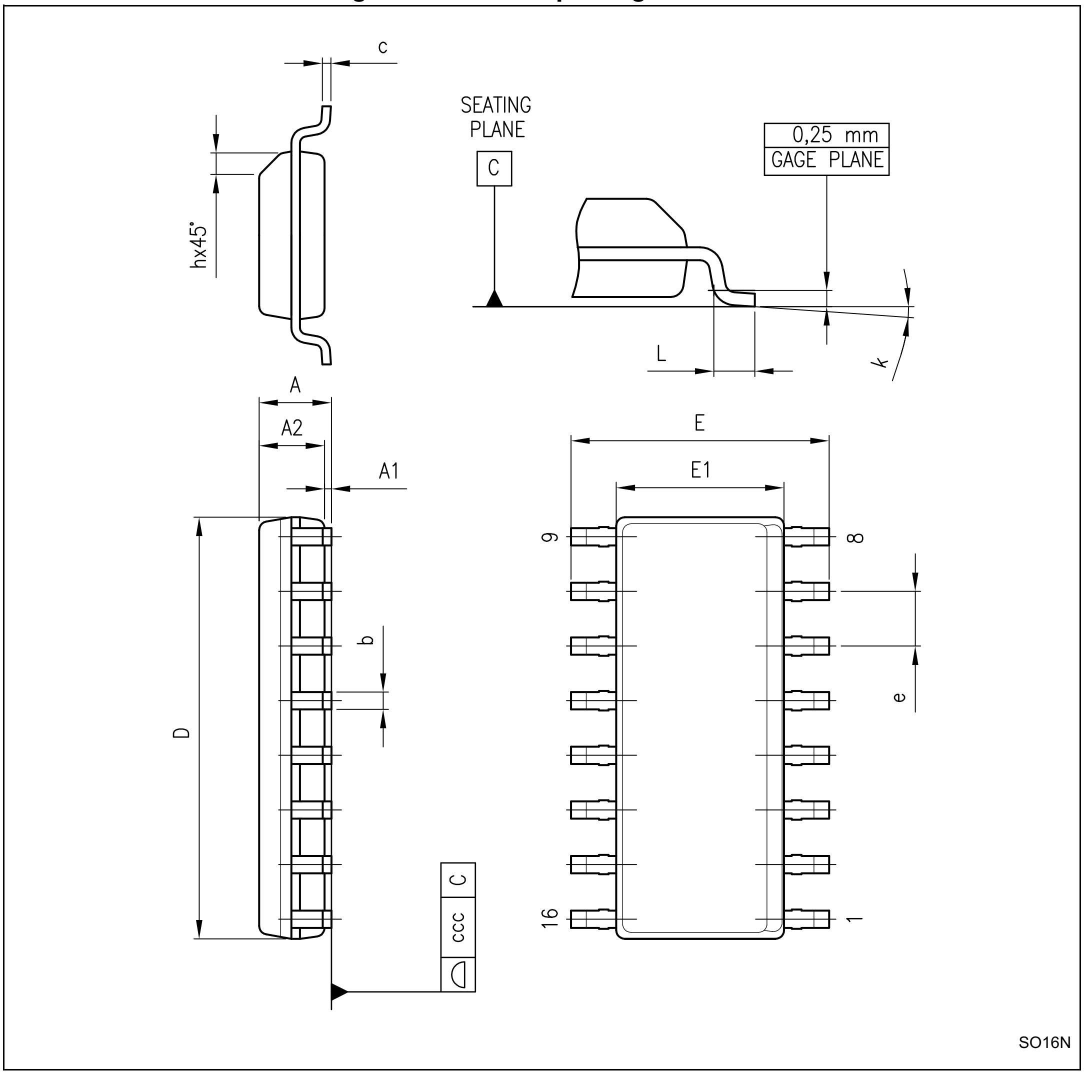


Table 27. SO16N package mechanical data

Symbol	Dimensions (mm)			
	Min.	Typ.	Max.	Notes
A	1.75			
A1	0.10		0.25	
A2	1.25			
b	0.31		0.51	
c	0.17		0.25	
D	9.80	9.90	10.00	(1), (2)
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	(3), (2)
e		1.27		
h	0.25		0.50	
L	0.40		1.27	
k	0		8	Degrees
ccc			0.10	

1. Dimension “D” does not include mold Flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. Dimensions referred to the bottom side of the package.
3. Dimension “E1” does not include interlead Flash or protrusions. Interlead Flash or protrusions shall not exceed 0.25 mm per side.

11 Revision history

Table 28. Document revision history

Date	Revision	Changes
06-Aug-2014	1	Initial release.
08-Aug-2014	2	Updated title, features and description in cover page. Updated *Table 1: Device summary*. Inserted *Table 3: Typical power*. Minor text changes.