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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

μPD78F9232CS, 78F9234CS

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD78F9232CS, 78F9234CS are 8-bit single-chip microcontrollers of the 78K0S microcontrollers. These microcontrollers feature Single-voltage Self-programming Flash memory and many peripherals.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

78K0S/KB1+ User's Manual: U17446E
78K/0S Series Instruction User's Manual: U11047E

FEATURES

- Minimum instruction execution time selectable from high speed (0.2 μs) to low speed (3.2 μs) (with CPU clock of 10 MHz)
- General-purpose registers: 8 bits × 8 registers
- ROM and RAM capacities

Item / Part number	Program Memory (Flash Memory)	Memory (Internal High-Speed RAM)
μPD78F9232CS	4 KB	256 bytes
μPD78F9234CS	8 KB	

- On-chip power-on clear (POC) circuit and low voltage detector (LVI)
- On-chip watchdog timer (operable on internal low-speed internal oscillator clock)
- I/O ports: 26
- Timer: 4 channels
  - 16-bit timer/event counter: 1 channel
  - 8-bit timer: 2 channels
  - Watchdog timer: 1 channel
- Serial interface: UART (LIN (Local Interconnect Network) bus supported) 1 channel
- Multiplier: 8 bits × 8 bits = 16 bits
- 10-bit resolution A/D converter: 4 channels
- Supply voltage: V_{DD} = 2.0 to 5.5 V[Note]
- Operating temperature range: T_A = −40 to +85°C

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

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APPLICATIONS

Household appliances, toys, and industrial equipment

ORDERING INFORMATION

Part Number	Package
μPD78F9232CS-CAA-A	32-pin plastic SDIP (7.62 mm (300))
μPD78F9234CS-CAA-A	32-pin plastic SDIP (7.62 mm (300))

Remark Products with -A at the end of the part number are lead-free products.

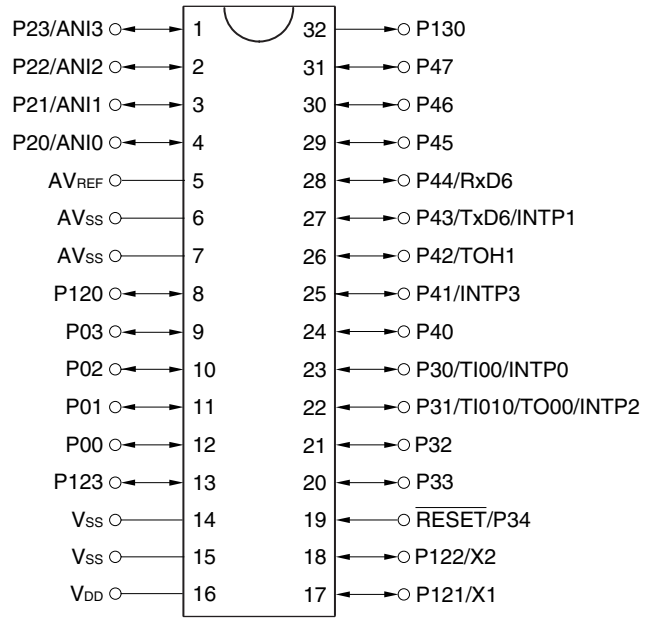
OVERVIEW OF FUNCTIONS

Item		μPD78F9232CS	μPD78F9234CS
Internal memory	Flash memory	4 KB	8 KB
	High-speed RAM	256 bytes	
Memory space		64 KB	
X1 input clock (oscillation frequency)		Crystal/ceramic/external clock input: 10 MHz (V_{DD} = 2.0 to 5.5 V)	
Internal oscillation clock	High speed (oscillation frequency)	Internal oscillation: 8 MHz (TYP.)	
	Low speed (for TMH1 and WDT)	Internal oscillation: 240 kHz (TYP.)	
General-purpose registers		8 bits × 8 registers	
Instruction execution time		0.2 μs/0.4 μs/0.8 μs/1.6 μs/3.2 μs (X1 input clock: f_X = 10 MHz)	
Multiplier		8 bits × 8 bits = 16 bits	
I/O port		Total: 26 pins CMOS I/O: 24 pins CMOS input: 1 pin CMOS output: 1 pin	
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer (timer H1): 1 channel • 8-bit timer (timer 80): 1 channel • Watchdog timer: 1 channel	
	Timer output	2 pins (PWM: 1 pin)	
A/D converter		10-bit resolution × 4 channels	
Serial interface		LIN-bus-supporting UART mode: 1 channel	
Vectored interrupt sources	External	4	
	Internal	9	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on clear • Internal reset by low-voltage detector	
Supply voltage		V_{DD} = 2.0 to 5.5 V[Note]	
Operating temperature range		T_A = −40 to +85°C	
Package		32-pin plastic SDIP	

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on- clear (POC) circuit is 2.1 V ±0.1 V.

PIN CONFIGURATION (Top View)

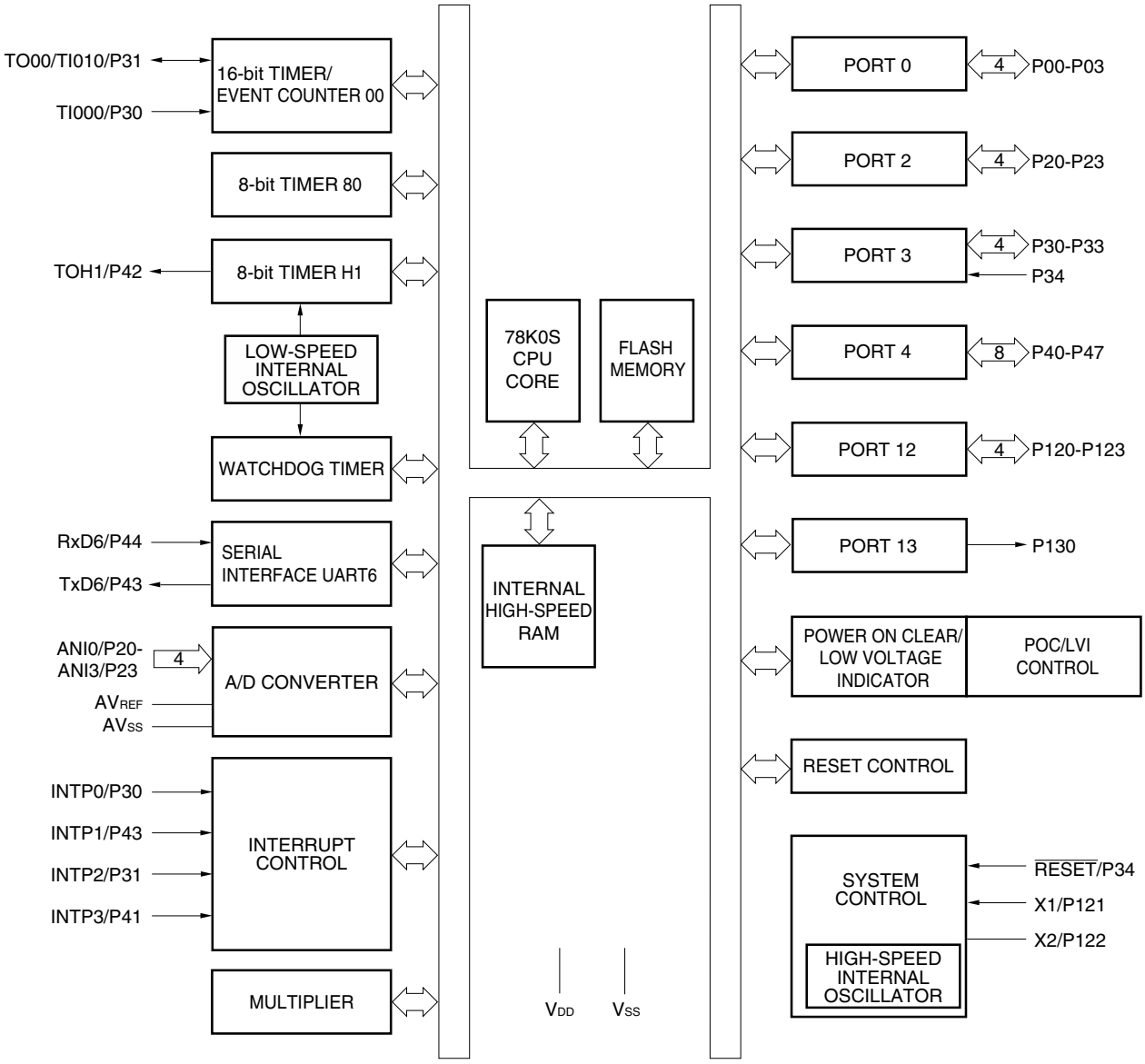
- **32-pin plastic SDIP**



Caution Connect the AVSS pin to VSS.

ANI0 to ANI3:	Analog input	P130:	Port 13
AVREF:	Analog reference voltage	RESET:	Reset
AVSS:	Analog ground	RxD6:	Receive data
INTP0 to INTP3:	External interrupt input	TI000, TI010:	Timer input
P00 to P03:	Port 0	TO00, TOH1:	Timer output
P20 to P23:	Port 2	TxD6:	Transmit data
P30 to P34:	Port 3	VDD:	Power supply
P40 to P47:	Port 4	VSS:	Ground
P120 to P123:	Port 12	X1, X2:	Crystal oscillator (X1 input clock)

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 Port Functions

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P00 to P03	I/O	Port 0. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–
P20 to P23	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	ANI0 to ANI3
P30	I/O	Port 3	Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.	Input	TI000/INTP0
P31					TI010/TO00/INTP2
P32					–
P33					–
P34	Input		Input only	Input	$\overline{\text{RESET}}$
P40	I/O	Port 4. 8-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–
P41					INTP3
P42					TOH1
P43					TxD6/INTP1
P44					RxD6
P45					–
P46					–
P47					–
P120	I/O	Port 12. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected only to P120 and P123 by setting software.		Input	–
P121					X1
P122					X2
P123					–
P130	Output	Port 13. 1-bit output-only port		Output	–

Caution The P121/X1 and P122/X2 pins are pulled down during reset.

1.2 Non-port Functions

Pin Name	I/O	Function	After Reset	Alternate-Function Pin
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI000
INTP1				P43/TxD6
INTP2				P31/TI010/TO00
INTP3				P41
RxD6	Input	Serial data input for asynchronous serial interface	Input	P44
TxD6	Output	Serial data output for asynchronous serial interface	Input	P43/INTP1
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture registers (CR000 and CR010) of 16-bit timer/event counter 00	Input	P30/INTP0
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P31/TO00/INTP2
TO00	Output	16-bit timer/event counter 00 output	Input	P31/TI010/INTP2
TOH1	Output	8-bit timer H1 output	Input	P42
ANI0 to ANI3	Input	Analog input of A/D converter	Input	P20 to P23
AV_{REF}	–	Reference voltage of A/D converter	–	–
AV_{SS}	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–
$\overline{RESET}$	Input	System reset input	–	P34
X1	Input	Connection of crystal/ceramic resonator for system clock oscillation. External clock input	–	P121
X2	–	Connection of crystal/ceramic resonator for system clock oscillation.	–	P122
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–

Caution The P121/X1 and P122/X2 pins are pulled down during reset.

1.3 Pin I/O Circuits and Connection of Unused Pins

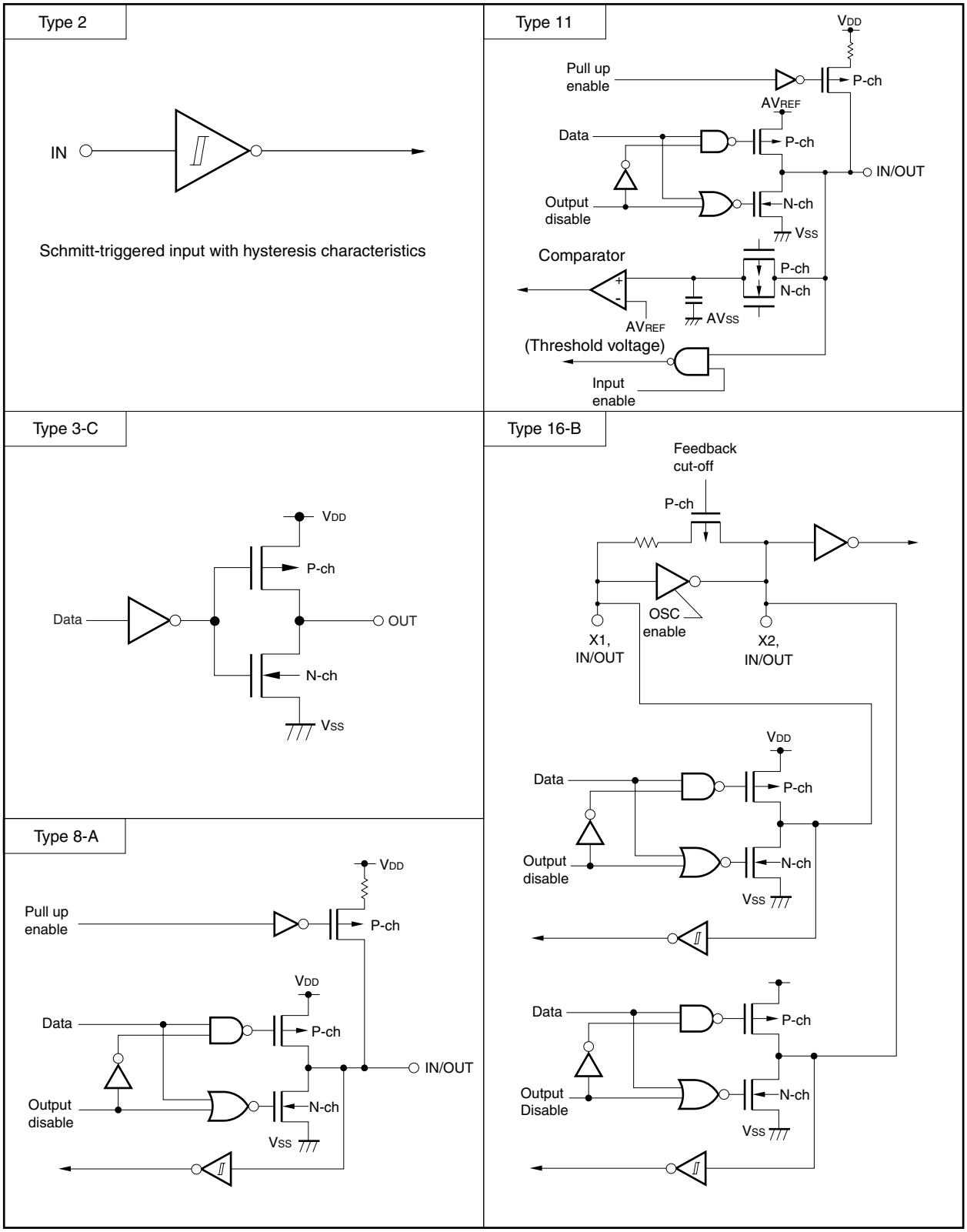
Table 1-1 shows I/O circuit type of each pin and the connections of unused pins.

For the configuration of the I/O circuit of each type, refer to **Figure 1-1**.

Table 1-1. Types of Pin I/O Circuits and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P00 to P03	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P20/ANI0 to P23/ANI3	11		Input: Independently connect to AV_{REF} or V_{SS} via a resistor. Output: Leave open.
P30/TI000/INTP0	8-A		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P31/TI010/TO00/INTP2			
P32 and P33			
P34/$\overline{\text{RESET}}$	2	Input	Connect to V_{DD} via a resistor.
P40	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P41/INTP3			
P42/TOH1			
P43/TxD6/INTP1			
P44/RxD6			
P45 to P47			
P120			
P121/X1	16-B		Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P122/X2			
P123	8-A		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P130	3-C	Output	Leave open.
AV_{REF}	–	–	Directly connect to V_{DD}.
AV_{SS}	–	–	Directly connect to V_{SS}.

Figure 1-1. Pin I/O Circuits



2. ELECTRICAL SPECIFICATIONS (TARGET)

These specifications are only target values, and may not be satisfied by mass-produced products.

Absolute Maximum Ratings (T_A = 25°C)

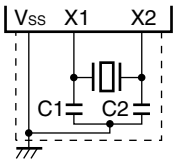
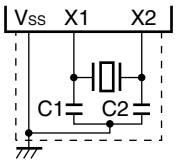
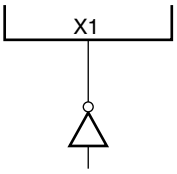
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.3 to +6.5	V
	V_{SS}		−0.3 to +0.3	V
	AV_{REF}		−0.3 to V_{DD} + 0.3[Note]	V
	AV_{SS}		−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P30 to P34, P40 to P47, P120 to P123	−0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P20 to P23	−0.3 to AV_{REF} + 0.3[Note] and −0.3 to V_{DD} + 0.3[Note]	V
Output voltage	V_O		−0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}		−0.3 to AV_{REF} + 0.3[Note] and −0.3 to V_{DD} + 0.3[Note]	V
Output current, high	I_{OH}	Per pin	−10.0	mA
		Total of pins other than P20 to P23	−44.0	mA
		Total of P20 to P23	−44.0	mA
Output current, low	I_{OL}	Per pin	20.0	mA
		Total of pins other than P20 to P23	44.0	mA
		Total of P20 to P23	44.0	mA
Operating ambient temperature	T_A	In normal operation mode	−40 to +85	°C
		During flash memory programming		
Storage temperature	T_{stg}	Flash memory blank status	−65 to +150	°C
		Flash memory programming already performed	−40 to +125	°C

Note Must be 6.5 V or lower

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

X1 Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 2]		2.0		10.0	MHz
Crystal resonator		Oscillation frequency (f_X)[Note 2]		2.0		10.0	MHz
External clock		X1 input frequency (f_X)[Note 2]	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		10.0	MHz
			2.0 V ≤ V_{DD} < 2.7 V	2.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	2.7 V ≤ V_{DD} ≤ 5.5 V	0.045		0.25	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.09		0.25	

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

High-Speed Internal Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
High-speed internal oscillator	Oscillation frequency (f_X = 8 MHz[Note 2]) deviation	2.7 V ≤ V_{DD} ≤ 5.5 V	T_A = –10 to +80°C			±3	%
			T_A = –40 to +85°C			±5	%
	Oscillation frequency (f_X)[Note 2]	2.0 V ≤ V_{DD} < 2.7 V		5.5			MHz

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Low-Speed Internal Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note], V_{SS} = 0 V)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Low-speed internal oscillator	Oscillation frequency (f_{RL})		120	240	480	kHz

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note], V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH1}	Pins other than P20 to P23	Per pin	2.0 V ≤ V_{DD} ≤ 5.5 V			–5	mA
			Total	4.0 V ≤ V_{DD} ≤ 5.5 V			–25	mA
				2.0 V ≤ V_{DD} < 4.0 V			–15	mA
	I_{OH2}	P20 to P23	Per pin	2.0 V ≤ AV_{REF} ≤ 5.5 V			–5	mA
			Total	2.0 V ≤ AV_{REF} ≤ 5.5 V			–15	mA
Output current, low	I_{OL1}	Pins other than P20 to P23	Per pin	2.0 V ≤ V_{DD} ≤ 5.5 V			10	mA
			Total	4.0 V ≤ V_{DD} ≤ 5.5 V			30	mA
				2.0 V ≤ V_{DD} < 4.0 V			15	mA
	I_{OL2}	P20 to P23	Per pin	2.0 V ≤ AV_{REF} ≤ 5.5 V			10	mA
			Total	4.0 V ≤ AV_{REF} ≤ 5.5 V			30	mA
				2.0 V ≤ AV_{REF} < 4.0 V			15	mA
Input voltage, high	V_{IH1}	P00 to P03, P30 to P34, P40 to P47, P120, P123			0.8V_{DD}		V_{DD}	V
	V_{IH2}	P20 to P23			0.7AV_{REF}		AV_{REF}	V
	V_{IH3}	P121, P122			0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P03, P30 to P34, P40 to P47, P120, P123			0		0.2V_{DD}	V
	V_{IL2}	P20 to P23			0		0.3AV_{REF}	V
	V_{IL3}	P121, P122			0		0.2V_{DD}	V
Output voltage, high	V_{OH1}	Total of pins other than P20 to P23 I_{OH1} = –15 mA		4.0 V ≤ V_{DD} ≤ 5.5 V I_{OH1} = –5 mA	V_{DD} – 1.0			V
		I_{OH1} = –100 μA		2.0 V ≤ V_{DD} < 4.0 V	V_{DD} – 0.5			V
	V_{OH2}	Total of pins P20 to P23 I_{OH2} = –10 mA		4.0 V ≤ AV_{REF} ≤ 5.5 V I_{OH2} = –5 mA	AV_{REF} – 1.0			V
		2.0 V ≤ AV_{REF} < 4.0 V I_{OH2} = –100 μA			AV_{REF} – 0.5			V
Output voltage, low	V_{OL1}	Total of pins other than P20 to P23 I_{OL1} = 30 mA		4.0 V ≤ V_{DD} ≤ 5.5 V I_{OL1} = 10 mA			1.3	V
		2.0 V ≤ V_{DD} < 4.0 V		I_{OL1} = 400 μA			0.4	V
	V_{OL2}	Total of pins P20 to P23 I_{OL2} = 30 mA		4.0 V ≤ AV_{REF} ≤ 5.5 V I_{OL2} = 10 mA			1.3	V
		2.0 V ≤ AV_{REF} < 4.0 V		I_{OL2} = 400 μA			0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD}		Pins other than X1			1	μA
Input leakage current, low	I_{LIL}	V_I = 0 V		Pins other than X1			–1	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}		Pins other than X2			1	μA
Output leakage current, low	I_{LOL}	V_O = 0 V		Pins other than X2			–1	μA
Pull-up resistance	R_{PU}	V_I = 0 V			10	30	100	kΩ
Pull-down resistance	R_{PD}	P121, P122, reset status			10	30	100	kΩ

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 2]	I_{DD1}[Note 3]	Crystal/ceramic oscillation, external clock input oscillation operating mode[Note 6]	f_X = 10 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		6.1	12.2	mA
				When A/D converter is operating[Note 8]		7.6	15.2	
			f_X = 6 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		5.5	11.0	mA
				When A/D converter is operating[Note 8]			14.0	
			f_X = 5 MHz V_{DD} = 3.0 V ±10%[Note 5]	When A/D converter is stopped		3.0	6.0	mA
				When A/D converter is operating[Note 8]		4.5	9.0	
	I_{DD2}	Crystal/ceramic oscillation, external clock input HALT mode[Note 6]	f_X = 10 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.7	3.8	mA
				When peripheral functions are operating			6.7	
			f_X = 6 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.3	3.0	mA
				When peripheral functions are operating			6.0	
			f_X = 5 MHz V_{DD} = 3.0 V ±10%[Note 5]	When peripheral functions are stopped		0.48	1	mA
				When peripheral functions are operating			2.1	
	I_{DD3}[Note 3]	High-speed internal oscillation operating mode[Note 7]	f_X = 8 MHz V_{DD} = 5.0 V ±10%[Note 4]	When A/D converter is stopped		5.0	10.0	mA
				When A/D converter is operating[Note 8]		6.5	13.0	
	I_{DD4}	High-speed internal oscillation HALT mode[Note 7]	f_X = 8 MHz V_{DD} = 5.0 V ±10%[Note 4]	When peripheral functions are stopped		1.4	3.2	mA
				When peripheral functions are operating			5.9	
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%	When low-speed internal oscillation is stopped		3.5	20.0	μA
				When low-speed internal oscillation is operating		17.5	32.0	
			V_{DD} = 3.0 V ±10%	When low-speed internal oscillation is stopped		3.5	15.5	μA
				When low-speed internal oscillation is operating		11.0	26.0	

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

2. Total current flowing through the internal power supply (V_{DD}). Peripheral operation current is included (however, the current that flows through the pull-up resistors of ports is not included).

3. Peripheral operation current is included.

4. When the processor clock control register (PCC) is set to 00H.

5. When the processor clock control register (PCC) is set to 02H.

6. When crystal/ceramic oscillation clock, external clock input is selected as the system clock source using the option byte.

7. When the high-speed internal oscillation clock is selected as the system clock source using the option byte.

8. The current that flows through the AV_{REF} pin is included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Crystal/ceramic oscillation clock, external clock input	4.0 V ≤ V_{DD} ≤ 5.5 V	0.2		16	μs
			3.0 V ≤ V_{DD} < 4.0 V	0.33		16	μs
			2.7 V ≤ V_{DD} < 3.0 V	0.4		16	μs
			2.0 V ≤ V_{DD} < 2.7 V	1		16	μs
		High-speed internal oscillation clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.23		4.22	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.47		4.22	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.95		4.22	μs
TI000/TI010 input high-level width, low-level width	t_{TIH}, t_{TIL}	4.0 V ≤ V_{DD} ≤ 5.5 V		2/fsam+ 0.1[Note 2]			μs
		2.0 V ≤ V_{DD} < 4.0 V		2/fsam+ 0.2[Note 2]			μs
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			2			μs

Notes 1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

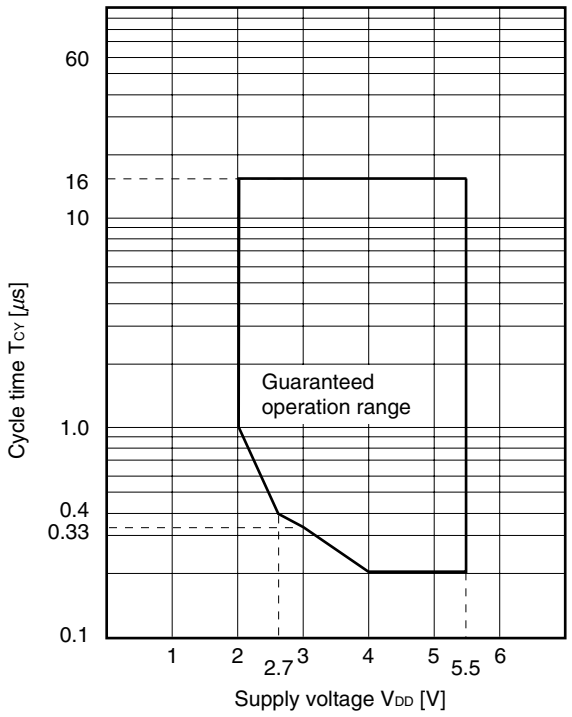
2. Selection of fsam = f_{XP}, f_{XP}/4, or f_{XP}/256 is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 or TI010 valid edge as the count clock, fsam = f_{XP}.

CPU Clock Frequency, Peripheral Clock Frequency

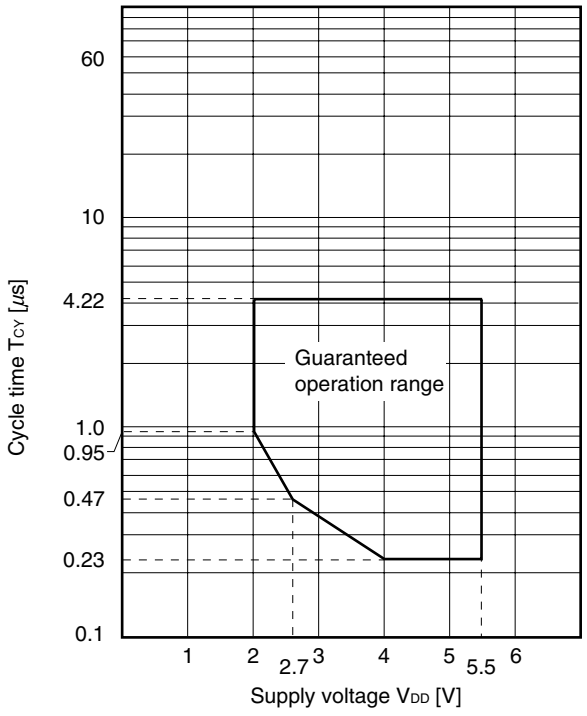
Parameter	Conditions	CPU clock (f_{CPU})	Peripheral clock (f_{XP})
Ceramic resonator, Crystal resonator, External clock	4.0 V ≤ V_{DD} ≤ 5.5 V	125 kHz ≤ f_{CPU} ≤ 10 MHz	500 kHz ≤ f_{XP} ≤ 10 MHz
	3.0 V ≤ V_{DD} < 4.0 V	125 kHz ≤ f_{CPU} ≤ 6 MHz	
	2.7 V ≤ V_{DD} < 3.0 V	125 kHz ≤ f_{CPU} ≤ 5 MHz	
	2.0 V ≤ V_{DD} < 2.7 V[Note]	125 kHz ≤ f_{CPU} ≤ 2 MHz	500 kHz ≤ f_{XP} ≤ 5 MHz
High-speed internal oscillator	4.0 V ≤ V_{DD} ≤ 5.5 V	500 kHz (Typ.) ≤ f_{CPU} ≤ 8 MHz (Typ.)	2 MHz (Typ.) ≤ f_{XP} ≤ 8 MHz (Typ.)
	2.7 V ≤ V_{DD} < 4.0 V	500 kHz (Typ.) ≤ f_{CPU} ≤ 4 MHz (Typ.)	
	2.0 V ≤ V_{DD} < 2.7 V[Note]	500 kHz (Typ.) ≤ f_{CPU} ≤ 2 MHz (Typ.)	2 MHz (Typ.) ≤ f_{XP} ≤ 4 MHz (Typ.)

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

T_{CY} vs. V_{DD} (Crystal/Ceramic Oscillation Clock, External Clock Input)



T_{CY} vs. V_{DD} (High-speed internal oscillator Clock)



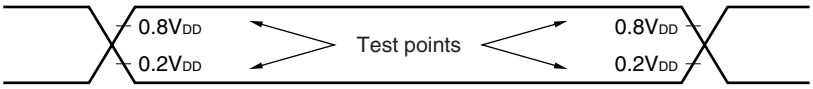
(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V[Note], V_{SS} = 0 V)

UART mode (UART6, dedicated baud rate generator output)

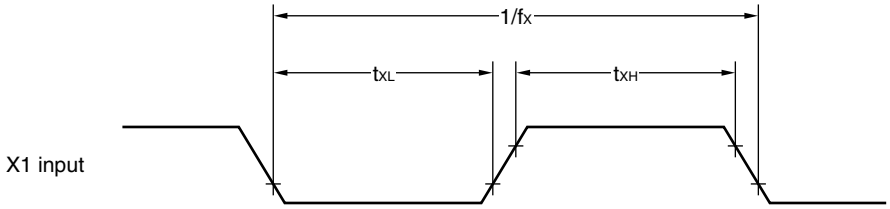
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

Note Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

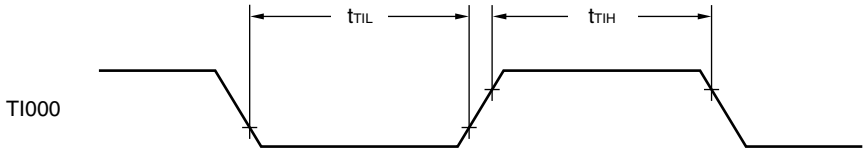
AC Timing Test Points (Excluding X1 Input)



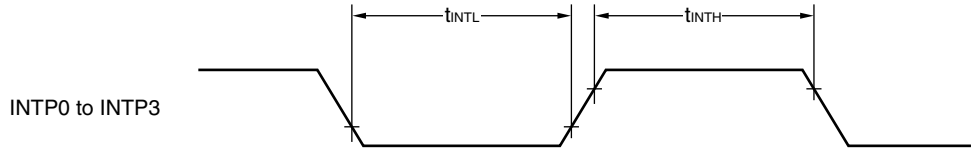
Clock Timing



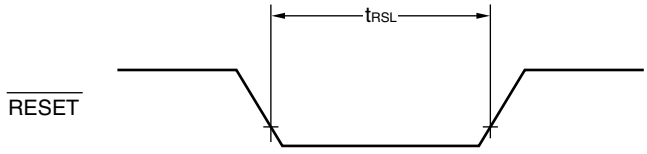
TI000 Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



A/D Converter Characteristics (T_A = –40 to +85°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ AV_{REF} ≤ 4.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ 5.5 V	3.0		100	μs
		4.0 V ≤ AV_{REF} < 4.5 V	4.8		100	μs
		2.85 V ≤ AV_{REF} < 4.0 V	6.0		100	μs
		2.7 V ≤ AV_{REF} < 2.85 V	14.0		100	μs
Zero-scale error[Notes 1, 2]	Ezs	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	Efs	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
Integral non-linearity error[Note 1]	ILE	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
Differential non-linearity error[Note 1]	DLE	4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
Analog input voltage	V_{AIN}		V_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The conversion accuracy may be degraded if the level of a port that is not used for A/D conversion is changed during A/D conversion.

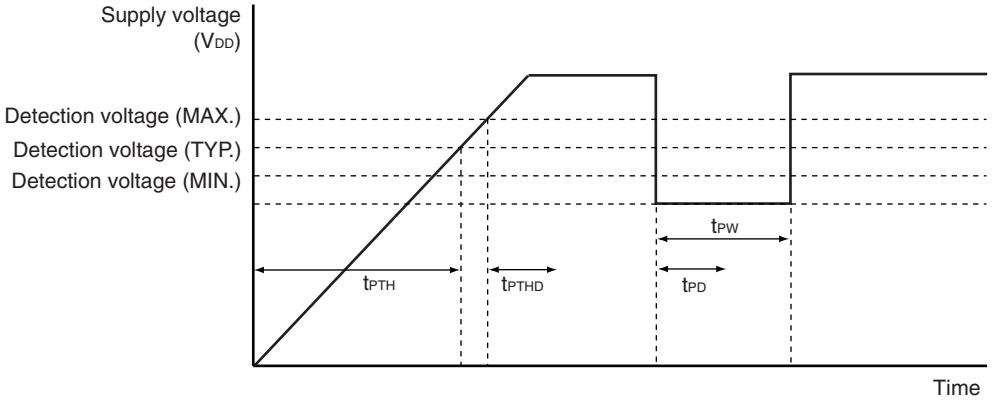
POC Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		2.0	2.1	2.2	V
Power supply boot time	t_{PTH}	V_{DD}: 0 V → 2.1 V	1.5			μs
Response delay time 1[Note 1]	t_{PTHD}	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2[Note 2]	t_{PD}	When power supply falls			1.0	ms
Minimum pulse width	t_{PW}		0.2			ms

Notes 1. Time required from voltage detection to internal reset release.

2. Time required from voltage detection to internal reset signal generation.

POC Circuit Timing



LVI Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.1	4.3	4.5	V
	V_{LVI1}		3.9	4.1	4.3	V
	V_{LVI2}		3.7	3.9	4.1	V
	V_{LVI3}		3.5	3.7	3.9	V
	V_{LVI4}		3.3	3.5	3.7	V
	V_{LVI5}		3.15	3.3	3.45	V
	V_{LVI6}		2.95	3.1	3.25	V
	V_{LVI7}		2.7	2.85	3.0	V
	V_{LVI8}		2.5	2.6	2.7	V
	V_{LVI9}		2.25	2.35	2.45	V
Response time[Note 1]	t_{LD}			0.2	2.0	ms
Minimum pulse width	t_{LW}		0.2			ms
Operation stabilization wait time[Note 2]	t_{LWAIT}			0.1	0.2	ms

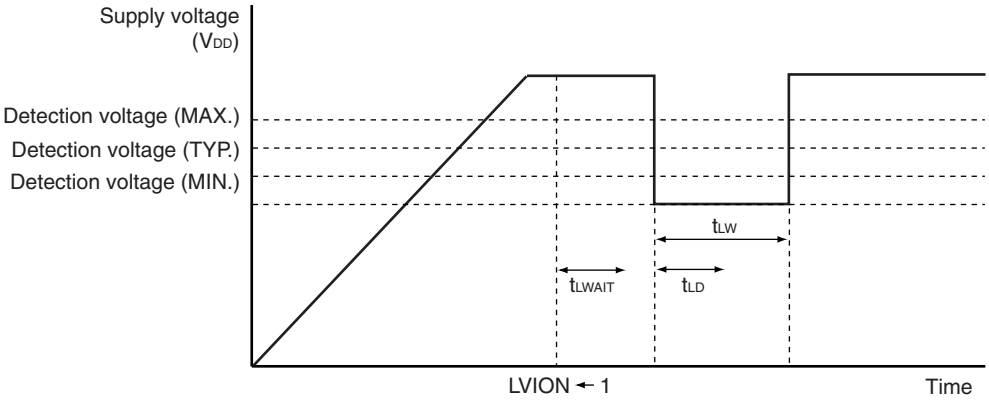
Notes 1. Time required from voltage detection to interrupt output or internal reset signal generation.

2. Time required from setting LVION to 1 to operation stabilization.

Remarks 1. $V_{LVI0} > V_{LVI1} > V_{LVI2} > V_{LVI3} > V_{LVI4} > V_{LVI5} > V_{LVI6} > V_{LVI7} > V_{LVI8} > V_{LVI9}$

2. $V_{POC} < V_{LVIm}$ (m = 0 to 9)

LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Release signal set time	t_{SREL}		0			μs

Flash Memory Programming Characteristics (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	V_{DD} = 5.5 V				7.0	mA
Erasure count[Note 1] (per 1 block)	N_{ERASE}	T_A = –40 to +85°C		1000			Times
Chip erase time	T_{CERASE}	T_A = –10 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.8	s
			3.5 V ≤ V_{DD} < 4.5 V			1.0	s
			2.7 V ≤ V_{DD} < 3.5 V			1.2	s
		T_A = –10 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			4.8	s
			3.5 V ≤ V_{DD} < 4.5 V			5.2	s
			2.7 V ≤ V_{DD} < 3.5 V			6.1	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			1.6	s
			3.5 V ≤ V_{DD} < 4.5 V			1.8	s
			2.7 V ≤ V_{DD} < 3.5 V			2.0	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			9.1	s
			3.5 V ≤ V_{DD} < 4.5 V			10.1	s
			2.7 V ≤ V_{DD} < 3.5 V			12.3	s
Block erase time	T_{BERASE}	T_A = –10 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.4	s
			3.5 V ≤ V_{DD} < 4.5 V			0.5	s
			2.7 V ≤ V_{DD} < 3.5 V			0.6	s
		T_A = –10 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			2.6	s
			3.5 V ≤ V_{DD} < 4.5 V			2.8	s
			2.7 V ≤ V_{DD} < 3.5 V			3.3	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.9	s
			3.5 V ≤ V_{DD} < 4.5 V			1.0	s
			2.7 V ≤ V_{DD} < 3.5 V			1.1	s
		T_A = –40 to +85°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			4.9	s
			3.5 V ≤ V_{DD} < 4.5 V			5.4	s
			2.7 V ≤ V_{DD} < 3.5 V			6.6	s
Byte write time	T_{WRITE}	T_A = –40 to +85°C, N_{ERASE} ≤ 1000				150	μs
Internal verify	T_{VERIFY}	Per 1 block				6.8	ms
		Per 1 byte				27	μs
Blank check	T_{BLKCHK}	Per 1 block				480	μs
Retention years		T_A = 85°C[Note 2], N_{ERASE} ≤ 1000		10			Years

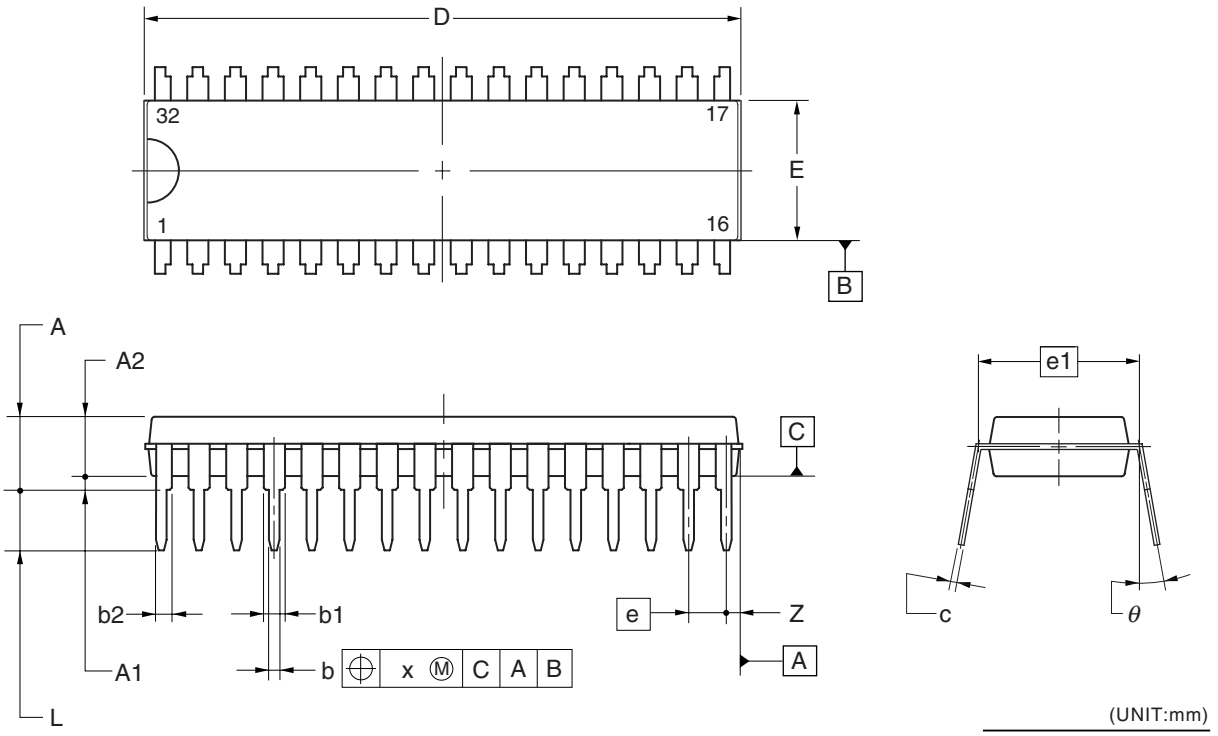
Note 1. Depending on the erasure count (N_{ERASE}), the erase time varies. Refer to the chip erase time and block erase time parameters.

2. When the average temperature when operating and not operating is 85°C.

Remark When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

3. PACKAGE DRAWING

32-PIN PLASTIC SDIP (7.62mm(300))



(UNIT:mm)

ITEM	DIMENSIONS
D	28.05±0.15
E	6.60±0.20
A	3.45±0.15
A1	0.65±0.10
A2	2.80
e	1.778
e1	7.62
b	0.50±0.10
b1	1.02±0.10
b2	0.75±0.10
c	$0.25^{+0.10}_{-0.05}$
L	2.86±0.20
x	0.25
θ	0° to 15°
Z	0.615

P32CS-70-CAA

APPENDIX A. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD78F9232CS, 78F9234CS Preliminary Product Information	This manual
78K0S/KB1+ User's Manual	U17446E
78K/0S Series Instructions User's Manual	U11047E

Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U16656E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U16654E
	Language	U14872E
ID78K0S-NS Ver. 2.52 Integrated Debugger	Operation	U16584E
ID78K0S-QB Ver. 2.81 Integrated Debugger	Operation	U17287E
PM plus Ver. 5.20		U16934E

Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
QB-78K0SKX1MINI In-Circuit Emulator	U17272E
QB-78K0SKX1 In-Circuit Emulator	U17219E
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E

Documents Related to Flash Memory Writing (User's Manuals)

Document Name	Document No.
PG-FP4 Flash Memory Programmer	U15260E
PG-FPL2 Flash Memory Programmer	U17307E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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