G-LINK

GLT6100L08

Ultra Low Power 128k x 8 CMOS SRAM

Nov 2000(Rev. 02)

Features :

* Low-power consumption.
  -active: 30mA at 55ns.
  -Stand by :
  5 µA (CMOS input / output)
  1 µA (CMOS input / output, SL)
* Single +2.7 to 3.3V Power Supply.
* Equal access and cycle time.
* 55/70/85/100 ns access time.
* Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ inputs.
* 2.0V data retention mode.
* TTL compatible, Tri-state input/output.
* Automatic power-down when deselected.

Description :

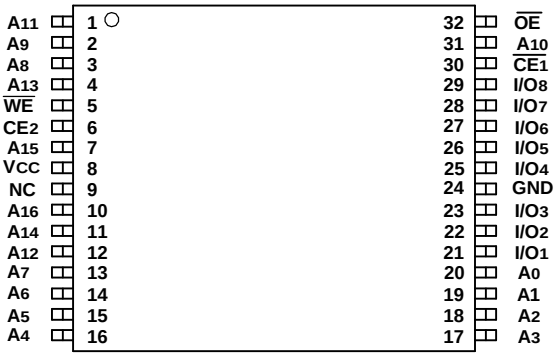
The GLT6100L08 is a low power CMOS Static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$, an active HIGH CE2, an active LOW OE, and Tri-state I/O's. This device has an automatic power-down mode feature when deselected.

Writing to the device is accomplished by taking chip Enable 1 ($\overline{CE1}$) with Write Enable ($\overline{WE}$) LOW, and Chip Enable 2 (CE2) HIGH. Reading from the device is performed by taking Chip Enable 1 ($\overline{CE1}$) with Output Enable ($\overline{OE}$) LOW while Write Enable ($\overline{WE}$) AND Chip Enable 2 (CE2) is HIGH. The I/O pins are placed in a high-impedance state when the device is deselected : the outputs are disabled during a write cycle.

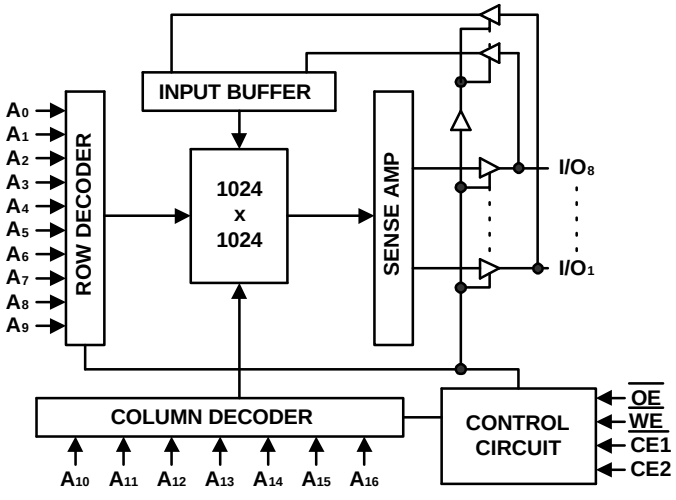
The GLT6100L08 comes with a 2V data retention feature and Lower Standby Power. The GLT6100L08 is available in a 32-pin TSOPI / sTSOP / 48-fpBGA packages.

Pin Configurations :

GLT6100L08



Function Block Diagram :



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Pin Descriptions:

Name	Function
A_0 - A_{16}	Address Inputs
$\overline{CE}_1$ and CE_2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_0 - I/O_7	Data Input and Data Output
V_{CC}	3V Power Supply
GND	Ground
NC	No Connection

Truth Table:

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High-Z	Standby
X	L	X	X	High-Z	Standby
L	H	H	L	Data Out	Active, Read
L	H	H	H	High-Z	Active, Output Disable
L	H	L	X	Data Out	Active, Write

Absolute Maximum Ratings*

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	4.6	V
Power Dissipation	P_T	-	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	°C
Temperature Under Bias	Tbias	-40	+85	°C

*Note : Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions (TA = -25°C to 85°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
	V_{IL}	-0.5*	-	0.6	V

* V_{IL} min = -1.0V for pulse width less than $t_{RC}/2$.

** For Industrial Temperature.

DC Operating Characteristics (Vcc=2.7V to 3.3V, T_A =-25°C to 85°C)

Parameter	Sym.	Test Conditions		55		70		85		100		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, Vin = Gnd to V_{CC}			1		1		1		1	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}_1$ =V_{IH} or CE2 = V_{IH} V_{CC} = Max, V_{OUT} = Gnd to V_{CC}			1		1		1		1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}_1$ =V_{IL} ,CE2 = V_{IH} V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA			3		3		3		3	mA
Average Operating Current	I_{CC1}	$\overline{CE}_1$ =V_{IL} ,CE2 = V_{IH} I_{OUT} = 0mA, Min Cycle, 100% Duty			30		25		20		15	mA
	I_{CC2}	$\overline{CE}_1$ =0.2V CE2 = V_{CC} – 0.2V I_{OUT} = 0mA, Cycle Time=1µs, 100% Duty			3		3		3		3	mA
Standby Power Supply Current(TTL Level)	I_{SB}	$\overline{CE}_1$ =V_{IH} or CE2 = V_{IL}			0.5		0.5		0.5		0.5	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE}_1$ ≥ V_{CC}-0.2V or CE2 ≤ 0.2V, f=0 V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}-0.2V	GLT6100L08LL		5		5		5		5	µA
			GLT6100L08SL		1		1		1		1	µA
Output Low Voltage	V_{OL}	I_{OL} = 2 mA			0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = 2 mA		2.4		2.4		2.4		2.4		V

Data Retention

Parameter	Sym.	Test Conditions	Min.	Max.	Unit
V_{CC} for Data retention	V_{DR}	$\overline{CE}_1$ ≥ V_{CC} -0.2V or CE_2 ≤ +0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V	1.0	-	V
Data Retention Current	I_{CCDR}			5	µA
Chip Deselect to Data Retention Time	t_{CDR}		0	-	ns
Operating Recovery Time(2)	t_R		t_{RC}	-	ns

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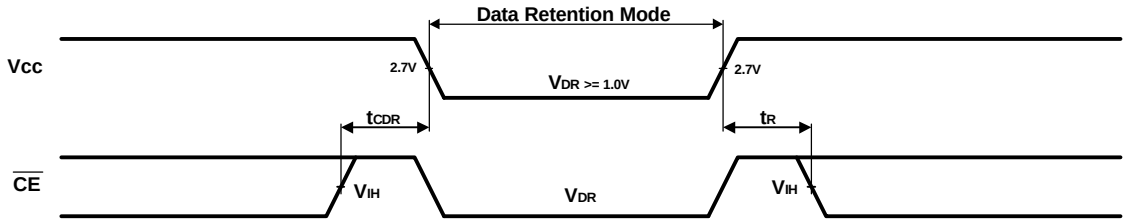
Data Retention Waveform (TA = -25°C to 85°C)

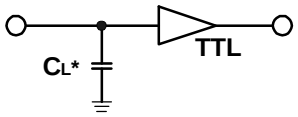


AC Test Conditions

Input Pulse Levels	0.6V to 2.2V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.4V

Output Load Condition
70ns / 85ns C_L = 30pf + 1TTL Load
Load 100ns / 120ns C_L = 100pf + 1TTL Load

AC Test Loads and Waveforms



*Including Scope and Jig Capacitance

Read Cycle [3,9] (Vcc=2.7V to 3.3V, T_A =-25°C to 85°C)

Parameter	Symbol	55		70		85		100		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	55		70		85		100		ns	
Address Access Time	t_{AA}		55		70		85		100	ns	
Chip Enable Access Time	t_{ACE}		55		70		85		100	ns	
Output Enable Access Time	t_{OE}		35		40		40		50	ns	
Output Hold from address Change	t_{OH}	10		10		10		10		ns	
Chip Enable to Output in Low-Z	t_{CLZ}	10		10		10		10		ns	4,5
Chip Disable to Output in High-Z	t_{CHZ}		25		30		35		40	ns	3,4,5
Output Enable to Output in Low-Z	t_{OLZ}	5		5		5		5		ns	
Output Disable to Output in High-Z	t_{OHZ}		25		25		30		35	ns	4,5
Power-Up Time	t_{PU}	0		0		0		0		ns	3,4,5
Power-Down Time	t_{PD}		55		70		85		100	ns	

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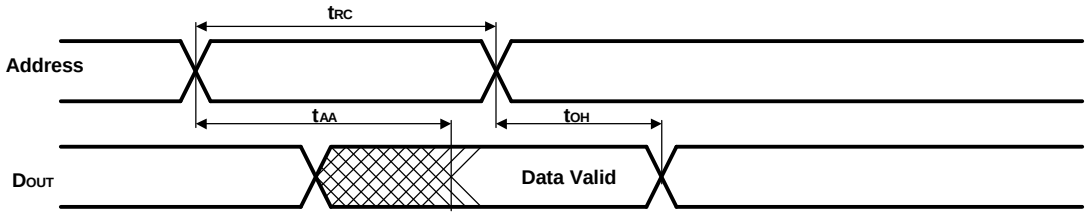
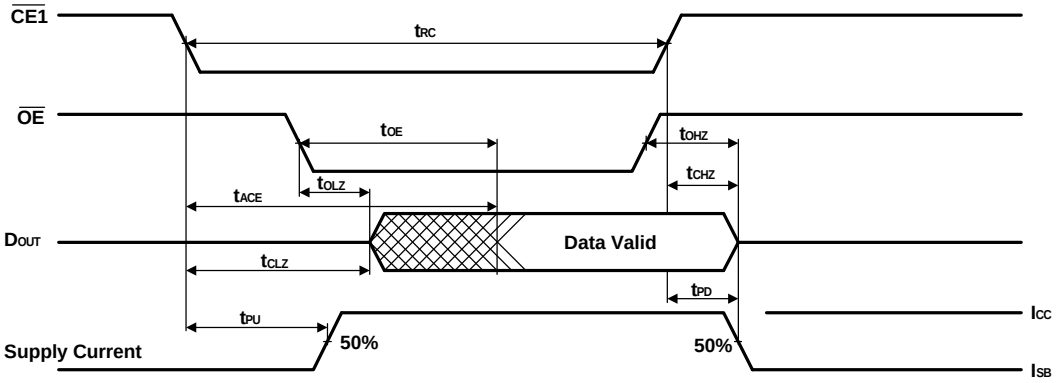
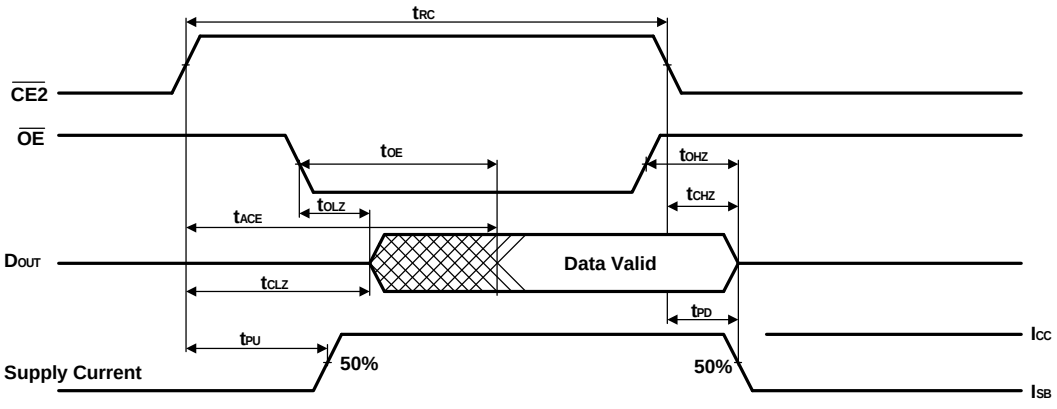
Timing Waveform of Read Cycle 1 (3,6,7,9) (Address Controlled)



Timing Waveform of Read Cycle 2 (5,6,8,9) ($\overline{CE1}$ Controlled)



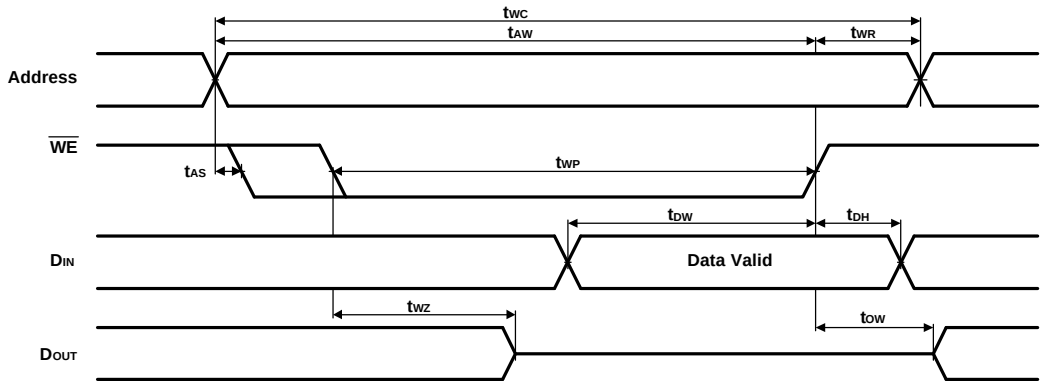
Timing Waveform of Read Cycle 1 (3,6,8,9) (CE2 Controlled)



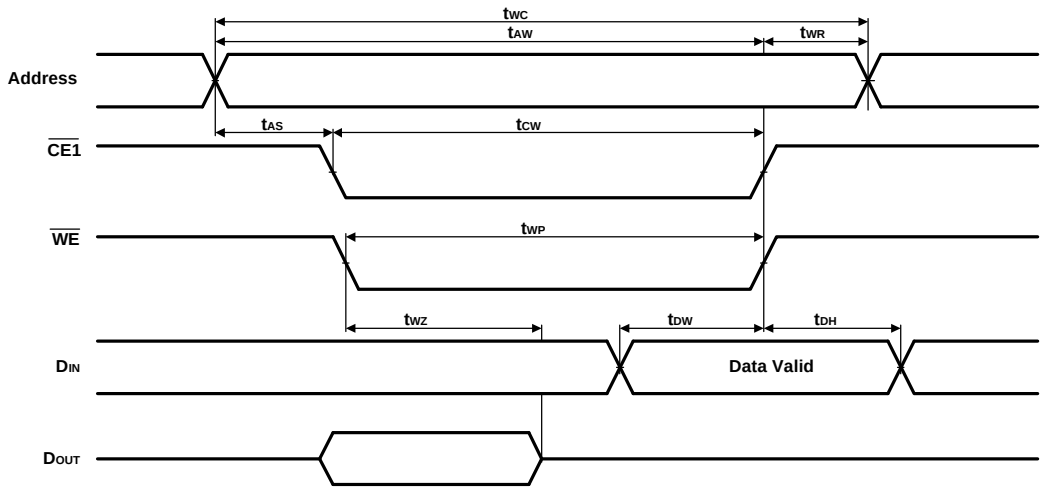
Write Cycle [3,9] (Vcc=2.7V to 3.3V, T_A = -25°C to 85°C)

Parameter	Symbol	55		70		85		100		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	55		70		85		100		ns	
Chip Enable to Write End	t_{CW}	45		60		70		80		ns	
Address Setup to Write End	t_{AW}	45		60		70		80		ns	
Address Setup Time	t_{AS}	0		0		0		0		ns	
Write Pulse Width	t_{WP}	45		50		60		70		ns	
Write Recovering Time	t_{WR}	0		0		0		0		ns	
Data Valid to Write End	t_{DW}	25		30		35		40		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enable to Output in High-Z	t_{WZ}		25		30		35		40	ns	
Output Active from Write End	t_{OW}	5		5		5		5		ns	

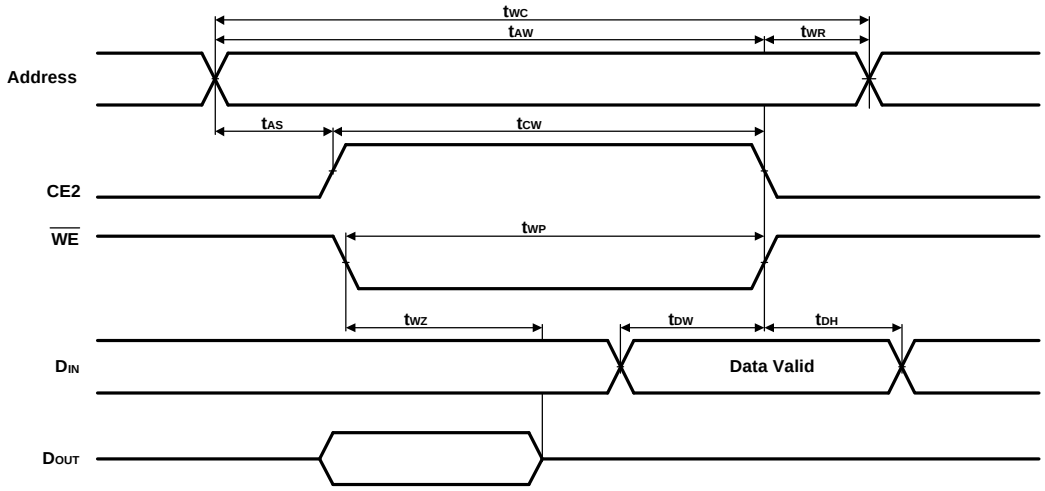
Timing Waveform of Write Cycle 1 [10,11] ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle 2 (10,11) ($\overline{CE1}$ Controlled)



Timing Waveform of Write Cycle 1 (10,11) (CE2 Controlled)



Notes :

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see AC Test Condition.
4. This parameter is tested with CL = 5pF. Transition is measured ± 500mV from steady – state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE1}$ transition LOW or CE2 transition HIGH.
9. All read cycle timings are referenced from the last valid address to the first transtion address.
10. $\overline{CE1}$ or WE must be HIGH or CE2 must be LOW during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

Part Number	*SPEED*	*POWER*	*PACKAGE*
GLT6100L08LL-55TS	55ns	Normal	TSOPI 32L
GLT6100L08LL-70TS	70ns	Normal	TSOPI 32L
GLT6100L08LL-85TS	85ns	Normal	TSOPI 32L
GLT6100L08LL-100TS	100ns	Normal	TSOPI 32L
GLT6100L08LL-55ST	55ns	Normal	sTSOPI 32L
GLT6100L08LL-70 ST	70ns	Normal	sTSOPI 32L
GLT6100L08LL-85 ST	85ns	Normal	sTSOPI 32L
GLT6100L08LL-100 ST	100ns	Normal	sTSOPI 32L
GLT6100L08SL-55TS	55ns	Normal	TSOPI 32L
GLT6100L08SL-70TS	70ns	Normal	TSOPI 32L
GLT6100L08SL-85TS	85ns	Normal	TSOPI 32L
GLT6100L08SL-100TS	100ns	Normal	TSOPI 32L
GLT6100L08SL-55ST	55ns	Normal	sTSOPI 32L
GLT6100L08SL-70 ST	70ns	Normal	sTSOPI 32L
GLT6100L08SL-85 ST	85ns	Normal	sTSOPI 32L
GLT6100L08SL-100 ST	100ns	Normal	sTSOPI 32L

Parts Numbers (Top Mark) Definition :

GLT 6 100 L 08 LL- 55 TS

4 : DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM

-SRAM
064 : 64K
256 : 256K
512 : 512K
100 : 1M
-DRAM
10 : 1M(C/EDO)*
11 : 1M(C/FPM)*
12 : 1M(H/EDO)*
13 : 1M(H/FPM)*
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
*See note

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.1V

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

SPEED
-SRAM
10 : 10ns
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
ST : sTSOP (Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP

LL : Low Low power
L : Low power
: Standard
SL : Super Low power

Note : C→CDROM , H→HDD.

Example :

1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

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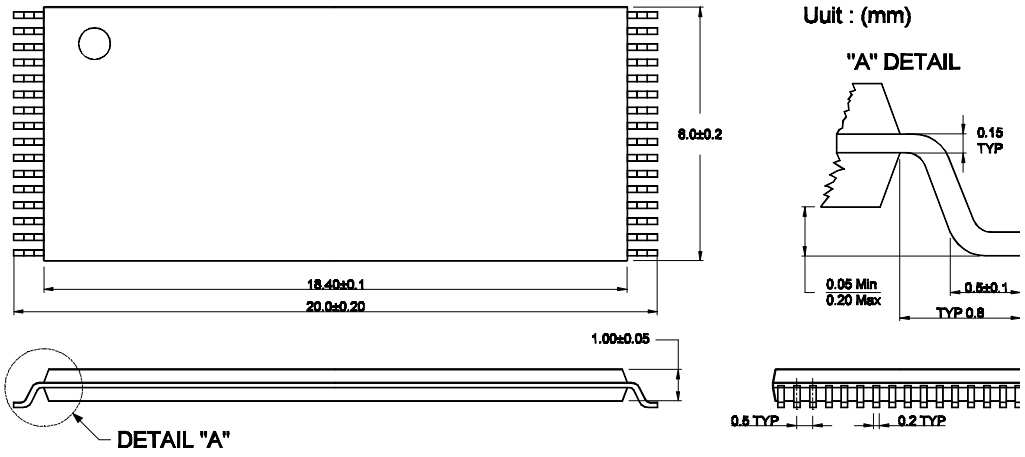
Package Information

32 pin 8x20mm Small Outline J-form Package (TSOP)



32 pin 8x13.4mm Small Outline J-form Package (sTSOP)