High Frequency Synchronous Step-Down Voltage Mode DC/DC Controller

FEATURES

- **Wide V_{IN} Range: 4.5V to 38V**
- **Line Feedforward Compensation**
- Low Minimum On-Time: $t_{ON(MIN)}$ < 30ns
- Powerful Onboard MOSFET Drivers
- Leading Edge Modulation Voltage Mode Control
- ±0.75%, 0.6V Reference Voltage Accuracy Over Temperature
- V_{OUT} Range: 0.6V to 0.8V_{IN}
- Programmable, Cycle-by-Cycle Peak Current Limit
- Sense Resistor or $R_{DS(ON)}$ Current Sensing
- Programmable Soft-Start
- Synchronizable Fixed Frequency from 250kHz to 1MHz
- Selectable Pulse-Skipping or Forced Continuous Modes of Operation
- Low Shutdown Current: 14µA Typical
- Thermally Enhanced 16-Lead MSOP and 3mm × 3mm QFN Packages

APPLICATIONS

- Automotive Systems
- Telecom and Industrial Power Supplies
- Point of Load Applications

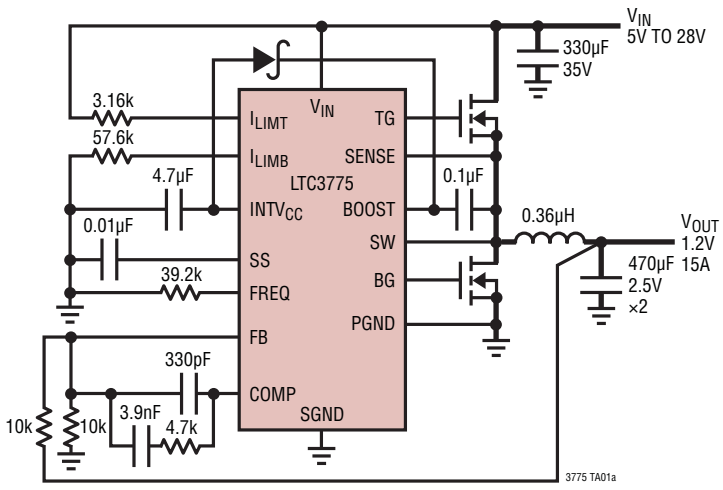
DESCRIPTION

The LTC®3775 is a high efficiency synchronous step-down switching DC/DC controller that drives an all N-channel power MOSFET stage from a 4.5V to 38V input supply voltage. A patented line feedforward compensation circuit and a high bandwidth error amplifier provide very fast line and load transient response.

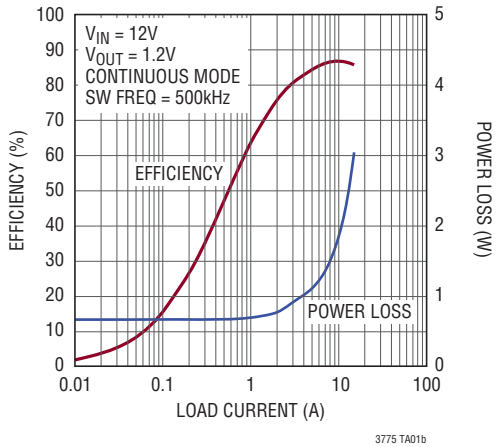
High step-down ratios are made possible by a low 30ns minimum on-time, allowing extremely low duty cycles. MOSFET $R_{DS(ON)}$ current sensing maximizes efficiency. Alternatively, a sense resistor can be used for higher current limit accuracy. Continuous monitoring of the voltages across the top and bottom MOSFETs allows cycle-by-cycle control of the inductor current, configurable by external resistors.

The soft-start function controls the duty cycle during start-up, providing a smooth output voltage ramp up. The operating frequency is user programmable from 250kHz to 1MHz and can be synchronized to an external clock.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current



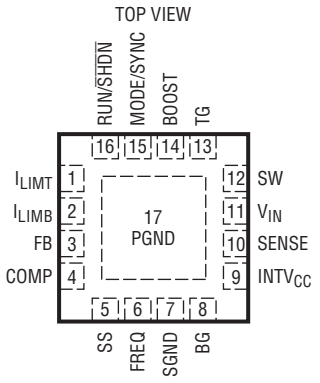
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{IN} ..... –0.3V to 40V
- BOOST ..... –0.3V to 46V
- BOOST-SW ..... –0.3V to 6V
- SW ..... –5V to 40V

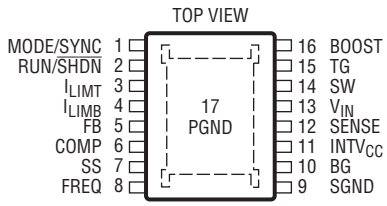
I_{LIMT} ..... –0.3V to V_{IN}
SENSE ..... –5V to V_{IN}
$INTV_{CC}$ ..... –0.3V to 6V
RUN/$\overline{SHDN}$ ..... –0.3V to 6V
FB, MODE/SYNC ..... –0.3V to $INTV_{CC}$
FREQ, I_{LIMB}, SS ..... –0.3V to $INTV_{CC}$
$INTV_{CC}$ RMS Currents 50mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W (NOTE 3)
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W (NOTE 3)
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3775EUD#PBF	LTC3775EUD#TRPBF	LDJK	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC3775IUD#PBF	LTC3775IUD#TRPBF	LDJK	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3775EMSE#PBF	LTC3775EMSE#TRPBF	3775	16-Lead Plastic MSOP	–40°C to 85°C
LTC3775IMSE#PBF	LTC3775IMSE#TRPBF	3775	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{RUN} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	V_{IN} Supply Voltage		●	4.5		38	V
I_{VIN}	Input DC Supply Current	V_{FB} = 0.7V (Note 5) V_{RUN} = 0V			3.5 14		mA µA
RUN/$\overline{SHDN}$ Pin							
V_{RUN}	RUN/$\overline{SHDN}$ Pin Enable Threshold			1.19	1.22	1.25	V
$V_{\overline{SHDN}}$	RUN/$\overline{SHDN}$ Pin Shutdown Threshold	$V_{RUN/\overline{SHDN}}$ Rising			0.74		V
$V_{\overline{SHDN}(HYST)}$	RUN/$\overline{SHDN}$ Pin Shutdown Threshold Hysteresis				140		mV
I_{RUN}	RUN/$\overline{SHDN}$ Pin Source Current	$V_{RUN/\overline{SHDN}}$ = 0V $V_{RUN/\overline{SHDN}}$ = 1.5V			–1 –5		µA µA
Error Amplifier							
V_{FB}	Feedback Pin Voltage		 ●	0.597 0.5955	0.600	0.603 0.6045	V V
ΔV_{FB}	Feedback Voltage Line Regulation	4.5V < V_{IN} < 38V			±0.01		%/V
ΔV_{OUT}	Output Voltage Load Regulation	1V < V_{COMP} < 2V (Note 6)			0.01	0.1	%
I_{FB}	FB Pin Input Current	V_{FB} = 0.6V		–50		50	nA
I_{COMP}	COMP Pin Output Current	Sourcing, V_{COMP} = 0V Sinking, V_{COMP} = 2V		–0.5 1	–1 60		mA mA
f_{0dB}	Error Amplifier Unity-Gain Crossover Frequency	(Note 6)			25		MHz
Soft-Start							
I_{SS}	SS Pin Source Current	V_{SS} = 0V			–1		µA
R_{SS}	SS Pin Pull-Down Resistance in Current Limit				1.3		kΩ
Current Limit							
I_{LIMB}	I_{LIMB} Source Current	V_{ILIMB} = 1V	●	–9	–10	–11	µA
I_{LIMT}	I_{LIMT} Sink Current	V_{ILIMT} = 12V	●	90	100	110	µA
I_{SENSE}	SENSE Pin Input Current					1	µA
$V_{ILIMT(MAX)}$	Topside Current Limit Threshold (V_{IN}-SENSE)	V_{ILIMT} = 0.1V	●	90	100	110	mV
$V_{ILIMB(MAX)}$	Bottom Side Current Limit Threshold (PGND-SW)	V_{ILIMB} = 0.5V	●	80	100	120	mV
$INTV_{CC}$ Low Dropout Voltage Regulator							
$INTV_{CC}$	LDO Regulator Output Voltage			4.9	5.2	5.5	V
$\Delta V_{INTVCC(LINE)}$	$INTV_{CC}$ Line Regulation	7.5V < V_{IN} < 38V			0.01		%/V
$\Delta V_{INTVCC(LOAD)}$	$INTV_{CC}$ Load Regulation	ΔI_{INTVCC} = 0mA to 20mA		–1	–0.1		%
$V_{DROPOUT}$	$INTV_{CC}$ Regulator Dropout Voltage (V_{IN} – V_{INTVCC})	I_{INTVCC} = 20mA			0.35		V
V_{UVLO}	$INTV_{CC}$ UVLO Voltage	$INTV_{CC}$ Rising Hysteresis		3.0	3.6 0.5	4.2	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, V_{RUN} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator							
f_{OSC}	Oscillator Frequency	R_{SET} = 39.2k	●	425	500	575	kHz
f_{HIGH}	Maximum Oscillator Frequency		●	1000			kHz
f_{LOW}	Minimum Oscillator Frequency		●			250	kHz
f_{SYNC}	External Sync Frequency Range	With Reference to Free Running		–20		20	%
$t_{ON(MIN)}$	TG Minimum On-Time	(Notes 6, 8) $V_{MODE/SYNC}$ = 0V			30		ns
$t_{OFF(MIN)}$	TG Minimum Off-Time	(Note 6)			300		ns
DC_{MAX}	Maximum TG Duty Cycle	f_{OSC} = 500kHz	●	90			%
V_{MODE}	MODE/SYNC Threshold	MODE/SYNC Rising			1.2		V
$V_{MODE(HYST)}$	MODE/SYNC Hysteresis				430		mV
$R_{MODE/SYNC}$	MODE/SYNC Input Resistance to SGND				50		kΩ
Driver							
BG R_{UP}	Bottom Gate (BG) Pull-Up On-Resistance				2.5		Ω
TG R_{UP}	Top Gate (TG) Pull-Up On-Resistance				2.5		Ω
BG R_{DOWN}	Bottom Gate (BG) Pull-Down On-Resistance				1.0		Ω
TG R_{DOWN}	Top Gate (TG) Pull-Down On-Resistance				1.5		Ω
BG, TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_L = 3300pF (Note 7)			15		ns
TG, BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_L = 3300pF (Note 7)			15		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3775 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3775E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3775I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: Failure to solder the exposed pad of the UD package to the PC board will result in a thermal resistance much higher than 68°C/W.

Note 4: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 5: Supply current in normal operation is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with supply voltage and the external MOSFETs used.

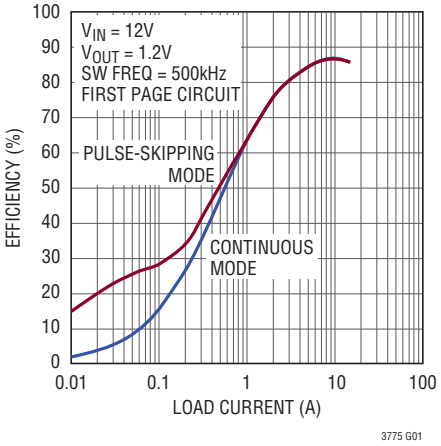
Note 6: Guaranteed by design, not subject to test.

Note 7: Rise and fall times are measured using 10% and 90% levels. Delay and nonoverlap times are measured using 50% levels.

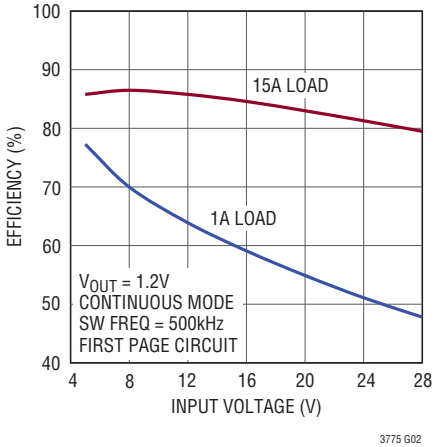
Note 8: The LTC3775 leading edge modulation architecture does not have a minimum TG pulse width requirement. The TG minimum pulse width is limited by the SW node rise and fall times.

TYPICAL PERFORMANCE CHARACTERISTICS

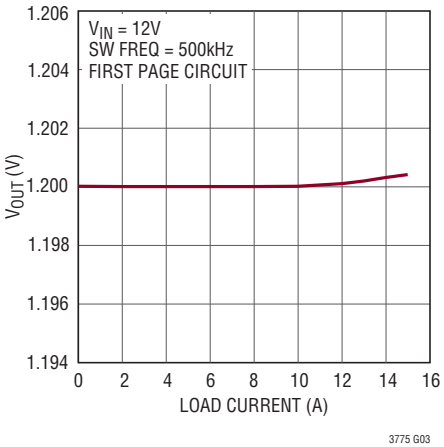
Efficiency vs Load Current



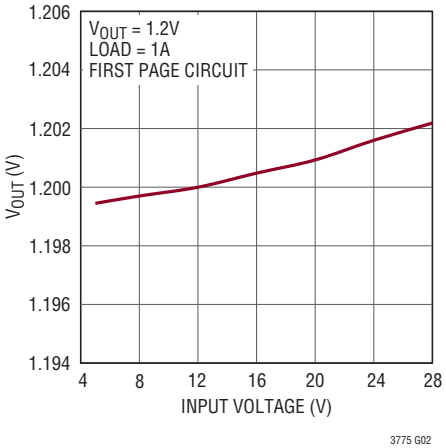
Efficiency vs Input Voltage



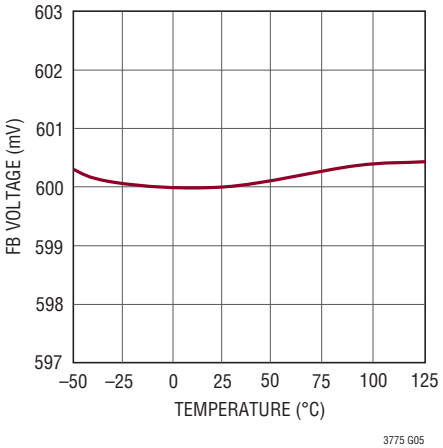
Load Regulation



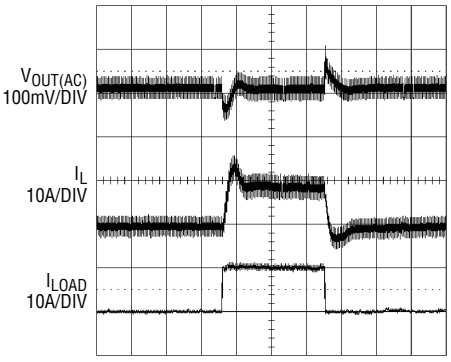
Line Regulation



FB Voltage vs Temperature

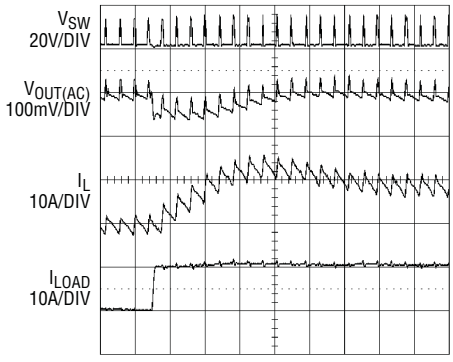


Load Step in Forced Continuous Mode



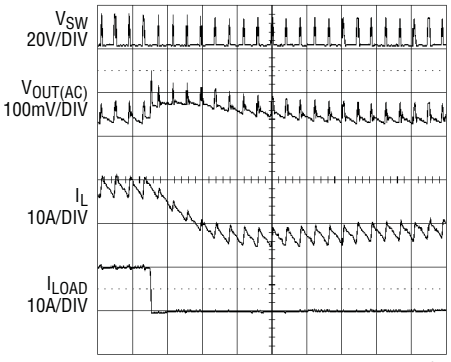
VIN = 12V 50µs/DIV
VOUT = 1.2V
LOAD STEP = 0A TO 10A TO 0A
MODE/SYNC = 0V
SW FREQ = 500kHz
FIRST PAGE CIRCUIT

Positive Load Step in Forced Continuous Mode



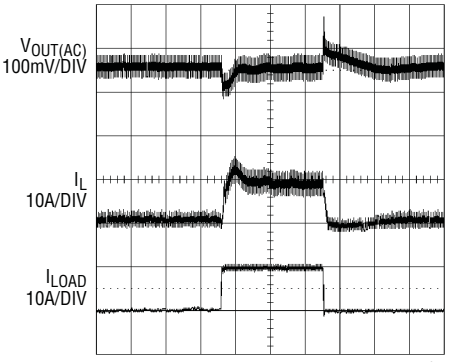
VIN = 12V 5µs/DIV
VOUT = 1.2V
LOAD STEP = 0A TO 10A
MODE/SYNC = 0V
SW FREQ = 500kHz
FIRST PAGE CIRCUIT

Negative Load Step in Forced Continuous Mode



VIN = 12V 5µs/DIV
VOUT = 1.2V
LOAD STEP = 10A TO 0A
MODE/SYNC = 0V
SW FREQ = 500kHz
FIRST PAGE CIRCUIT

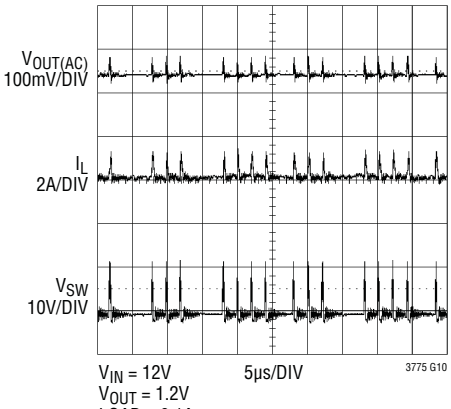
Load Step in Pulse-Skipping Mode



VIN = 12V 50µs/DIV
VOUT = 1.2V
LOAD STEP = 1A TO 11A TO 1A
MODE/SYNC = INTVCC
SW FREQ = 500kHz
FIRST PAGE CIRCUIT

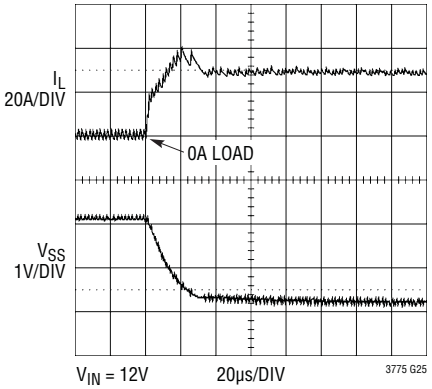
TYPICAL PERFORMANCE CHARACTERISTICS

Pulse-Skipping Mode Waveform with 0.1A Load



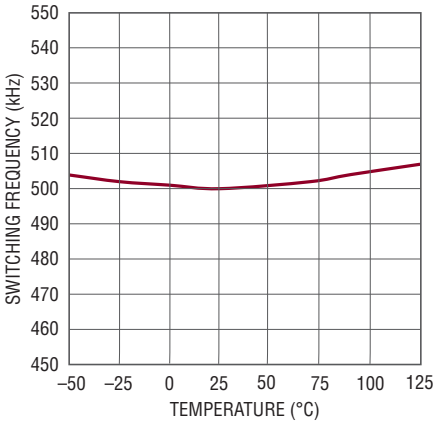
V_{IN} = 12V
V_{OUT} = 1.2V
LOAD = 0.1A
MODE/SYNC = $INTV_{CC}$
SW FREQ = 500kHz
FIRST PAGE CIRCUIT

Output Short-Circuit Waveform

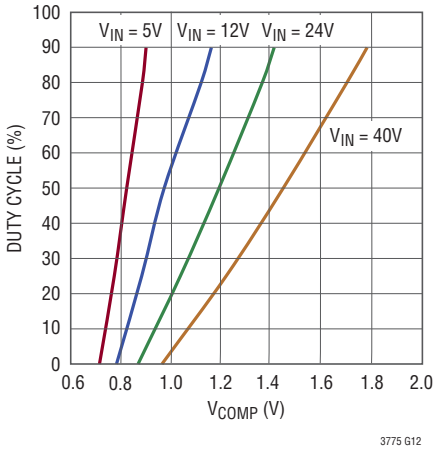


V_{IN} = 12V
V_{OUT} = 1.2V
C_{SS} = 0.01µF
FIRST PAGE CIRCUIT

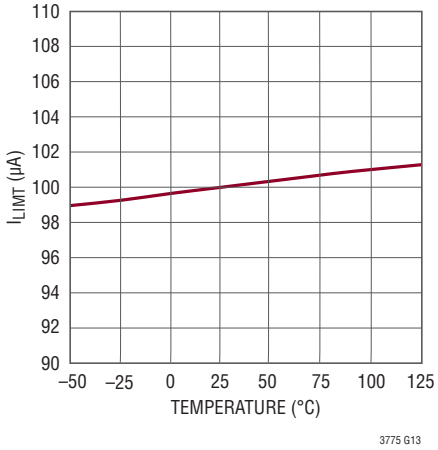
Switching Frequency vs Temperature



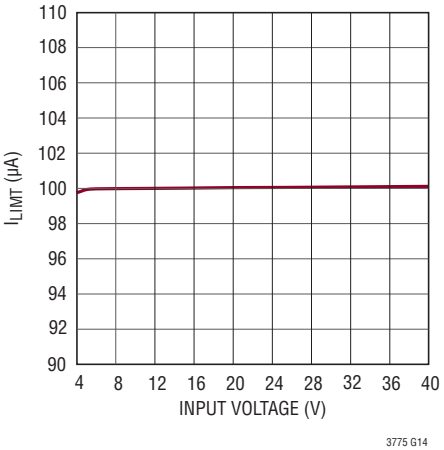
Duty Cycle vs V_{COMP}



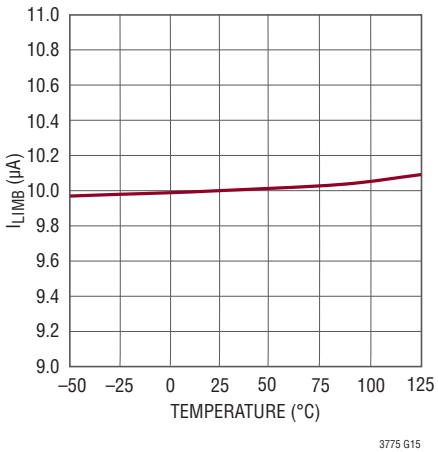
I_{LIMT} vs Temperature



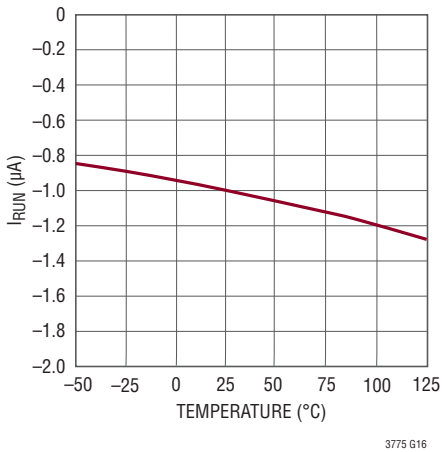
I_{LIMT} vs Input Voltage



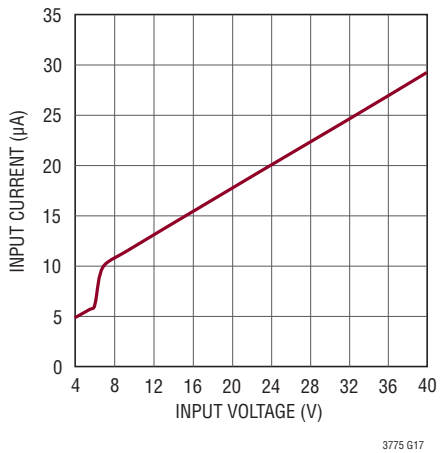
I_{LIMB} vs Temperature



I_{RUN} vs Temperature

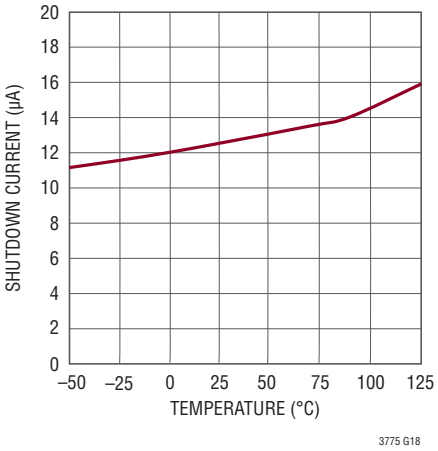


Shutdown Current vs Input Voltage

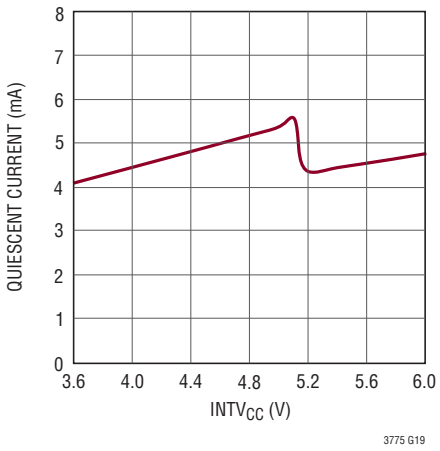


TYPICAL PERFORMANCE CHARACTERISTICS

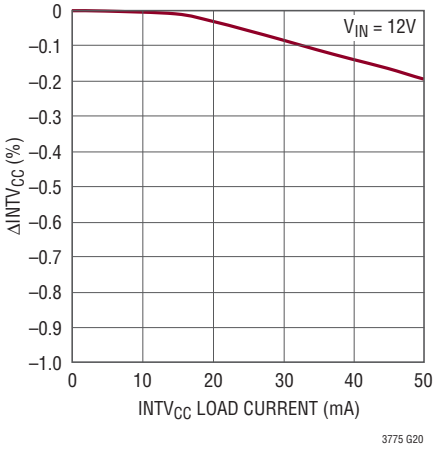
Shutdown Current vs Temperature



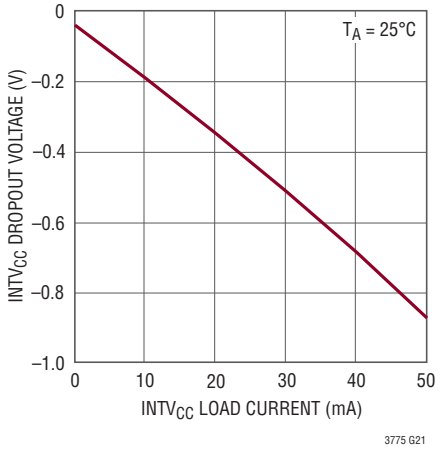
Quiescent Current vs $INTV_{CC}$



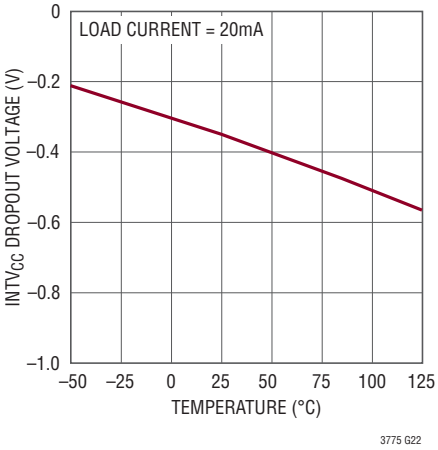
$INTV_{CC}$ Load Regulation



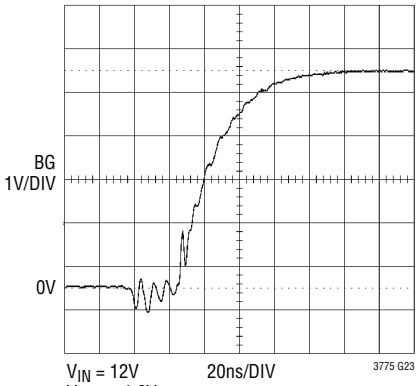
$INTV_{CC}$ Dropout



$INTV_{CC}$ Dropout vs Temperature

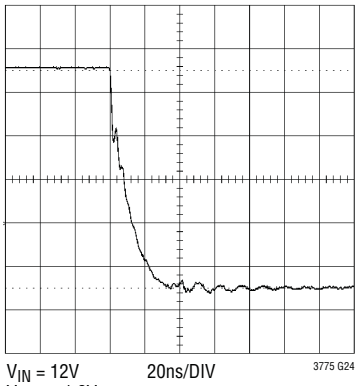


BG Turn-On Waveform Driving Renesas RJK0301



V_{IN} = 12V 20ns/DIV
V_{OUT} = 1.2V
LOAD = 1A
MOSFET: RENESAS RJK0301

BG Turn-Off Waveform Driving Renesas RJK0301



V_{IN} = 12V 20ns/DIV
V_{OUT} = 1.2V
LOAD = 1A
MOSFET: RENESAS RJK0301

PIN FUNCTIONS (QFN/MSOP)

I_{LIMT} (Pin 1/Pin 3): Topside Current Limit Set Point. This pin has an internal 100µA pull-down current, allowing the topside current limit threshold to be programmed by an external resistor connected to V_{IN}. See Current Limit Applications.

I_{LIMB} (Pin 2/Pin 4): Bottom Side Current Limit Set Point. This pin has an internal 10µA pull-up current, allowing the bottom side current limit threshold to be programmed by an external resistor connected to SGND. See Current Limit Applications.

FB (Pin 3/Pin 5): Error Amplifier Input. The FB pin is connected to a resistive divider from V_{OUT} to SGND. The feedback loop compensation network is also connected to this pin.

COMP (Pin 4/Pin 6): Error Amplifier Output. Use an RC network between the COMP pin and the FB pin to compensate the feedback loop for optimum transient response.

SS (Pin 5/Pin 7): Soft-Start. Connect this pin to an external capacitor, C_{SS}, to implement a soft-start function. When the voltage on the SS pin is less than the 0.6V internal reference, the LTC3775 regulates the V_{FB} voltage to the SS pin voltage instead of the 0.6V reference.

FREQ (Pin 6/Pin 8): Frequency Set. A resistor connected from this pin to SGND sets the free-running frequency of the internal oscillator. See Applications Information section for resistor value selection details.

SGND (Pin 7/Pin 9): Signal Ground. All the internal low power circuitry returns to the SGND pin. All feedback and soft-start connections should return to SGND. SGND should be Kelvin connected to a single point near the negative terminal of the V_{OUT} bypass capacitor.

BG (Pin 8/Pin 10): Bottom Gate Drive. This pin drives the gate of the bottom N-channel synchronous switch MOSFET. This pin swings from PGND to $INTV_{CC}$.

$INTV_{CC}$ (Pin 9/Pin 11): Internal 5.2V Regulator Output. The gate driver and control circuits are powered from this voltage. Bypass this pin to power ground with a low ESR ceramic capacitor of value 4.7µF or greater (X5R or better).

SENSE (Pin 10/Pin 12): Topside Current Sensing Input. Connect this pin to the switch node of the converter for top MOSFET $R_{DS(ON)}$ current sensing. Alternatively, this pin can be connected to a sense resistor at the drain of the top MOSFET for more accurate current limit.

V_{IN} (Pin 11/Pin 13): Main Input Supply. Bypass this pin to PGND with a low ESR ceramic capacitor of value 1µF or greater (X5R or better).

SW (Pin 12/Pin 14): Switch Node. Connect this pin to the source of the upper power MOSFET. This pin is also used as the input to the bottom side current limit comparator and the zero-crossing reverse current comparator.

TG (Pin 13/Pin 15): Top Gate Drive. This pin drives the gate of the top N-channel MOSFET. The TG driver draws power from the BOOST pin and returns to the SW pin, providing true floating drive to the top MOSFET.

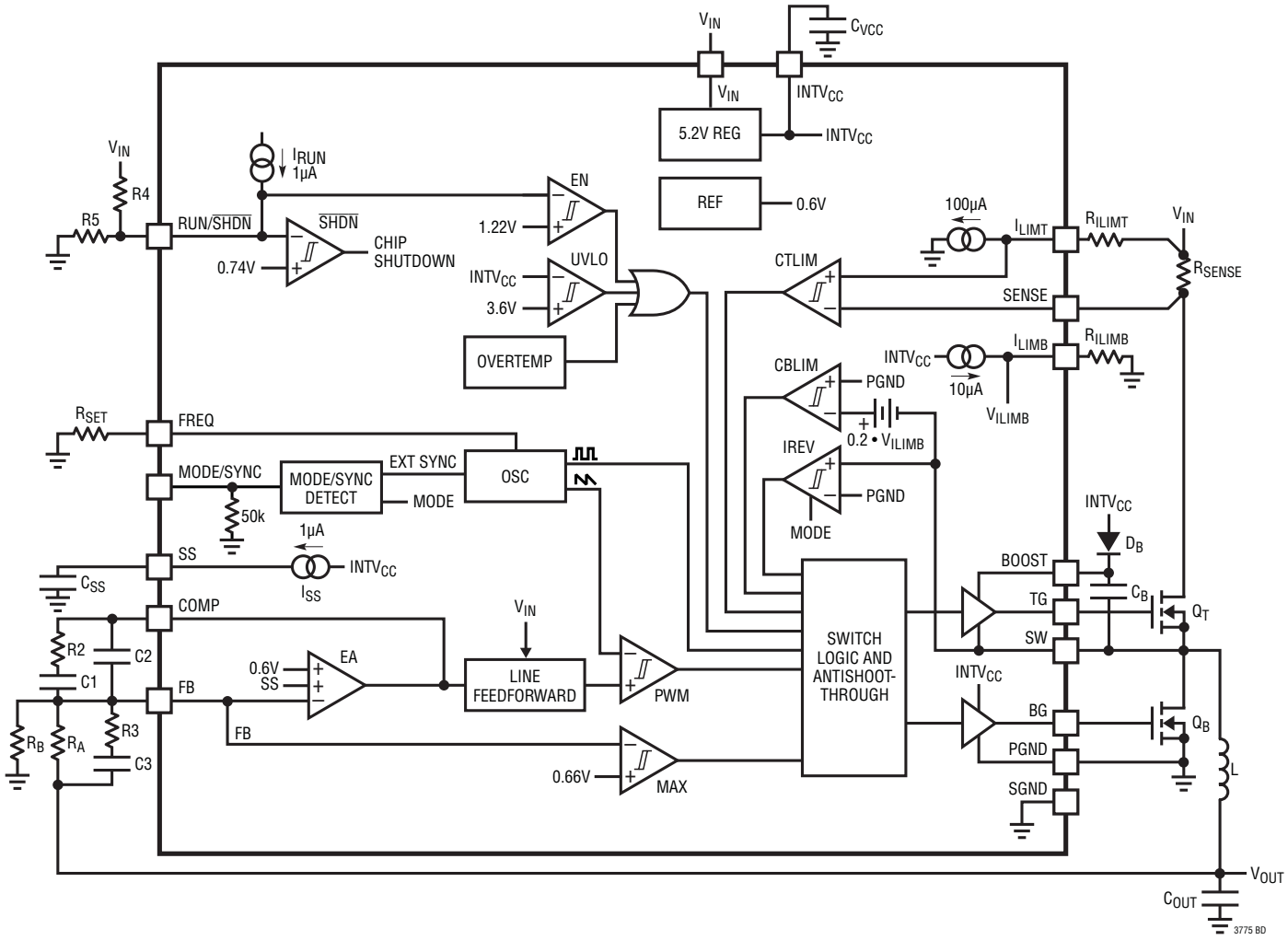
BOOST (Pin 14/Pin 16): Top Gate Driver Supply. This pin should be decoupled to SW with a 0.1µF low ESR ceramic capacitor. An external Schottky diode from $INTV_{CC}$ to BOOST creates a floating charge-pump supply at BOOST. No other external supplies are required.

MODE/SYNC (Pin 15/Pin 1): Pulse-Skipping Mode Enable/Sync Pin. This multifunction pin provides pulse-skipping mode enable/disable control and an external clock input for synchronization of the internal oscillator. Pulling this pin below 1.2V (DC) or driving it with an external logic-level synchronization signal disables pulse-skipping mode operation and forces continuous operation. Pulling the pin above 1.2V enables pulse-skipping mode operation. This pin has an internal 50k pull-down resistor connected to SGND.

RUN/$\overline{\text{SHDN}}$ (Pin 16/Pin 2): Enable/Shutdown Input. Pulling this pin above 1.22V enables the controller. Forcing this pin below 1.22V causes the driver outputs to pull low. Pulling this pin below 0.74V forces the LTC3775 into shutdown mode. While in shutdown, the $INTV_{CC}$ regulator and most internal circuitry turns off and the supply current drops below 14µA. This pin has an internal 1µA pull-up current that allows the LTC3775 to power up if this pin is left floating.

PGND (Exposed Pad Pin 17/Exposed Pad Pin 17): Power Ground. The BG driver returns to this pin. Connect PGND to the source of the bottom power MOSFET and the V_{IN} and $INTV_{CC}$ bypass capacitors. PGND is electrically isolated from SGND. The exposed pad of the QFN and MSOP packages is connected to PGND.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Operation (Refer to Block Diagram)

The LTC3775 is a constant frequency, voltage mode controller for DC/DC step-down converters. It is designed to be used in a synchronous switching architecture with two external N-channel MOSFETs. For circuit operation, please refer to the Block Diagram.

The LTC3775 uses voltage mode control in which the duty cycle is controlled directly by the error amplifier output. The error amplifier adjusts the voltage at the COMP pin by comparing the V_{FB} pin with the 0.6V internal reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference. The COMP voltage then rises, increasing the duty cycle until the LTC3775 output feedback voltage again matches the reference voltage.

In normal operation, the top MOSFET is turned on when the PWM comparator changes state and is turned off by the internal oscillator. The PWM comparator maintains the proper duty cycle by comparing the error amplifier output (after being "compensated" by the line feedforward multiplier) to a sawtooth waveform generated by the oscillator. When the top MOSFET is turned off, the bottom MOSFET is turned on until the next cycle begins, or if pulse-skipping mode operation is enabled, until the inductor current reverses as determined by the reverse current comparator.

Feedback Control

The LTC3775 senses the output voltage at V_{OUT} with an internal feedback op amp (see Block Diagram). This is a true op amp with a low impedance output, 80dB of open-loop gain and a 25MHz gain-bandwidth product. The positive input is connected to an internal 0.6V reference, while the negative input is connected to the FB pin. The output is connected to COMP, which is in turn connected to the line feedforward circuit and from there to the PWM generator.

At steady state, as shown in the Block Diagram, the output of the switching regulator is given the following equation

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_A}{R_B}\right)$$

Unlike many regulators that use a transconductance (g_m) amplifier, the LTC3775 is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows the feedback gain to be tightly controlled by external components. In addition, the voltage feedback amplifier allows flexibility in choosing pole and zero locations. In particular, it allows the use of "Type 3" compensation, which provides a phase boost at the LC pole frequency and significantly improves the control loop phase margin.

In a typical LTC3775 circuit, the feedback loop consists of the line feedforward circuit, the modulator, the external inductor, the output capacitor and the feedback amplifier with its compensation network. All these components affect loop behavior and need to be accounted for in the loop compensation. The modulator consists of the PWM generator, the output MOSFET drivers and the external MOSFETs themselves. The modulator gain varies linearily with the input voltage. The line feedforward circuit compensates for this change in gain, and provides a constant gain from the error amplifier output to the inductor input regardless of input voltage. From a feedback loop point of view, the combination of the line feedforward circuit and the modulator looks like a linear voltage transfer function from COMP to the inductor input and has a gain roughly equal to 30V/V. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll-off at the output with 180° phase shift. This roll-off is what filters the PWM waveform, resulting in the desired DC output voltage, but this phase shift causes stability issues in the feedback loop and must be frequency compensated. At higher frequencies, the reactance of the output capacitor approaches its ESR, and the roll-off due to the capacitor stops, leaving –20dB/decade and 90° of phase shift.

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Figure 1 shows a Type 3 amplifier. The transfer function of this amplifier is given by the following equation:

$$\frac{V_{COMP}}{V_{OUT}} = \frac{-\left(1+sR2C1\right)\left[1+s(R_A+R3)C3\right]}{sR_A\left(C1+C2\right)\left(1+s(C1||C2)R2\right)\left(1+sC3R3\right)}$$

The RC network across the error amplifier and the feedforward components R3 and C3 introduce two pole-zero pairs to obtain a phase boost at the system unity-gain frequency, f_C. In theory, the zeros and poles are placed symmetrically around f_C, and the spread between the zeros and the poles is adjusted to give the desired phase boost at f_C. However, in practice, if the crossover frequency is much higher than the LC double-pole frequency, this method of frequency compensation normally generates a phase dip within the unity bandwidth and creates some concern regarding conditional stability.

If conditional stability is a concern, move the error amplifier's zero to a lower frequency to avoid excessive phase dip. The following equations can be used to compute the feedback compensation component values:

f_{SW} = switching frequency

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

choose:

$$f_C = \text{crossover frequency} = \frac{f_{SW}}{10}$$

$$f_{Z1(ERR)} = f_{LC} = \frac{1}{2\pi R2C1}$$

$$f_{Z2(RES)} = \frac{f_C}{5} = \frac{1}{2\pi\left(R_A+R3\right)C3}$$

$$f_{P1(ERR)} = f_{ESR} = \frac{1}{2\pi R2(C1||C2)}$$

$$f_{P2(RES)} = 5f_C = \frac{1}{2\pi R3C3}$$

Required error amplifier gain at frequency f_C:

$$A_{V(CROSSOVER)}$$

$$\approx 40\log\sqrt{1+\left(\frac{f_C}{f_{LC}}\right)^2} - 20\log\sqrt{1+\left(\frac{f_C}{f_{ESR}}\right)^2} - 20\log\left(A_{MOD}\right)$$

$$\approx 20\log\frac{R2}{R_A}\bullet\frac{\left(1+\frac{f_{LC}}{f_C}\right)\left(1+\frac{f_{P2(RES)}}{f_C}+\frac{f_{P2(RES)}-f_{Z2(RES)}}{f_{Z2(RES)}}\right)}{\left(1+\frac{f_C}{f_{ESR}}+\frac{f_{LC}}{f_{ESR}-f_{LC}}\right)\left(1+\frac{f_{P2(RES)}}{f_C}\right)}$$

where A_{MOD} is the modulator and line feedforward gain and is equal to:

$$A_{MOD} \approx \frac{V_{IN(MAX)}\bullet DC_{MAX}}{V_{SAW}} = \frac{40V\bullet 0.95}{1.25V} \approx 30V/V$$

Once the value of resistor R_A and the pole and zero locations have been decided, the values of C1, R2, C2, R3 and C3 can be obtained from the above equations.

Compensating a switching power supply feedback loop is a complex task. The applications shown in this data sheet show typical values, optimized for the power components shown. Though similar power components should suffice, substantially changing even one major power component may degrade performance significantly. Stability also may depend on circuit board layout. To verify the calculated component values, all new circuit designs should be prototyped and tested for stability.

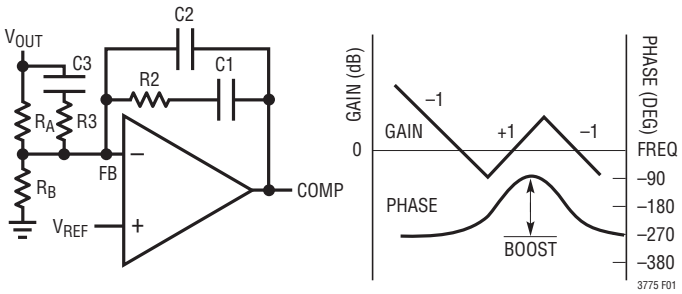

Figure 1. Type 3 Amplifier Compensation

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Output Overvoltage Protection

An overvoltage comparator, MAX, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Run/Shutdown

The LTC3775 can be put into a low power shutdown mode with quiescent current <14µA by pulling the RUN/$\overline{SHDN}$ pin below 0.74V. The RUN/$\overline{SHDN}$ pin can also be used as an accurate external UVLO (undervoltage lockout) input with a threshold of 1.22V. The driver outputs stay low if this pin is <1.22V. The external resistive divider R4 and R5 shown in the Block Diagram can be used to set the UVLO level based on V_{IN}. The V_{IN} voltage at which the switching starts is given by the following formula:

$$UVLO\ (Upper) = 1.22V \bullet (1 + R4/R5) - (1\mu A \bullet R4)$$

The RUN/$\overline{SHDN}$ pin has an internal 1µA pull-up for default turn-on if this pin is left floating. This 1µA pull-up current is included in the above UVLO calculation. When RUN/$\overline{SHDN}$ goes above 1.22V, this pull-up current is increased to 5µA. This provides some amount of hysteresis to the UVLO threshold. The lower UVLO level becomes:

$$UVLO\ (Lower) = 1.22V \bullet (1 + R4/R5) - (5\mu A \bullet R4)$$

So the amount of hysteresis is given by:

$$UVLO\ (Hysteresis) = 4\mu A \bullet R4$$

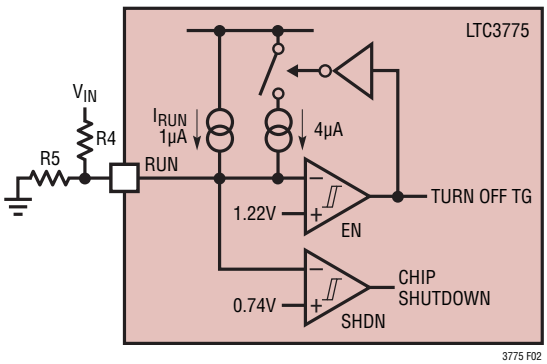

Figure 2. RUN Pin Control

Soft-Start

The LTC3775 includes a soft-start circuit that provides a smooth output voltage ramp during start-up. The SS pin requires an external capacitor, C_{SS}, to GND with the value determined by the required soft-start time. An internal 1µA current source charges C_{SS}. When the voltage on the SS pin is less than the 0.6V internal reference, the LTC3775 regulates the V_{FB} voltage to the SS pin voltage instead of the 0.6V reference. As the SS voltage rises linearly from 0V to 0.6V and beyond, the output voltage, V_{OUT}, rises smoothly from zero to its final value. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = \frac{0.9 \bullet C_{SS}}{1\mu A}$$

The SS pin is pulled low in the following conditions: during an LDO undervoltage condition ($INTV_{CC}$ < 3.6V), during shutdown (RUN pin < 1.22V), during an overtemperature condition (T_J > 165°C) and during current limit.

If either the top or bottom current limit comparator trips, the SS pin is pulled low until the inductor current regulates at around the current limit setting. Once the fault is cleared, SS will start charging up allowing the duty cycle and output voltage to increase gradually. **Due to the current limit action on the SS pin, it is important to avoid an overcurrent condition during start-up of the power supply, or V_{OUT} will fail to start up properly.**

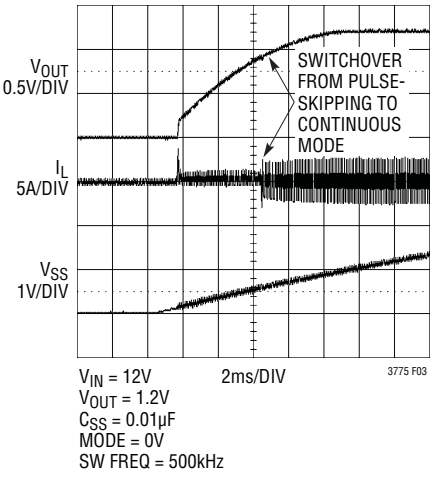

Figure 3. Typical Start-Up Waveform for a Buck Converter Using the LTC3775

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To prevent discharging a pre-biased V_{OUT}, the LTC3775 always starts switching in pulse-skipping mode up to SS = 0.54V, regardless of the mode selected by the MODE/SYNC pin. Thus if V_{OUT} > 0V during power-up, V_{OUT} will remain at the pre-biased voltage (if there is no load) until the SS voltage catches up with V_{OUT}, after which V_{OUT} will track the SS ramp. The LTC3775 reverts to the selected mode once SS > 0.54V.

Constant Switching Frequency

The internal oscillator can be programmed from 250kHz to 1MHz with an external resistor from the FREQ pin to ground, in order to optimize component size, efficiency and noise for the specific application. The internal oscillator can also be synchronized to an external clock connected to the MODE/SYNC pin and can lock to a range of ±20% of the programmed free-running frequency. When locked to an external clock, pulse-skipping mode operation is automatically disabled. Constant frequency operation offers a number of benefits: inductor and capacitor values can be chosen for a precise operating frequency and the feedback loop can be similarly tightly specified. Noise generated by the circuit will always be at known frequencies. Subharmonic oscillation and slope compensation, common headaches with constant frequency current mode switchers, are absent in voltage mode designs like the LTC3775.

Thermal Shutdown

The LTC3775 has a thermal detector that pulls the driver outputs low if the junction temperature of the chip exceeds 165°C. The thermal shutdown circuit has 25°C of hysteresis.

Current Limit

The LTC3775 includes an onboard cycle-by-cycle current limit circuit that limits the maximum output current to a user-programmed level. The current limit circuit consists of two comparators, CTLIM and CBLIM that monitor the voltage drop across the top and bottom MOSFETs respectively. Since the MOSFET's effective resistance, $R_{DS(ON)}$, is low during its on-time, the voltage drop from the drain to source is proportional to the current flow. Alternatively, for better accuracy, the topside current may be monitored with a sense resistor.

The benefit of having two comparators is to allow continuous monitoring and cycle-by-cycle control of the inductor current regardless of the operating duty cycle. In high duty cycle operation the top MOSFET, Q_T, is on most of the time. Thus, a high side comparator is necessary to limit the output current during high duty cycle operation. Architectures that contain only one comparator to monitor the low side MOSFET will not effectively limit the output current during high duty cycle operation. Conversely, during low duty cycle operation, a low side comparator is necessary to limit the output current. Another common current sensing scheme uses a sense resistor in series with the inductor to allow continuous monitoring. However, this scheme restricts the range of V_{OUT} due to the common mode range of the current limit comparator. The LTC3775 does not have this V_{OUT} restriction.

Figure 4 shows the current limit circuitry. The top current limit comparator, CTLIM monitors the current through the top MOSFET, Q_T, when TG is high. If the inductor current exceeds the current limit threshold when Q_T is on, Q_T turns off immediately and the bottom MOSFET, Q_B, turns on. The SENSE pin is the input for CTLIM. For applications where

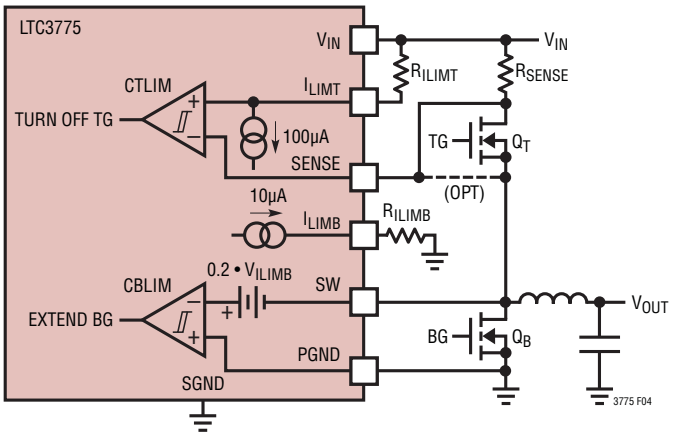

Figure 4. LTC3775 Current Limit Circuit

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the upper MOSFET's $R_{DS(ON)}$ is used to sense current, connect the SENSE pin to the source of Q_T (the SW node). Alternatively, for accurate current sensing, connect this pin to a sense resistor located at the drain of Q_T. The reference input of CTLIM is connected to the I_{LIMT} pin. Connect an external resistor, R_{ILIMT}, from the I_{LIMT} pin to V_{IN} to set the the current limit threshold. The voltage at the SENSE pin drops as the inductor current increases. CTLIM trips if the voltage at the SENSE pin goes below the voltage at the I_{LIMT} pin causing TG to pull low and turn off Q_T.

The bottom current limit comparator, CBLIM, monitors the current through the bottom MOSFET, Q_B, when BG is high. If the inductor current exceeds the current limit threshold when Q_B is on, Q_B remains on until the current drops below the threshold. The SW pin is the input for CBLIM. The reference input to CBLIM is derived from the voltage at the I_{LIMB} pin. Connect an external resistor, R_{ILIMB}, from the I_{LIMB} pin to SGND to set the current limit threshold.

The inductor current flows from PGND to SW when Q_B is on (for a positive load current). The SW node is therefore a negative voltage. The LTC3775 inverts the voltage at the SW pin before comparing it with the attenuated voltage (5×) at the I_{LIMB} pin. BG stays high once CBLIM trips and TG remains low until the inductor current drops below the threshold. Figure 5 shows typical waveforms during output overload.

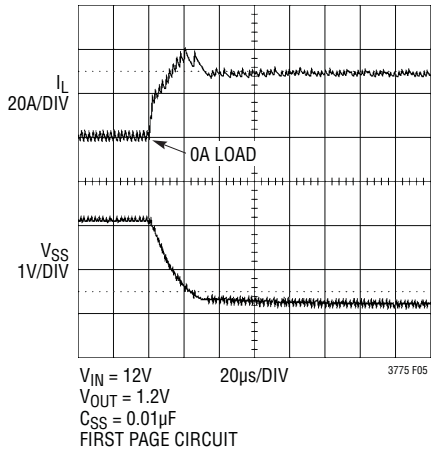

Figure 5. Typical Waveforms During Output Overload

Current Limit Blanking Time

The LTC3775 current limit circuit features a short blanking time following low-to-high and high-to-low transitions at the SW node. This prevents false tripping of the current limit circuit if there is ringing on the SW node.

When the top gate, TG, goes high, the topside comparator, CTLIM, waits for 200ns before turning on to monitor the SENSE voltage. Likewise, when the bottom gate, BG, goes high the bottom side comparator, CBLIM, waits for 200ns before turning on to monitor the SW voltage. This means that the minimum TG and BG pulse is slightly more than 200ns during current limit. These blanking times do not, however, limit the duty cycle capability of the control loop. The LTC3775 control loop is capable of operation with a TG on-time as low as 30ns.

If a sense resistor is employed on the top side, the LTC3775 automatically lowers the CTLIM blanking time from 200ns to 100ns. The CBLIM blanking time remains at 200ns. The blanking time can be reduced when a sense resistor is used because the SENSE pin connects to the drain of the top MOSFET which rings less than the SW node. The LTC3775 detects that a sense resistor is employed by checking that the SENSE pin stays high (equal to V_{IN}) when BG is high. If the SENSE pin is connected to the SW node, SENSE will be at 0V when BG is high.

The Current Sensing Input Pins

The SENSE and I_{LIMT} pins are inputs to the top current limit comparator, CTLIM. The top current limit threshold is set by the resistor, R_{ILIMT}, connected to the I_{LIMT} pin and the I_{LIMT} pin 100µA pull-down current. R_{ILIMT} should be placed close to the LTC3775 and the other end of R_{ILIMT} should run parallel with the SENSE trace to the Kelvin sense connection underneath the sense resistor, as shown in Figure 6. The sense resistor should be connected to the drain of the top power MOSFET and the V_{IN} node using short, wide PCB traces. Ideally, the top terminal of the sense resistors will be immediately adjacent to the positive terminal of the input capacitor, as shown in Figure 7a. This path is a part of the high di/dt loop formed by the sense resistor, top power MOSFET, inductor and output capacitor.

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Since the current limit comparator contains leading edge blanking, an external RC filter is not required for proper operation. However, an external filter can be designed by adding a capacitor across the SENSE and I_{LIMT} pins (C_F in Figure 7a). The filter component should be placed close to the SENSE and I_{LIMT} pins.

If $R_{DS(ON)}$ sensing is employed, the Kelvin sense connection should run from the SENSE pin and the R_{ILIMT} resistor to the source and drain terminals of the top power MOSFET respectively, as shown in Figure 7b. The external RC filter should not be added since the source terminal is switching.

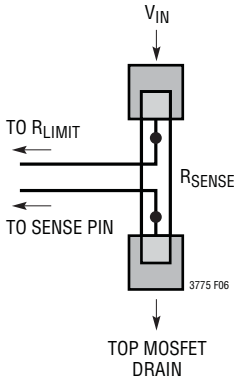

Figure 6. Kelvin SENSE Connection for Topside Current Limiting Sensing

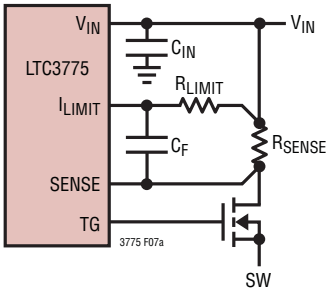

Figure 7a. External Filter for Topside Current Sensing

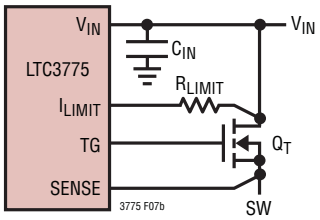

Figure 7b. Kelvin Connection for Topside $R_{DS(ON)}$ Sensing

The bottom side current limit threshold is set by the resistor, R_{ILIMB}, from the I_{LIMB} pin to SGND and the I_{LIMB} pin 10µA pull-up current. The voltage at ILIMB is attenuated 5× internally before it is applied to the input of bottom current limit comparator, CBLIM. This voltage must be quiet. Connect R_{ILIMB} from the I_{LIMB} pin to a quiet ground near the LTC3775 SGND pin. The other input of CBLIM is connected to the SW pin. The SW pin is also shared with the bottom gate driver and should be connected near the drain of the bottom MOSFET, Q_B.

Pulse-Skipping Mode

The LTC3775 can operate in one of two modes selectable with the MODE/SYNC pin: pulse-skipping mode or forced continuous mode. Pulse-skipping mode is selected when increased efficiency at light loads is desired, as shown in Figure 8. In this mode, the bottom MOSFET is turned off when inductor current reverses in order to minimize the efficiency loss due to reverse current flow. As the load current decreases (see Figure 9), the duty cycle is reduced to maintain regulation until the minimum on-time (50ns) is reached. When the load decreases below this point, the LTC3775 begins to skip cycles to maintain regulation. This reduces the frequency and improves efficiency by minimizing gate charge losses.

In forced continuous mode, the bottom MOSFET is always on when the top MOSFET is off, allowing the inductor current to reverse at low currents. This mode is less efficient due to switching, but has the advantages of better transient

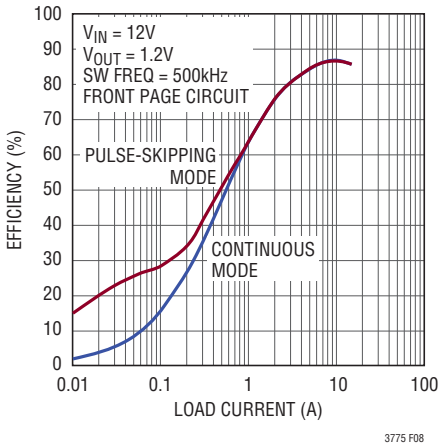

Figure 8. Efficiency in Pulse-Skipping/Forced Continuous Modes

APPLICATIONS INFORMATION

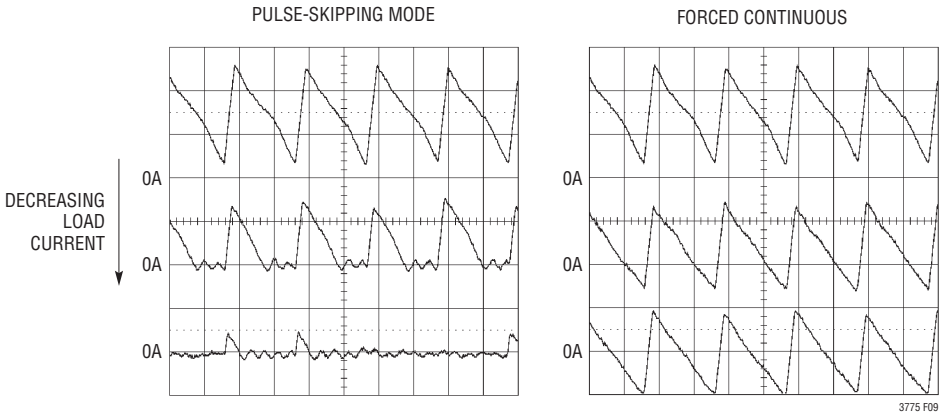

Figure 9. Comparison of Inductor Current Waveforms for Pulse-Skipping Mode and Forced Continuous Mode

response at low load currents, constant frequency operation, and the ability to maintain regulation when sinking current. See Figure 8 for a comparison of the efficiency at light loads for each mode.

In pulse-skipping mode, the LTC3775 reverse-current comparator, IREV, monitors the SW pin for zero crossing when the bottom gate, BG, is high. It turns off BG if the inductor current reverses and the SW voltage goes above GND. To prevent false tripping due to ringing on the SW node when BG is first turned on, there is a blanking time of 200ns similar to the bottom side current limit blanking. Under certain light load conditions, if the TG on-time is short, the inductor current may reverse during the IREV blanking time but the LTC3775 will only turn off BG after the blanking time.

In applications where a low value inductor is used, the high di/dt of the inductor ripple current together with the parasitic series inductance of the bottom MOSFET, Q_B, and PCB trace inductance creates an opposing voltage to the voltage drop across the $R_{DS(ON)}$ of QB. This can cause IREV to trip early, before the inductor current reverses. The parasitic series inductance of the PCB trace can be minimized by connecting the SW pin closer to the drain of Q_B.

$INTV_{CC}$ Regulator

The LTC3775 features a P-channel low dropout linear regulator (LDO) that supplies power to the $INTV_{CC}$ pin from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3775's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5.2V when V_{IN} is greater than 6.5V. The $INTV_{CC}$ pin must be bypassed to ground with a low ESR (X5R or better) ceramic capacitor of at least 4.7µF. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

An internal undervoltage lockout (UVLO) monitors the voltage on $INTV_{CC}$ to ensure that the LTC3775 has sufficient gate drive voltage. If the $INTV_{CC}$ voltage falls below the UVLO threshold of 3.1V, the gate drive outputs remain low.

Thermal Considerations

The LTC3775 is offered in a 3mm × 3mm QFN package (UD16) that has a thermal resistance $R_{TH(JA)}$ of 68°C/W and the MSOP (MSE16) package has a thermal resistance of 40°C/W. Both packages have a lead pitch of 0.5mm.

The regulator can supply up to 50mA of gate drive load current. The expected LDO load current can be calculated from the gate charge requirement of the external MOSFET:

$$I_{INTVCC} = (f_{SW}) \bullet (Q_{G(QT)} + Q_{G(QB)}) + 3.5mA$$

where:

3.5mA is the quiescent current of LTC3775

$Q_{G(QT)}$ is the total gate charge of the top MOSFET

$Q_{G(QB)}$ is the total gate charge of the bottom MOSFET

f_{SW} is the switching frequency

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The value of Q_G should come from the plot of V_{GS} vs Q_G in the Typical Performance Characteristics section of the MOSFET data sheet. The value listed in the electrical specifications may be measured at a higher V_{GS}, such as 10V, whereas the value of interest is at the 5V $INTV_{CC}$ gate drive voltage.

Care must be taken to ensure that the maximum junction temperature of the LTC3775 is never exceeded. The junction temperature can be estimated using the following equations:

$$P_{DISS} = V_{IN} \bullet I_{INTVCC}$$

$$T_J = T_A + P_{DISS} \bullet R_{TH(JA)}$$

As an example of the required thermal analysis, consider a buck converter with a 24V input voltage and an output voltage of 3.3V at 15A. The switching frequency is 500kHz and the maximum ambient temperature is 70°C. The power MOSFET used for this application is the Vishay Siliconix Si7884DP, which has a typical $R_{DS(ON)}$ of 7.5mΩ at V_{GS} = 4.5V and 5.5mΩ at V_{GS} = 10V. From the plot of V_{GS} vs Q_G, the total gate charge at V_{GS} = 5V is 18.5nC (the temperature coefficient of the gate charge is low). One power MOSFET is used for the top side and one for the bottom side. For the UD package:

$$I_{INTVCC} = 3.5mA + 2 \bullet 18.5nC \bullet 500kHz = 22mA$$

$$P_{DISS} = 24V \bullet 22mA = 528mW$$

$$T_J = 70°C + 528mW \bullet 68°C/W = 105.9°C$$

In this example, the junction temperature rise is 35.9°C. These equations demonstrate how the gate charge current typically dominates the quiescent current of the IC, and how the choice of the operating frequency and board heat sinking can have a significant effect on the thermal performance of the solution.

To prevent the maximum junction temperature from being exceeded, the input supply current of the IC should be checked when operating in continuous mode (heavy load) at maximum V_{IN}. A trade-off between the operating frequency and the size of the power MOSFETs may need to be made in order to maintain a reliable junction temperature.

Finally, it is important to verify the calculations by performing a thermal analysis of the final PCB using an infrared camera or thermal probe.

Operation at Low Supply Voltage

The LTC3775 has a minimum input voltage of 4.5V. The gate driver for the LTC3775 consists of a PMOS pull-up and an NMOS pull-down device, allowing the full $INTV_{CC}$ voltage to be applied to the gates during power MOSFET switching. Nonetheless, care should be taken to determine the minimum gate drive supply voltage ($INTV_{CC}$) in order to choose the optimum power MOSFETs. Important parameters that can affect the minimum gate drive voltage are the minimum input voltage ($V_{IN(MIN)}$), the LDO dropout voltage, the Q_G of the power MOSFETs, and the operating frequency.

If the input voltage V_{IN} is low enough for the $INTV_{CC}$ LDO to be in dropout, then the minimum gate drive supply voltage is:

$$V_{INTVCC} = V_{IN(MIN)} - V_{DROPOUT}$$

The LDO dropout voltage is a function of the total gate drive current and the quiescent current of the IC (typically 3.5mA). A curve of dropout voltage versus output current for the LDO is shown in Figure 10. The temperature coefficient of the LDO dropout voltage is approximately 6000ppm/°C. See the $INTV_{CC}$ Regulator and Thermal Considerations sections for information about calculating the total quiescent current.

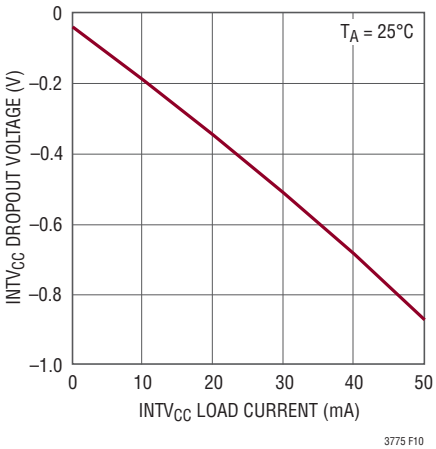

Figure 10. $INTV_{CC}$ LDO Dropout Voltage vs Current

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After the calculations have been completed, it is important to measure the gate drive waveforms and the gate driver supply voltage ($INTV_{CC}$ to PGND) over all operating conditions (low V_{IN}, nominal V_{IN} and high V_{IN}, as well as from light load to full load) to ensure adequate power MOSFET enhancement. Consult the power MOSFET data sheet to determine the actual $R_{DS(ON)}$ for the measured V_{GS}, and verify your thermal calculations by measuring the component temperatures using an infrared camera or thermal probe.

Operation at High Supply Voltage

At high input voltages, the LTC3775's internal LDO can dissipate a significant amount of power, which could cause the maximum junction temperature to be exceeded. Conditions such as a high operating frequency, or the use of more than one power MOSFET in parallel, could push the junction temperature rise to high levels. To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode at maximum V_{IN}. See the Thermal Considerations section for calculation of the maximum junction temperature.

Low Duty Cycle Operation

The LTC3775 uses a leading edge modulation architecture. Because the top MOSFET turns on when the PWM comparator trips, the top MOSFET minimum on-time is not dependent on the propagation delay of the PWM comparator; it is only limited by the internal delays of the gate drivers and the rise/fall time of the power MOSFET gate. This allows the LTC3775 to operate in very low duty cycle applications with a large step-down ratio. Figure 11 shows minimum on-time waveforms for forced continuous mode operation.

If pulse-skipping mode is selected, the LTC3775 allows the controller to skip pulses at light load, thereby reducing switching losses and improving the efficiency. Figure 12 shows waveforms of the minimum on-time in pulse-skipping mode.

If the TG on-time is less than the blanking time of the topside current limit comparator, CTLIM, the topside comparator never trips during normal operation. The blanking time

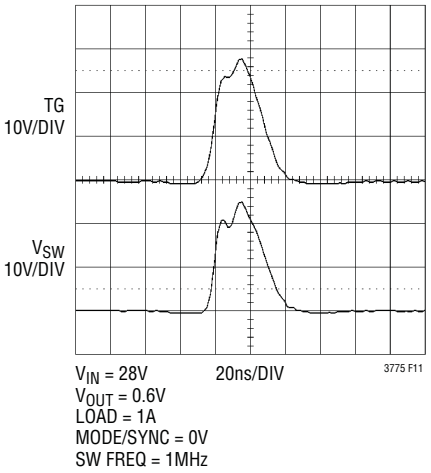

Figure 11. Minimum On-Time Waveforms in Forced Continuous Mode

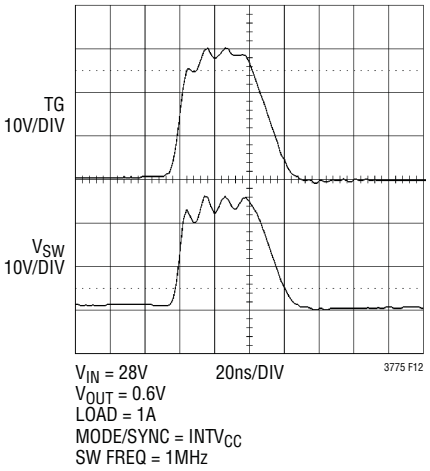

Figure 12. Minimum On-Time Waveforms in Pulse-Skipping Mode

is 200ns for $R_{DS(ON)}$ sensing and 100ns when a sense resistor is used. For TG on-times smaller than the topside blanking times, the LTC3775 relies on the bottom current limit comparator, CBLIM, to monitor the inductor current. If CBLIM trips, the LTC3775 starts to skip pulses and at the same time pulls down the soft-start capacitor to limit the duty cycle. If V_{OUT} drops sufficiently, the TG on-time can increase enough to turn on CTLIM and limit the peak inductor current. The minimum on-time of the application circuit can be calculated at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{f_{SW} \bullet V_{IN(MAX)}}$$

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High Duty Cycle Operation

The maximum duty cycle is limited by the LTC3775 internal oscillator reset time, the propagation delay of the PWM comparator and the BOOST pin supply refresh rate. The minimum off-time is typically 300ns.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the controller will enter dropout and attempt to turn on the top MOSFET continuously. To avoid depleting the charge on the bootstrap capacitor, C_B, the LTC3775 has an internal counter that turns on the bottom MOSFET every eight cycles for 200ns to refresh the bootstrap capacitor. Figure 13 shows maximum duty cycle operation with the 200ns BOOST pin supply refresh.

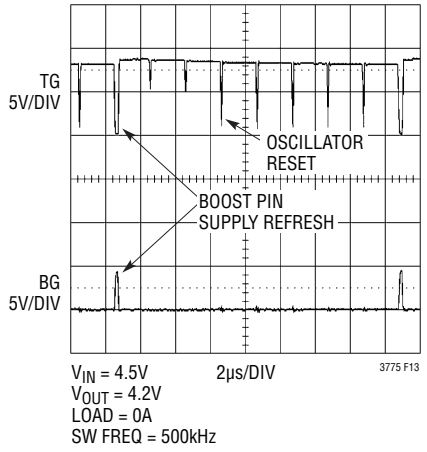

Figure 13. Maximum Duty Cycle Waveforms

EXTERNAL COMPONENTS SELECTION

Operating Frequency

The choice of operating frequency and inductor value is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses and gate charge losses. However, lower frequency operation requires more inductance for a given amount of ripple current, resulting in a larger inductor size and higher cost. If the ripple current is allowed to increase, larger output capacitors may be required to maintain the same output ripple. For converters with high step-down V_{IN} to V_{OUT} ratios, another consideration is the minimum on-time of the LTC3775 (see the Minimum On-Time Considerations section). A final consideration for operating frequency is that in noise-sensitive communications systems, it is often desirable to keep the switching noise out of a sensitive frequency band.

The LTC3775 uses a constant frequency architecture that can be programmed over a 250kHz to 1MHz range with a single resistor from the FREQ pin to ground, as shown in Figure 14. The nominal voltage on the FREQ pin is 1.22V, and the current that flows from this pin is used to charge and discharge an internal oscillator capacitor. The value of R_{SET} for a given operating frequency can be chosen from Figure 14 or from the following equation:

$$R_{SET}(k\Omega) = \frac{19500}{f(kHz)}$$

The oscillator can also be synchronized to an external clock applied to the MODE/SYNC pin with a frequency in the range of ±20% of the programmed free-running frequency set by the FREQ pin. In this synchronized mode, pulse-skipping mode operation is disabled. The clock high level must exceed 1.5V for a minimum of approximately 25ns to engage the feature. The bottom MOSFET will turn-on following the rising edge of the external clock.

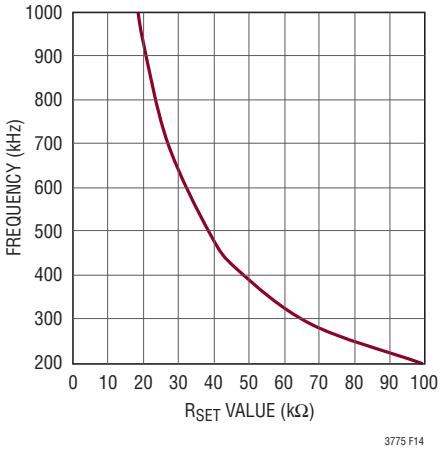

Figure 14. Frequency Set Resistor (R_{SET}) Value

Top MOSFET Driver Supply

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from

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$INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately V_{IN} + $INTV_{CC}$. The boost capacitor needs to store at least 100 times the gate charge required by the top MOSFET. In most applications a 0.1µF to 1µF X5R or X7R dielectric capacitor is adequate. The reverse breakdown of the Schottky diode, D_B, must be greater than $V_{IN(MAX)}$.

Power MOSFET Selection

The LTC3775 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the threshold voltage $V_{(GS)TH}$, breakdown voltage $V_{(BR)DSS}$, maximum current $I_{DS(MAX)}$, on-resistance $R_{DS(ON)}$ and input capacitance.

The gate drive voltage is set by the 5.2V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3775 applications. If the $INTV_{CC}$ voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered. Pay close attention to the $V_{(BR)DSS}$ specification because most logic-level MOSFETs are limited to 30V or less. The MOSFETs selected should have a $V_{(BR)DSS}$ rating greater than the maximum input voltage and some margin should be added for transients and spikes.

MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 15). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain voltage drops. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. To estimate the capacitance C_{MILLER}, take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

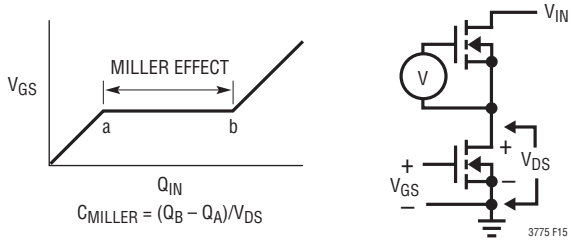

Figure 15. Gate Charge Characteristics

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Top Gate Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom Gate Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the top and bottom MOSFETs at maximum output current are given by:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}{}^2\right)\left(\rho_{T(TOP)}\right)\left(R_{DS(ON)(MAX)}\right)$$

$$+V_{IN}{}^2\left(\frac{I_{OUT(MAX)}}{2}\right)\left(R_{DR}\right)\left(C_{MILLER}\right)\bullet$$

$$\left(\frac{1}{INTV_{CC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right)\bullet f_{SW}$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}{}^2\right)\left(\rho_{T(TOP)}\right)\left(R_{DS(ON)(MAX)}\right)$$

where:

R_{DR} = Effective top driver resistance

$V_{TH(IL)}$ = MOSFET data sheet specified typical gate threshold voltage at the specified drain current

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C_{MILLER} = Calculated Miller capacitance using the gate charge curve from the MOSFET data sheet

f_{SW} = Switching frequency

Both MOSFETs have conduction losses (I^2R) while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For V_{IN} < 12V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 12V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The bottom MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the bottom switch is on close to 100% of the period.

Schottky Diode Selection

An optional Schottky diode connected between the SW node (cathode) and the source of the bottom MOSFET (anode) conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing a charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed next to each other on the same layer of the PC board.

Input Capacitor Selection

The input bypass capacitor has three primary requirements: its ESR must be low to minimize the supply drop when the top MOSFETs turn on, its RMS current capability must be adequate to withstand the ripple current at the input, and its capacitance must be large enough to maintain the input voltage until the input supply can respond. Generally, a capacitor (particularly a non-ceramic type) that meets the first two parameters will have far more capacitance than is required to keep capacitance-based droop under control. The input capacitor's voltage rating should be at least 1.4 times the maximum input voltage.

In continuous mode, the source current of the top N-channel MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramics have high voltage coefficients of capacitance and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited surface mount applicability; and electrolytics' higher ESR and dryout may require several to be used in parallel. Sanyo OS-CON SVP, SVPD series; Sanyo POSCAP TQC series or aluminum electrolytic capacitors from Panasonic WA series or Cornel Dublilier SPV series, in parallel with a couple of high performance ceramic capacitors, can be used as an effective means of achieving low ESR and high bulk capacitance.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where ΔI_L is the inductor ripple current.

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ΔI_L may be calculated using the equation:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Since ΔI_L increases with input voltage, the output ripple voltage is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Manufacturers such as Sanyo, Panasonic and Cornell Dublilier should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has a good (ESR)(size) product. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to offset the effect of lead inductance.

In surface mount applications, multiple capacitors may have to be connected in parallel to meet the ESR or transient current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent output capacitor choices are the Sanyo POSCAP TPD, POSCAP TPB, AVX TPS, AVX TPSV, the Kemet T510 series of surface mount tantalums, Kemet AO-CAPs or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

Inductor Selection

The inductor in a typical LTC3775 application circuit is chosen based on the required ripple current, its size and its saturation current rating. The inductor should not be allowed to saturate below the hard current limit threshold.

The inductor value sets the ripple current, which is commonly chosen at around 40% of the anticipated full load current. Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency is obtained at low frequency with small ripple current. However, achieving high efficiency requires a large inductor and generates higher output voltage excursion during load transients. There is a trade-off between component size, efficiency and operating frequency. Given a specified limit for ripple current, the inductor value can be obtained using the following equation:

$$L = \frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko. See the Current Limit Programming section for calculation of the inductor saturation current.

Current Limit Programming

If current sensing is implemented with a sense resistor, the topside current limit can be programmed by setting R_{ILIMT} as follows:

$$R_{ILIMT} = CF \bullet R_{SENSE} \bullet \frac{I_{O(MAX)} + 0.5 \bullet \Delta I_L}{I_{LIMIT(MIN)}}$$

where:

R_{SENSE} = Sense resistor value

$I_{O(MAX)}$ = Maximum output current

ΔI_L = Inductor ripple current (refer to the Output Capacitor Selection section).

$I_{LIMT(MIN)}$ = I_{LIMT} pin minimum pull-down current of 90μA

CF = Correction factor to provide safety margin and account for R_{SENSE} tolerance; use a value of CF = 1.2 is reasonable.

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If topside MOSFET $R_{DS(ON)}$ sensing is used, the R_{ILIMT} value is calculated from the following equation:

$$R_{ILIMIT} = \rho_T \bullet R_{DS(ON)(QT)(MAX)} \bullet \frac{I_{O(MAX)} + 0.5 \bullet \Delta I_L}{I_{LIMIT(MIN)}}$$

$R_{DS(ON)(QT)(MAX)}$ is the maximum MOSFET on-resistance typically specified at 25°C. The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.5%/°C as shown in Figure 16. For a maximum junction temperature of 100°C, using a value ρ_T = 1.4 is reasonable.

The bottom side current limit can be programmed by setting R_{ILIMB} as follows:

$$R_{ILIMB} = 5 \bullet \rho_T \bullet R_{DS(ON)(QB)(MAX)} \bullet \frac{I_{O(MAX)} + 0.5 \bullet \Delta I_L}{I_{LIMB(MIN)}}$$

where $I_{LIMB(MIN)} = I_{LIMB}$ pin minimum pull-up current of 9µA.

The resulting values of R_{ILIMT} and R_{ILIMB} should be checked in an actual circuit to ensure that the current limit kicks in as expected. Circuits that use MOSFETs with low value $R_{DS(ON)}$ for current sensing should be checked carefully. The PCB trace resistance and parasitic inductance can significantly change the actual current limit threshold. Care should be taken to shorten the PCB trace at the SENSE, SW and PGND connections.

The current limit setting also determines the worst-case peak current flowing in the inductor during an overload condition. The inductor saturation current rating needs to be higher than the worst-case peak inductor current:

$$I_{L(SAT)} \geq \frac{I_{LIMT(MAX)} \bullet R_{ILIMT}}{R_{SENSE(MIN)}}$$

or

$$I_{L(SAT)} \geq \frac{I_{LIMT(MAX)} \bullet R_{ILIMT}}{R_{DSON(QT)(MIN)}}$$

or

$$I_{L(SAT)} \geq \frac{\left(0.2 \bullet I_{LIMB(MAX)}\right) \bullet R_{ILIMB}}{R_{DSON(QB)(MIN)}}$$

$I_{LIMT(MAX)}$ = I_{LIMT} pin maximum pull-down current of 110µA

$I_{LIMB(MAX)}$ = I_{LIMB} pin maximum pull-up current of 11µA

$R_{DS(ON)(QT)(MIN)}$ and $R_{DS(ON)(QB)(MIN)}$ are the power MOSFET minimum on-resistances. MOSFET data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ is the same percentage below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

The saturation current rating for the inductor should be determined at the maximum input voltage, maximum output current and the maximum expected core temperature. The saturation current ratings for most commercially available inductors drop at high temperature. To verify safe operation, it is a good idea to characterize the inductor's core/winding temperature under the following conditions: 1) worst-case operating conditions, 2) maximum allowable ambient temperature and 3) with the power supply mounted in the final enclosure. Thermal characterization can be done by placing a thermocouple in intimate contact with the winding/core structure, or by burying the thermocouple within the windings themselves.

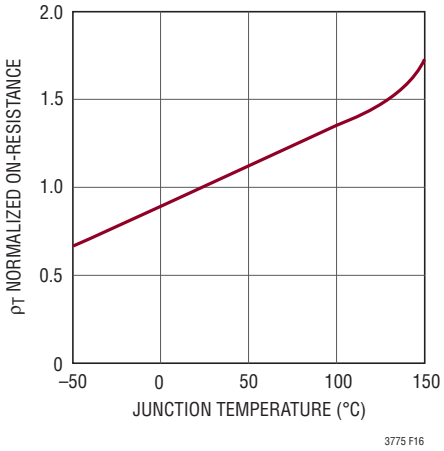

Figure 16. Typical MOSFET $R_{DS(ON)}$ vs Temperature

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MODE/SYNC Pin

The MODE/SYNC pin is a dual function pin that can be used to program the operating mode or to synchronize the switching frequency to an external clock. Pulse-skipping mode is enabled when the MODE/SYNC pin is above 1.2V. The mode is forced continuous when the pin is below 1.2V.

If this pin is left floating, an internal 50k pull-down resistor defaults the selection to forced continuous mode. During power-up, the LTC3775 overrides this mode selection and operates in pulse-skipping mode to prevent the discharge of a pre-biased output capacitor.

The internal LTC3775 oscillator can be synchronized to an external clock with a signal greater than 1.5V. A low-to-high transition on the MODE/SYNC pin resets the oscillator sawtooth waveform (high) and forces TG low (see Figure 17).The external oscillator frequency must be within ±20% of the frequency programmed by the R_{SET} resistor, or else the part will revert to free-running mode. The internal oscillator locks to the external clock after the second clock transition is received. When external synchronization is detected, the LTC3775 will operate in forced continuous mode.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3775. Check the following in your layout:

1. Keep the signal and power grounds separate. The signal ground consists of the LTC3775 SGND pin and the (–) terminal of V_{OUT}. The power ground consists of the optional Schottky diode anode, the source of the bottom side MOSFET, and the (–) terminal of the input capacitor. Connect the signal ground to the (–) terminal of the output capacitor. Also, try to connect the (–) terminal of the output capacitor as close as possible to the (–) terminals of the input capacitor.
2. The high di/dt loop formed by the top N-channel MOSFET, the bottom MOSFET and the C_{IN} capacitor should have short leads and PC trace lengths to minimize high frequency noise and voltage stress from inductive ringing.
3. Connect the drain of the topside MOSFET directly to the (+) plate of C_{IN}, and connect the source of the bottom side MOSFET directly to the (–) terminal of C_{IN}. This capacitor provides the AC current to the MOSFETs.
4. Place the ceramic C_{INTVCC} decoupling capacitor immediately next to the IC, between $INTV_{CC}$ and SGND. Likewise, the C_B capacitor should also be next to the IC between BOOST and SW.
5. Place the small-signal components away from high frequency switching nodes (BOOST, SW, TG and BG).
6. For optimum load regulation and true remote sensing, the top of the output resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC3775 in order to keep the high impedance FB node short.
7. For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC3775 is not shared with other converters. AC input current from another converter could cause substantial input voltage

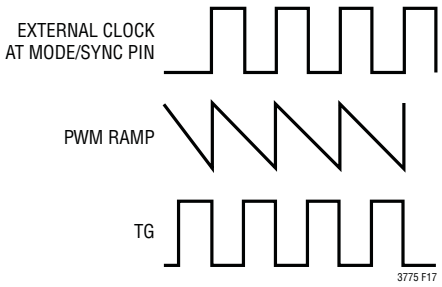

Figure 17. External Synchronization

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ripple, and this could interfere with the operation of the LTC3775. A few inches of PC trace or wire (L ≅ 100nH) between C_{IN} of the LTC3775 and the actual source V_{IN} should be sufficient to prevent input noise interference problems.

8. The top current limit programming resistor, R_{ILIMT}, should be placed close to the LTC3775 and the other end of R_{ILIMT} should run parallel to the SENSE trace to the Kelvin sense connection underneath the sense resistor.

9. The bottom current limit programming resistor, R_{ILIMB}, should be placed close to the LTC3775 and the other end of R_{ILIMB} should connect to SGND.

10. The SW pin should be connected to the drain of the bottom MOSFET.

Checking Transient Response

For all new LTC3775 PCB circuits, transient tests need to be performed to verify the proper feedback loop operation. The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet (ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing which would indicate a stability problem.

Measuring transient response presents a challenge in two respects: obtaining an accurate measurement and generating a suitable transient for testing the circuit. Output measurements should be taken with a scope probe directly across the output capacitor. Proper high frequency probing techniques should be used. Do not use the 6" ground lead that comes with the probe! Use an adapter that fits on the tip of the probe and has a short ground clip to ensure that inductance in the ground path doesn't cause a bigger spike than the transient signal being measured. The typical probe tip ground shield is spaced just right to span the leads of a typical output capacitor. In general, it is best to take this measurement with the 20MHz bandwidth limit on the oscilloscope turned on to limit high frequency noise. Note that microprocessor manufacturers typically specify ripple ≤20MHz, as energy above 20MHz is generally radiated (and not conducted) and does not affect the load even if it appears at the output capacitor.

Now that we know how to measure the signal, we need to have something to measure. The ideal situation is to use the actual load for the test, switching it on and off while watching the output. If this isn't convenient, a current step generator is needed. This generator needs to be able to turn on and off in nanoseconds to simulate a typical switching logic load, so stray inductance and long clip leads between the LTC3775 and the transient generator must be minimized.

Figure 18 shows an example of a simple transient generator. Be sure to use a noninductive resistor as the load element. Many power resistors use an inductive spiral pattern and are not suitable for use here. A simple solution is to take ten 1/4W film resistors and wire them in parallel to get the desired value. This gives a noninductive resistive load which can dissipate 2.5W continuously or 250W if pulsed with a 1% duty cycle, enough for most LTC3775 circuits. Solder the MOSFET and the resistor(s) as close to the output of the LTC3775 circuit as possible and set up the signal generator to pulse at a 100Hz rate with a 1% duty cycle. This pulses the LTC3775 with 100µs transients 10ms apart, adequate for viewing the entire transient recovery time for both positive and negative transitions while keeping the load resistor cool.

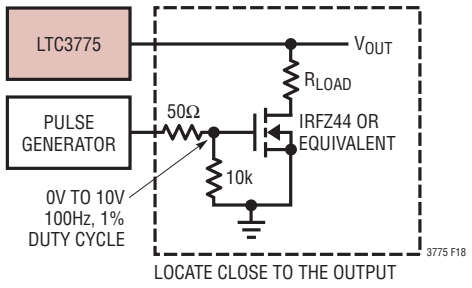


Figure 18. Transient Load Generator

APPLICATIONS INFORMATION

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 5V to 26V (12V nominal), V_{OUT} = 1.2V ±5%, $I_{OUT(MAX)}$ = 15A, f = 500kHz.

First, verify the minimum on-time which occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{1.2V}{(26V)(500kHz)} = 92.3ns$$

The minimum on-time is lower than the top current limit comparator blanking time of 100ns with sense resistor sensing. The controller will rely on the bottom MOSFET $R_{DS(ON)}$ sensing at high V_{IN}.

Next, verify the maximum duty cycle which occurs at minimum V_{IN}:

$$\text{Maximum Duty Cycle} = \frac{1.2V}{5V} = 24\%$$

This is below the LTC3775 maximum duty cycle of 90%.

Next, calculate R_{SET} to give the 500kHz operating frequency:

$$R_{SET} = \frac{19500}{500} = 39k$$

Next, choose the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \frac{1.2V}{(500kHz)(0.4)(15A)}\left(1-\frac{1.2}{26}\right) = 0.38\mu H$$

Select 0.36µH which is the nearest standard value.

The resulting maximum ripple current is:

$$\Delta I_L = \frac{1.2V}{(500kHz)(0.36\mu H)}\left(1-\frac{1.2V}{26V}\right) = 6.4A$$

Next, choose the top and bottom MOSFET switch. Since the drain of each MOSFET will see the full supply voltage 26V (max) plus any ringing, choose a 30V MOSFET to provide a margin of safety. Because the top MOSFET is on for a short time, a RENESAS RJK0305DPB ($R_{DS(ON)}$ = 13mΩ (max), $C_{MILLER} = Q_{GD}/10V$ = 150pF, $V_{GS(TH)}$ = 2.5V, θ_{JA} = 40°C/W) is sufficient. Check its power dissipation at current limit with = $\rho_{100°C}$ = 1.4:

$$P_{TOP} = \frac{1.2V}{26V}\left((15A)^2 \bullet 1.4 \bullet 13m\Omega\right) + (26V)^2\left(\frac{15A}{2}\right)(2.5\Omega)(150pF)\left(\left(\frac{1}{5.2-2.5}\right)+\frac{1}{2.5}\right)500kHz = 0.19W + 0.73W = 0.92W$$

And double check the assumed T_J in the MOSFET:

T_J = 70°C + (0.92W)(40°C/W) = 107°C

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary.

A RENESAS RJK0301DPB ($R_{DS(ON)}$ = 4mΩ (max), θ_{JA} = 40°C/W) is chosen for the synchronous MOSFET.

$$P_{BOT} = \frac{26V-1.2V}{26V}\left((15A)^2 \bullet 1.4 \bullet 4m\Omega\right) = 1.26W$$

And double check the assumed T_J in the MOSFET:

T_J = 70°C + (1.26W)(40°C/W) = 120°C

Next, the $INTV_{CC}$ LDO current is calculated:

I_{INTVCC} = (500kHz)(8nC + 32nC) + 3.5mA = 23.5mA

And double check the T_J in the LTC3775:

T_J = 70°C + (23.5mA)(26V)(68°C/W) = 112°C

Next, set the current limit resistors with a sense resistor of 3mΩ.

$$R_{ILIMT} = 1.2 \bullet 3m\Omega \bullet \frac{15A + 0.5 \bullet 6.4A}{90\mu A} = 728\Omega$$

$$R_{ILIMB} = 5 \bullet 1.4 \bullet 4m\Omega \bullet \frac{15A + 0.5 \bullet 6.4A}{9\mu A} = 56.62k$$

Use the next higher standard values of 732Ω and 57.6k.

APPLICATIONS INFORMATION

The worst-case peak inductor current based on a sense resistor tolerance of ±1% is

$$I_{L(SAT)} \geq \frac{110\mu A \bullet 732\Omega}{2.97m\Omega} = 27.1A$$

The input RMS current is highest at $V_{IN(MIN)}$ = 5V and $I_{OUT(MAX)}$ = 15A:

$$I_{RMS} \approx 15A \frac{\sqrt{1.2V(5V-1.2V)}}{5V} = 6.4A$$

C_{IN} is chosen for an RMS current rating of >6.4A at 85°C. For the output capacitor, two low ESR OS-CON capacitors (470µF/5mΩ each) are used to minimize output voltage changes due to inductor current ripple and load steps. The ripple voltage will be:

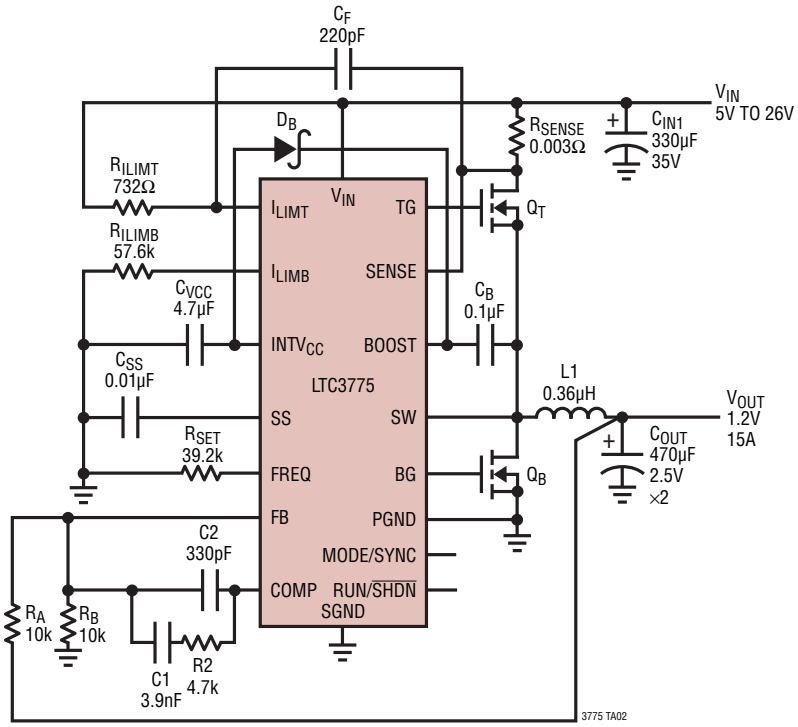
$$V_{OUT(RIPPLE)} = 6.4A \bullet \left(\frac{0.005}{2} + \frac{1}{8 \bullet 500kHz \bullet 470\mu F \bullet 2}\right)$$
$$= 17.7mV$$

However, a 0A to 15A load step will cause an output voltage change of at least:

$$\Delta V_{OUT(STEP)} = (15A)(0.0025\Omega) = 37.5mV$$

TYPICAL APPLICATIONS

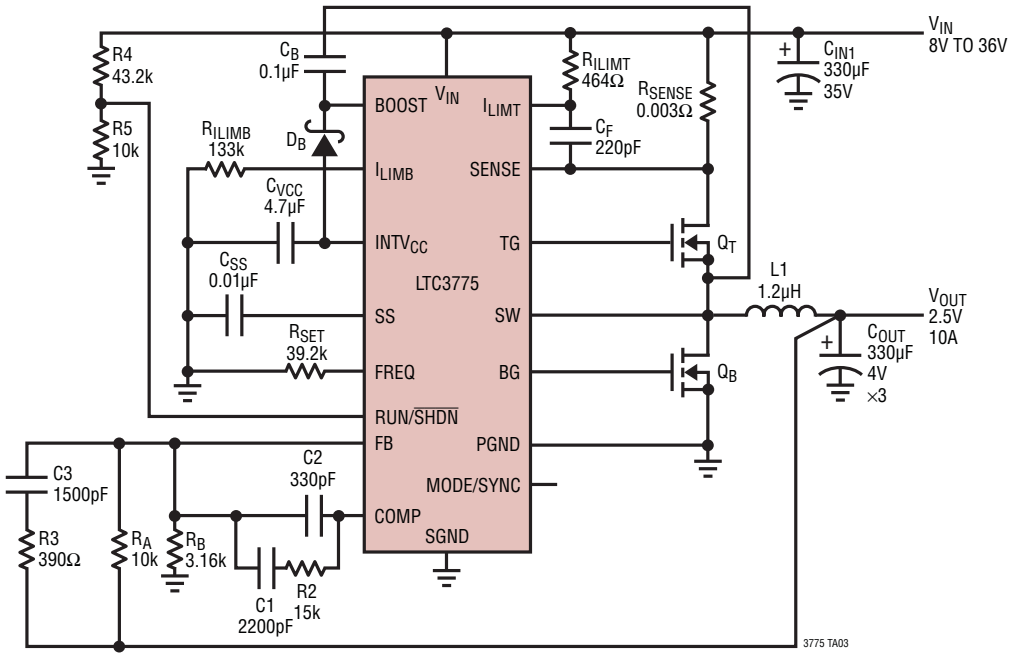
5V to 26V Input, 1.2V/15A Output at 500kHz



C_{OUT}: SANYO 2R5TPD470M5
D_B: CMDSH4E
L1: IHLP-4040DZ-ER-R36-M11
Q_B: RJK0301DPB-00-J0
Q_T: RJK0305DPB-00-J0

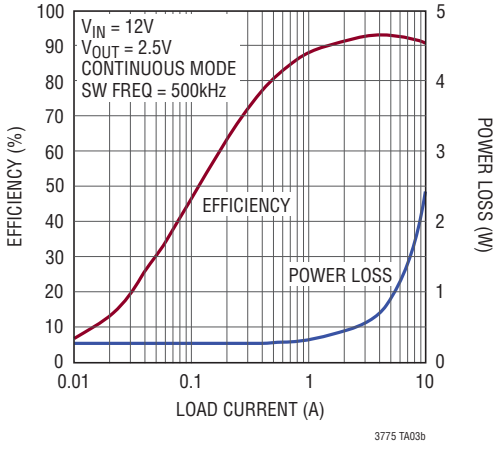
TYPICAL APPLICATIONS

8V to 36V Input, 2.5V/10A Output at 500kHz

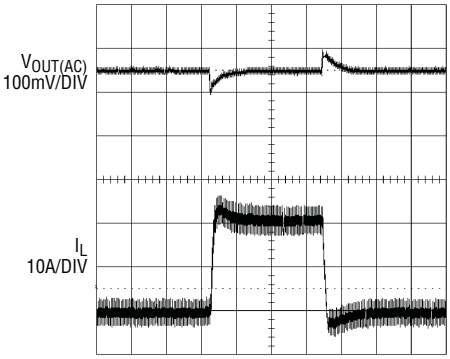


C_{OUT}: SANYO 4TPD330M
D_B: CMDSH4E
L1: TOKO FDA1254-1R2M
Q_B,Q_T: INFINEON BSZ097N04LS

Efficiency and Power Loss vs Load Current

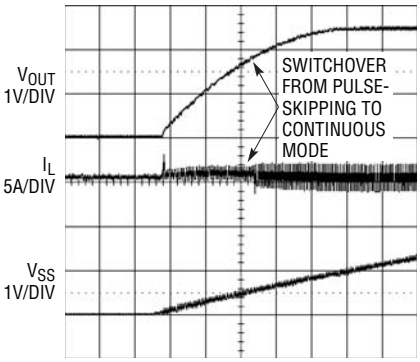


Load Step



V_{IN} = 12V
V_{OUT} = 2.5V
LOAD = 0A TO 10A TO 0A
MODE = 0V
SW FREQ = 500kHz

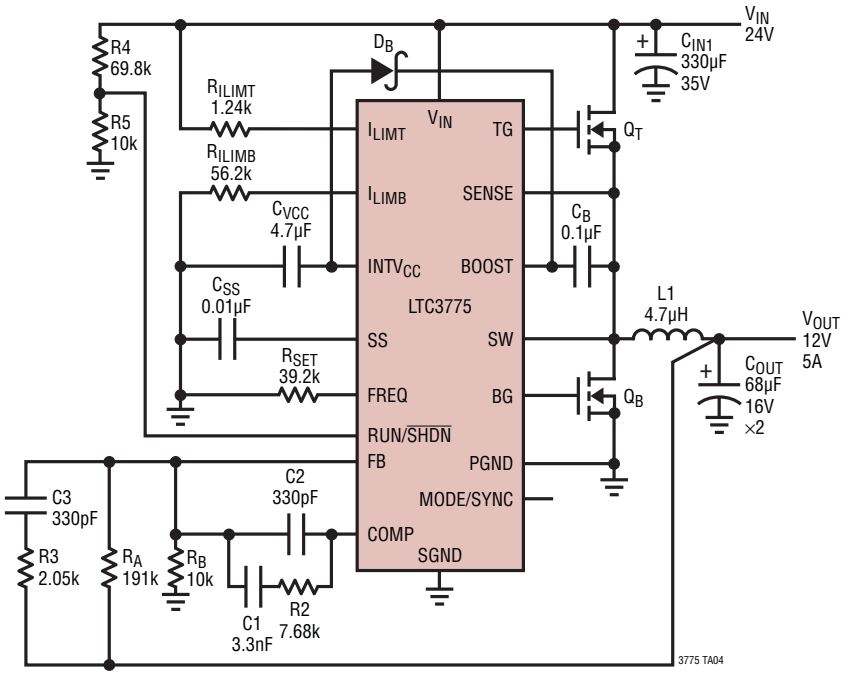
Start-Up



V_{IN} = 12V
V_{OUT} = 2.5V
CSS = 0.01µF
MODE = 0V
SW FREQ = 500kHz

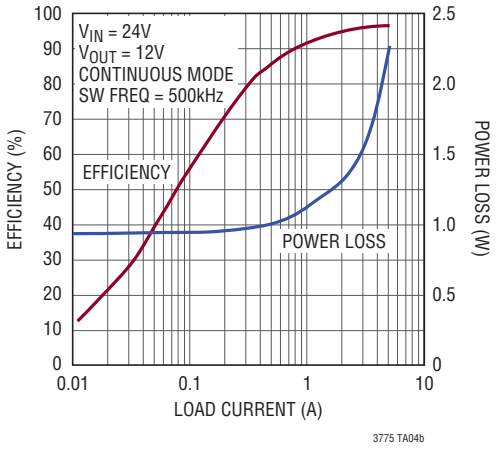
TYPICAL APPLICATIONS

24V Input, 12V/5A Output at 500kHz

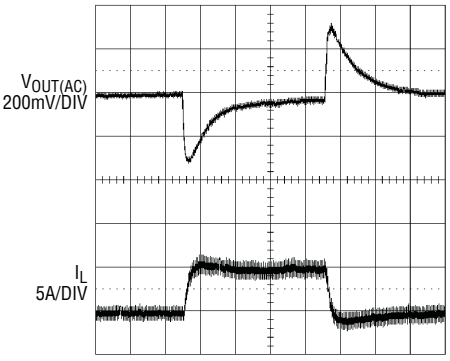


C_{OUT}: SANYO 16TQC68M
D_B: CMDSH4E
L1: IHLP-4040DZ-ER-4R7-M11
Q_B, Q_T: RJK0305DPB-00-JO

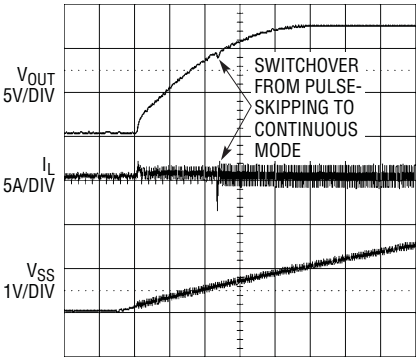
Efficiency and Power Loss vs Load Current



Load Step

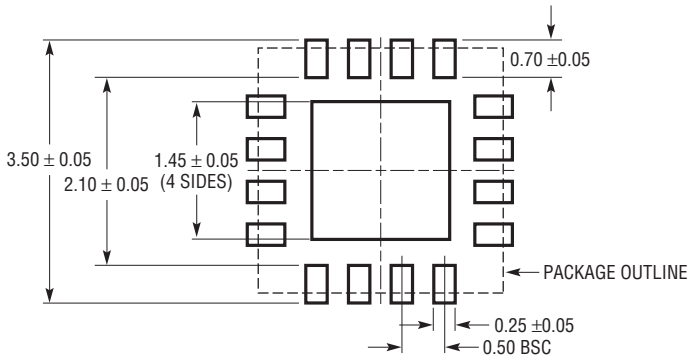


Start-Up

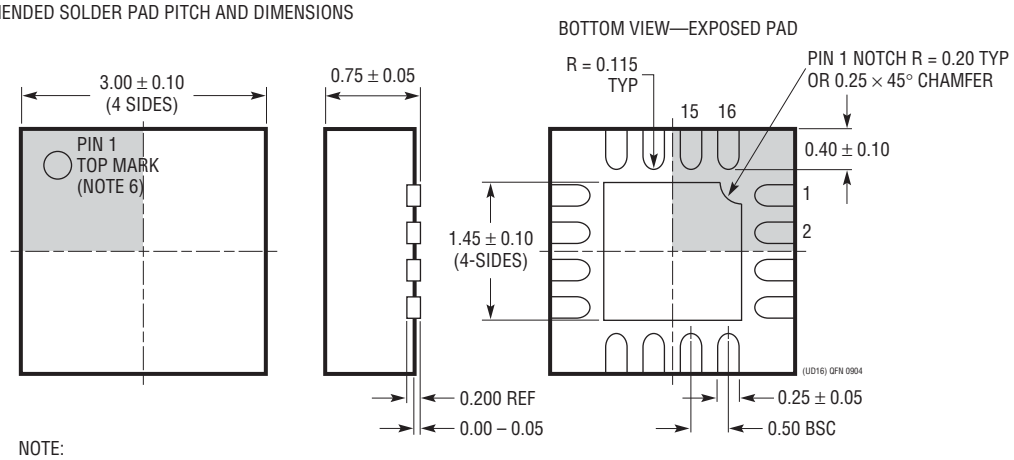


PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



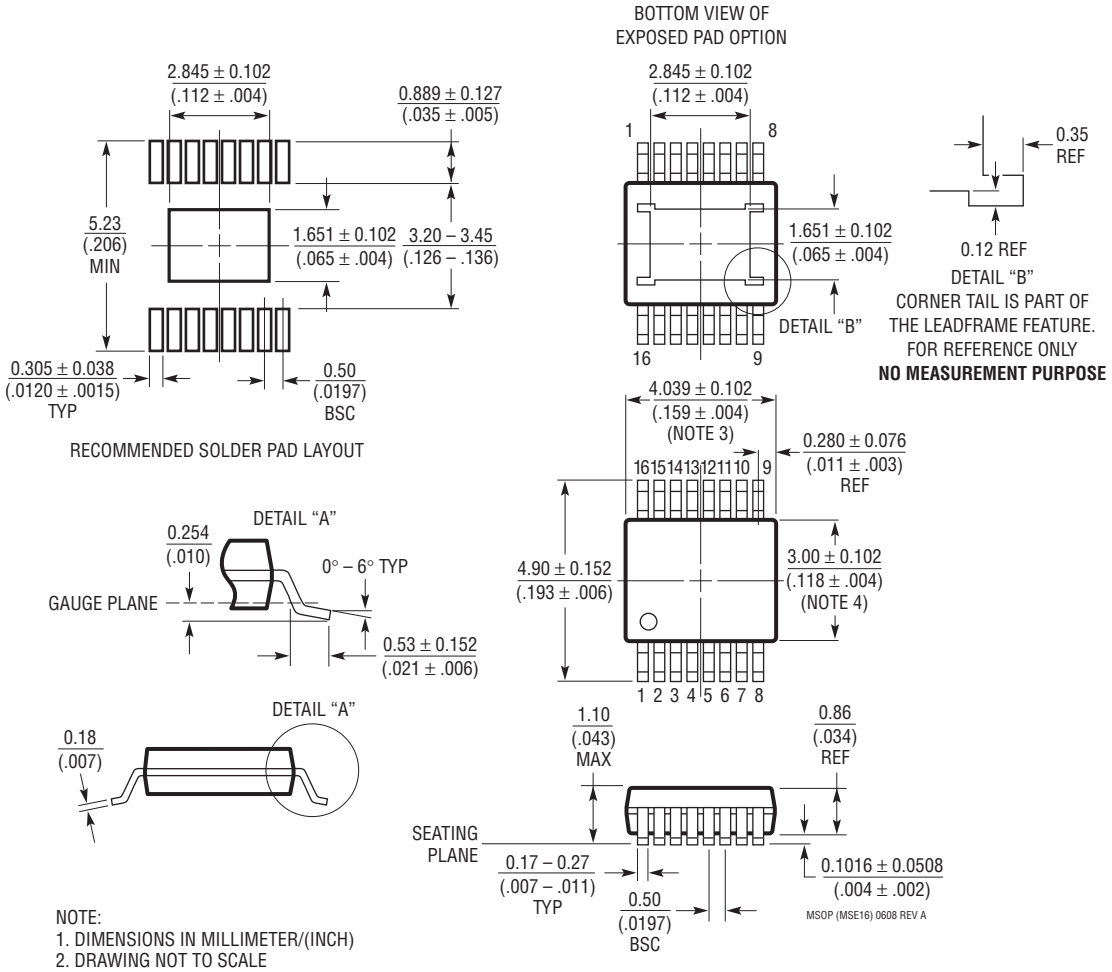
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev A)



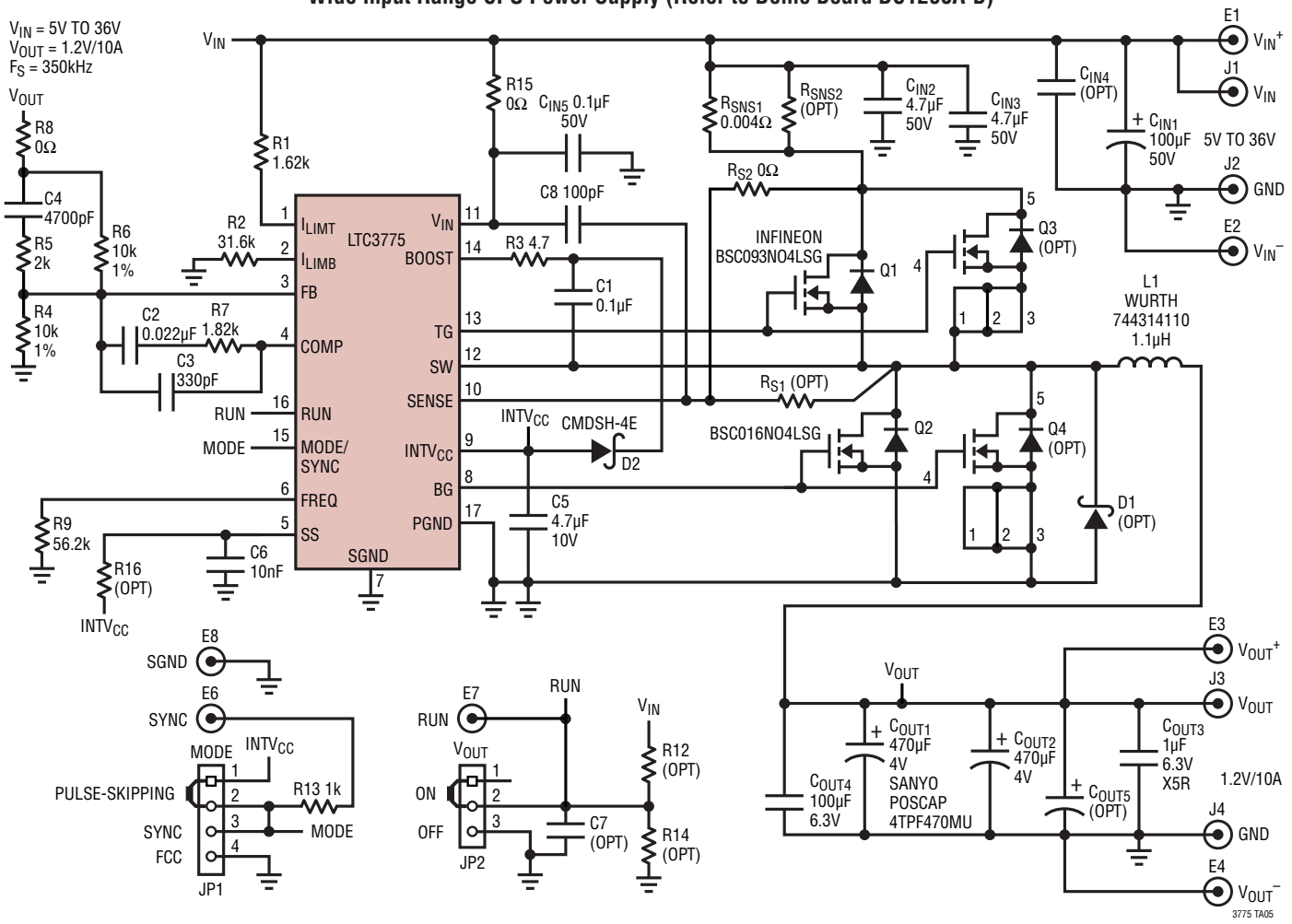
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/10	MSOP package added. Reflected throughout the data sheet.	1 to 34

TYPICAL APPLICATION

Wide Input Range CPU Power Supply (Refer to Demo Board DC1290A-B)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3854	Small Footprint Wide V_{IN} Range Synchronous Step-Down DC/DC Controller	Fixed 400kHz Operating Frequency, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5.25V, 2mm × 3mm QFN-12
LTC3851A/ LTC3851A-1	Wide V_{IN} Range Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Operating Frequency 250kHz to 750kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5.25V, MSOP-16E, 3mm × 3mm QFN-16, SSOP-16
LTC3878/ LTC3879	No R_{SENSE}™ Constant On-Time Synchronous Step-Down DC/DC Controller	Very Fast Transient Response, $t_{ON(MIN)}$ = 43ns, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 0.9V_{IN}, SSOP-16, MSOP-16E, 3mm × 3mm QFN-16
LTC3850/ LTC3850-1/ LTC3850-2	Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controllers, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed Operating Frequency 250kHz to 780kHz, 4V ≤ V_{IN} ≤ 30V, 0.8V ≤ V_{OUT} ≤ 5.25V
LTC3860	Dual, Multiphase Synchronous Step-Down DC/DC Controller with Diff Amp and 3-State Output Drive	Operates with Power Blocks, DRMOS Devices or External MOSFETs 3V ≤ V_{IN} ≤ 24V, $t_{ON(MIN)}$ = 20ns
LTC3853	Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed Operating Frequency 250kHz to 750kHz, 4V ≤ V_{IN} ≤ 24V, V_{OUT} Up to 13.5V

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