PO100HSTL50A

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Dual Differential LVDS/LVPECL/HSTL to LVTTL Translator
& Dual LVTTL/LVCMOS to Differential HSTL Translator

High Frequency Noise Canncellation Translator

FEATURES:

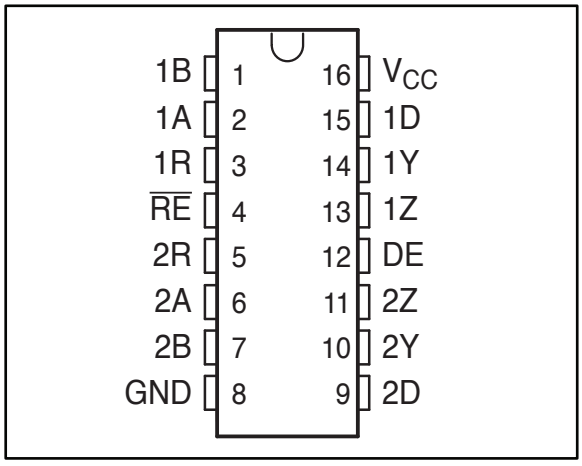
- Patented Technology
- Differential LVDS/LVPECL/HSTL to LVTTL Translator
  - Operating frequency up to 1GHz with 2pf load
  - Operating frequency up to 800MHz with 5pf load
  - Operating frequency up to 450MHz with 15pf load
  - Very low output pin to pin skew < 150ps
  - Propagation delay < 1.8ns max with 15pf load
- LVTTL/LVCMOS to Differential HSTL Translator
  - Operating frequency up to 1.65GHz with 5pf load
  - Operating frequency up to 500MHz with 15pf load
  - Very low output pin to pin skew < 100ps
  - Propagation delay < 1.4ns max with 15pf load
- 2.4V to 3.6V power supply
- Industrial temperature range: –40°C to 85°C
- Available in 16-pin 150ml SOIC package

DESCRIPTION:

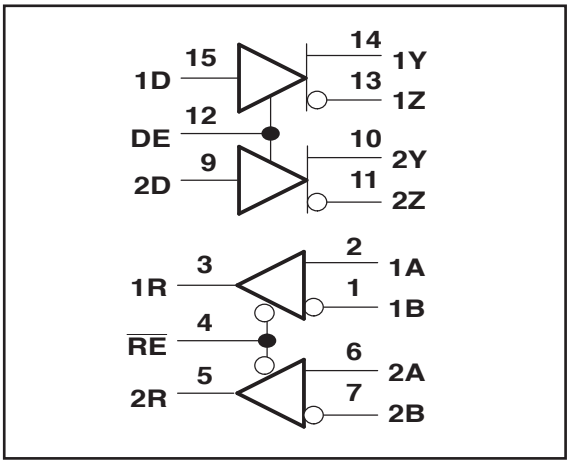
Potato Semiconductor's PO100HSTL50A is designed for world top performance using submicron CMOS technology to achieve 1GHz LVTTL output frequency with less than 1.8ns propagation delay and 1.65GHz HSTL output frequency with less than 1.4ns propagation delay.

The PO100HSTL50A is a low-skew, The small outline 16 pin package and the low skew design to make it ideal for applications which require the translation of a clock or a data signal.

Pin Configuration



Logic Block Diagram



Pin Description

RECEIVER INPUTS		RECEIVER OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
50 MV < V_{ID} < 50 mV	L	?
$V_{ID} \leq -50$ mV	L	L
Open	L	H
X	H	Z

DRIVER INPUTS		DRIVER OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

High Frequency Noise Canncellation Translator

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to Vcc	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input B Pullup Resistor			88		KΩ
$R_{PULLDOWN}$	Input A Pulldown Resistor			88		KΩ

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = Vcc	-	-	1	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

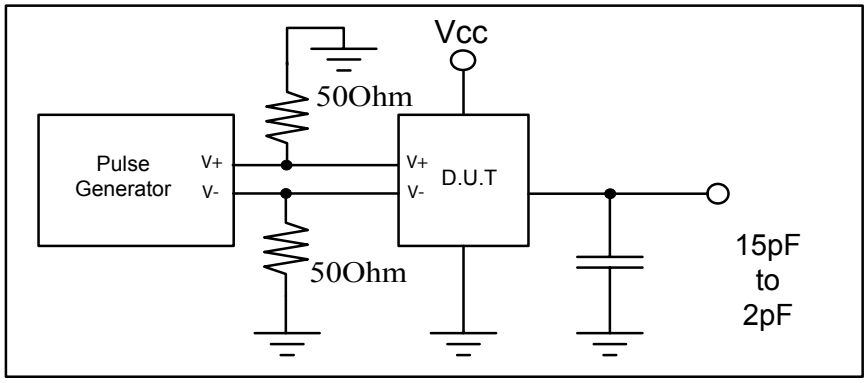
Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25•C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Receiver Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{PD}	Propagation Delay D to Output pair	CL = 15pF	1.8	ns
t_{PZH} or t_{PZL}	Output Enable Time	CL = 15pF	2.5	ns
t_{PHZ} or t_{PLZ}	Output Disable Time	CL = 15pF	2.5	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	150	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	300	ps
fmax	Input Frequency	CL =15pF	450	MHz
fmax	Input Frequency	CL = 5pF	800	MHz
fmax	Input Frequency	CL = 2pF	1000	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Circuit



Test Waveforms

FIGURE 1.
LVDS/ PECL/ ECL/ HSTL /DIFFERENTIAL INPUT WAVEFORM DEFINITIONS

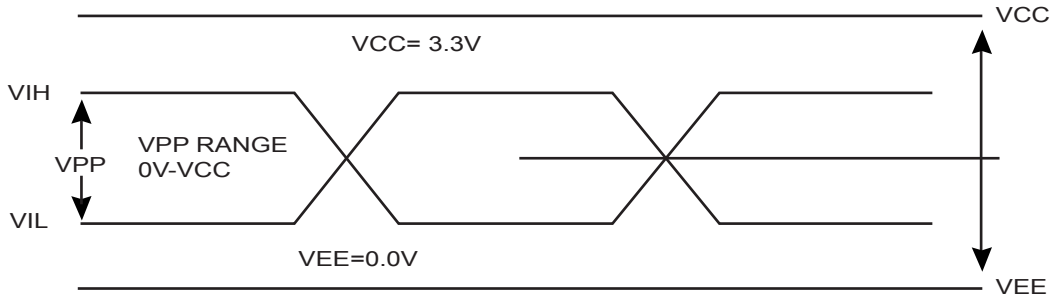


FIGURE 2.
LVTTL OUTPUT

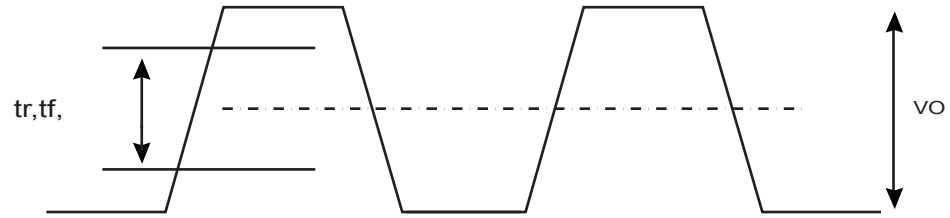
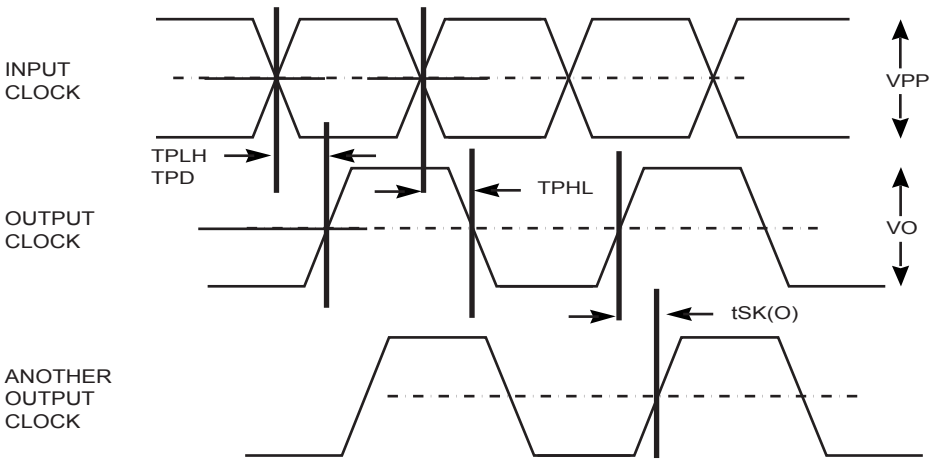


FIGURE 3.
Propogation Delay, Output pulse skew, and output-to-output skew for D to output

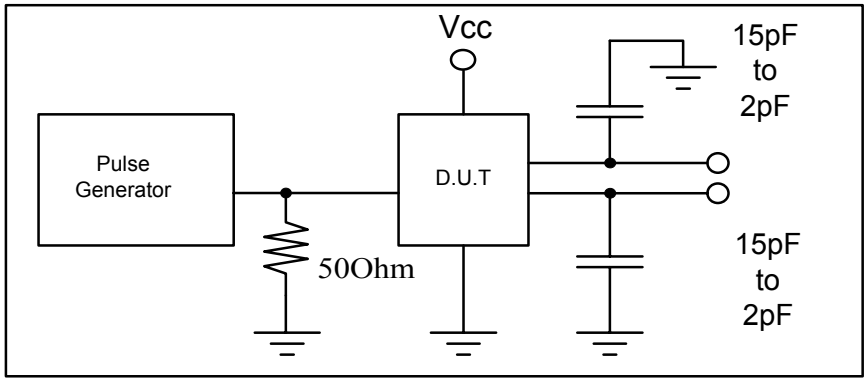


Driver Switching Characteristics

Symbol	Description	Test Conditions (1)	Typ	Max	Unit
t_{PD}	Propagation Delay D to Output pair	CL = 15pF		1.4	ns
t_{PZH} or t_{PZL}	Output Enable Time	CL = 15pF		2.5	ns
t_{PHZ} or t_{PLZ}	Output Disable Time	CL = 15pF		2.5	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V		0.8	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz		100	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz		250	ps
fmax	Input Frequency	CL =15pF		500	MHz
fmax	Input Frequency	CL = 5pF		1.65	GHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Circuit



Test Waveforms

FIGURE 1.
LVTTL/LVCMOS INPUT WAVEFORM DEFINITION

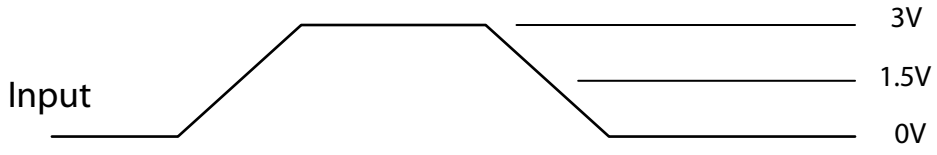


FIGURE 2.
HSTL OUTPUT

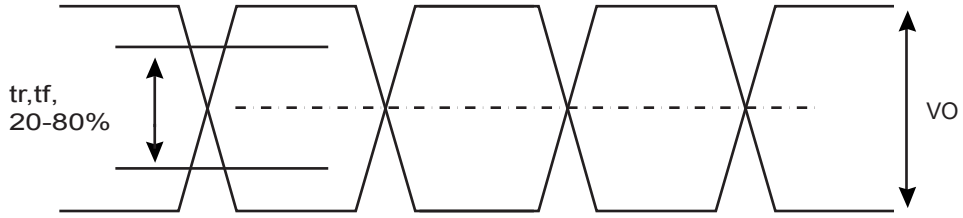
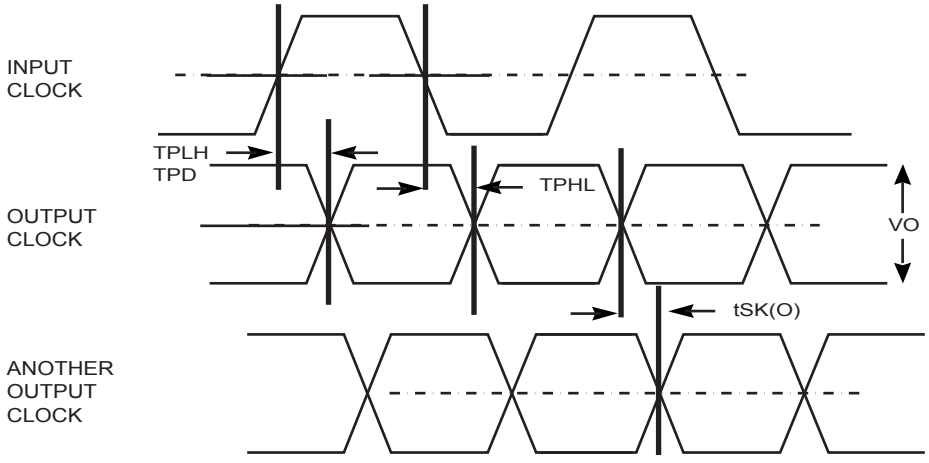
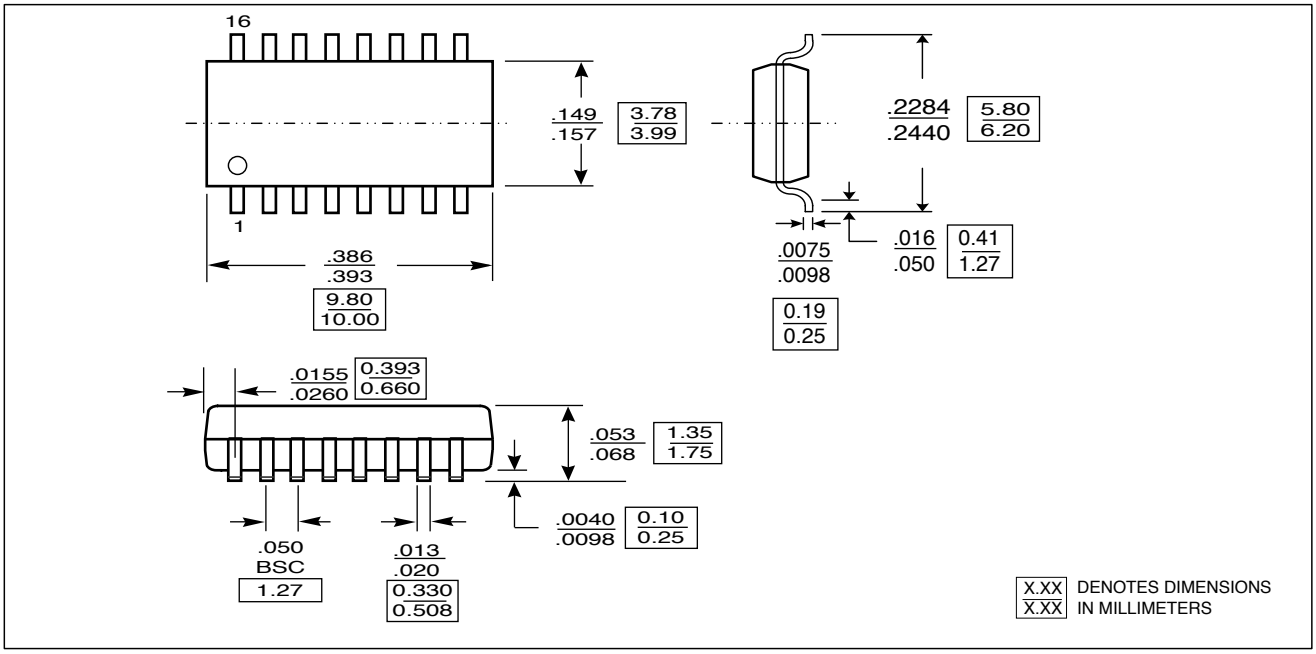


FIGURE 3.
Propogation Delay, Output pulse skew, and output-to-output skew for D to output pair



Packaging Mechanical Drawing: 16 pin SOIC



IC Ordering Information

Ordering Code	Package		Top-Marking	T_A
PO100HSTL50ASU for Tube	16-pin SOIC	Pb-free & Green	PO100HSTL50AS	-40°C to 85°C
PO100HSTL50ASR for Tape & Reel	16-pin SOIC	Pb-free & Green	PO100HSTL50AS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
S	SOIC 16	16	8	Top Left Corner	39 (12”)	3000	64 (20”)	48