ANALOG DEVICES

High Voltage Input Protection Device

Preliminary Technical Data

ADM1270

FEATURES

Controls supply voltages from 4 V to 60 V
Gate drive for low voltage drop reverse supply protection
Gate drive for P-channel FETs
In-rush current limiting control
Adjustable current limit
Foldback current limiting
Automatic retry or latch-off on current fault
Programmable current-limit timer for SOA
Power-good and Fault outputs
Analog UV and OV protection
16-lead 3x3mm LFCSP package
16-lead QSOP package

APPLICATIONS

Industrial Modules
Battery Powered/Portable Instrumentation

GENERAL DESCRIPTION

The ADM1270 is a current limiting controller that is intended to provide inrush current limiting and overcurrent protection for modular or battery powered systems. When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1270 is designed to control the in-rush current during powering on of a system via an external P-channel FET.

FUNCTIONAL BLOCK DIAGRAM

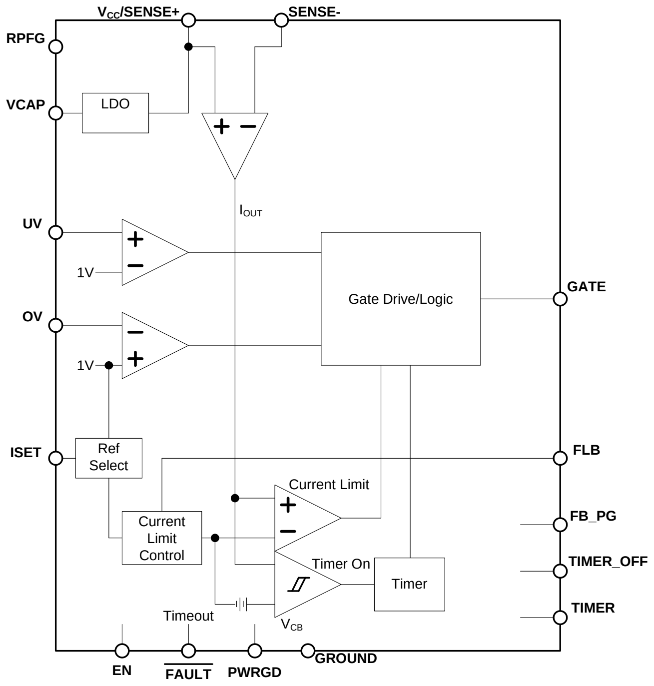

Figure 1.

To protect the system from a reverse polarity input supply, there is a provision made to control an additional external P-channel FET. This feature is used to prevent reverse current flow that could damage the load or the ADM1270.

The ADM1270 is available in a 3x3 16-lead LFCSP and a 16-lead QSOP package.

Rev. PrE

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REVISION HISTORY

SPECIFICATIONS

V_{CC}/V_{SENSE+} = 4 V to 60 V, $V_{SENSE} = (V_{SENSE+} - V_{SENSE-})$ = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range	V_{CC}	4		60	V	
Quiescent Current	I_{CC}		360	500	µA	GATE on
UV PIN						
Input Current	I_{UV}			100	nA	UV ≤ 5.5 V; T_A = −40°C to +85°C
Input Current	I_{UV}			1	µA	UV ≤ 5.5 V; T_A = −40°C to +125°C
UV Threshold	UV_{TH}	0.99	1.0	1.01	V	UV falling
UV Threshold Hysteresis	UV_{HYST}	50	60	70	mV	
UV Glitch Filter	UV_{GF}	4		7	µs	50 mV overdrive
UV Propagation Delay	UV_{PD}		5	8	µs	UV low to GATE pull-down active
OV PIN						
Input Current	I_{OV}			100	nA	OV ≤ 5.5 V; T_A = −40°C to +85°C
Input Current	I_{OV}			1	µA	OV ≤ 5.5 V; T_A = −40°C to +125°C
OV Threshold	OV_{TH}	0.99	1.0	1.01	V	OV rising
OV Threshold Hysteresis	OV_{HYST}	20	30	40	mV	
OV Glitch Filter	OV_{GF}	0.5		1.5	µs	50 mV overdrive
OV Propagation Delay	OV_{PD}		1	2	µs	OV high to GATE pull-up active
SENSE−						
Input Current	I_{SENSE-}		40	80	µA	SENSE− = 60 V
VCAP PIN						
Internally Regulated Voltage	V_{VCAP}	3.546	3.6	3.654	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
Undervoltage Lockout Rising	$UVLO_{RISE}$			3.4	V	V_{CC} rising
Undervoltage Lockout Falling	$UVLO_{FALL}$	3.0			V	V_{CC} falling
Undervoltage Hysteresis	$UVLO_{HYST}$		210		mV	
ISET PIN						
Reference Select Threshold	$V_{ISETRSTH}$	2.55	2.6	2.65	V	If $V_{ISET} > V_{ISETRSTH}$, an internal 1 V reference (V_{CLREF}) is used
Internal Reference	V_{CLREF}		2		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier	AV_{CSAMP}		40		V/V	Accuracies included in total sense voltage accuracies
Input Current	I_{ISET}			100	nA	V_{ISET} ≤ VCAP V; T_A = −40°C to +85°C
Input Current	I_{ISET}			1	µA	V_{ISET} ≤ VCAP V; T_A = −40°C to +125°C
RPFG PIN						
Reverse Protection FET Gate Drive Voltage	V_{RPFG}		0		V	Vcc ≤ 10V
	ΔV_{RPFG}	10	12	14	V	$\Delta V_{RPFG} = V_{CC} - V_{RPFG}$; 60 V ≥ V_{CC} ≥ 14 V; I_{RPFG} ≤ 5 µA
RPFG Pull-Dn (On) Current	I_{RPFGDN}	7	10	13	µA	V_{RPFG} = Vcc V
GATE PIN						
Gate Drive Voltage	ΔV_{GATE}					$\Delta V_{GATE} = V_{CC} - V_{GATE}$
		10	12	14	V	60 V ≥ V_{CC} ≥ 14 V; I_{GATE} ≤ 5 µA
Gate Pull-Dn (On) Current	I_{GATEDN}	20	25	30	µA	V_{GATE} = Vcc V
Gate Pull-Up (Off) Current	I_{GATEUP}					
Regulation	I_{GATEUP_REG}	−45	−60	−75	µA	ΔV_{GATE} ≥ 2 V; (SENSE+) – (SENSE−) = 70 mV
Fault	I_{GATEUP_FLT}	−7	−13	−20	mA	ΔV_{GATE} = 2 V
CURRENT SENSE VOLTAGE						
Sense Voltage Current Limit (SENSE+ – SENSE−)	$V_{SENSECL}$	46	50	54	mV	V_{ISET} > 2.65 V; V_{FLB} > 1.1 V; ΔV_{GATE} = 3 V; I_{GATE} = 0 µA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Foldback Inactive						$\Delta V_{GATE} = 3$ V; $I_{GATE} = 0$ µA
			62.5		mV	$V_{ISET} = 2.5$ V; $V_{FLB} > 1.35$ V
			50		mV	$V_{ISET} = 2$ V; $V_{FLB} > 1.1$ V
			25		mV	$V_{ISET} = 1$ V; $V_{FLB} > 0.57$ V
		8.5	12.5	16.5	mV	$V_{ISET} = 0.5$ V; $V_{FLB} > 0.3$ V
Foldback Active		6.0	10.0	14	mV	$V_{FLB} = 0$ V; $\Delta V_{GATE} = 3$ V; $I_{GATE} = 0$ µA
		21.0	25.0	29.0	mV	$V_{ISET} > 2$ V; $V_{FLB} = 0.5$ V; $\Delta V_{GATE} = 3$ V; $I_{GATE} = 0$ µA
Circuit Breaker Offset	V_{CBOS}	0.5	1	1.5	mV	Circuit breaker trip voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
SEVERE OVERCURRENT						
Voltage Threshold	$V_{SENSEOC}$	90	100	110	mV	$V_{ISET} > 2.65$ V
		20	25	30	mV	$V_{ISET} = 0.5$ V
Glitch Filter Duration		0.5		1.5	µs	
Response Time			2.0	3.5	µs	
TIMER PIN						
Timer Pull-Up Current	$I_{TIMERUP}$	−18	−20	−22	µA	Overcurrent fault; $0.2\text{ V} \leq V_{TIMER} \leq 2\text{ V}$
Timer High Threshold	V_{TIMERH}	1.96	2.0	2.04	V	
Timer Low Threshold	V_{TIMERL}	0.18	0.2	0.22	V	
TIMER_OFF PIN						
POR Pull-Up Current	I_{POR}	−18	−20	−22	µA	Initial Power-On Reset; $V_{TIMER\_OFF} = 1$ V
Retry Pull-Up Current	I_{TMROFF}	−0.8	−1	−1.2	µA	After fault when GATE is off; $V_{TIMER\_OFF} = 1$ V
Timer_off High Threshold	$V_{TMROFFH}$	1.96	2.0	2.04	V	
FOLDBACK (FLB PIN)						
Input Current	I_{FLB}			100	nA	$V_{FLB} \leq 5.5$ V; $T_A = -40$°C to +85°C
Input Current	I_{FLB}			1	µA	$V_{FLB} \leq 5.5$ V; $T_A = -40$°C to +125°C
FEEDBK_PG (FB_PG PIN)						
PWRGD Rising Threshold	V_{PGTH}	0.99	1.0	1.01	V	FB_PG rising
PWRGD Threshold Hysteresis	PG_{HYST}	20	30	40	mV	
Input Current	I_{FBPG}			100	nA	$V_{FB\_PG} \leq 5.5$ V; $T_A = -40$°C to +85°C
Input Current	I_{FBPG}			1	µA	$V_{FB\_PG} \leq 5.5$ V; $T_A = -40$°C to +125°C
Power-Good Glitch Filter	PG_{GF}	0.5		1.5	µs	50 mV overdrive
$\overline{\text{FAULT}}$ PIN						
Output Low Voltage	V_{OL_FAULT}			0.1	V	$I_{FAULT} = 100$ µA
				0.5	V	$I_{FAULT} = 1$ mA
Leakage Current	I_{FAULT}			1	µA	$V_{FAULT} = 5.5$ V; $\overline{\text{FAULT}}$ output high-Z
ENABLE PIN						
Input High Voltage	V_{IH}	1.2			V	
Input Low Voltage	V_{IL}			0.4	V	
Leakage Current	I_{EN}			1	µA	$V_{EN} = 5.5$ V
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.1	V	$I_{PWRGD} = = 100$ µA
				0.5	V	$I_{PWRGD} = 1$ mA
VCC For Valid PWRGD		1.7			V	$I_{SINK} = 100$ µA; $V_{OL\_PWRGD} = 0.4$ V
Leakage Current	I_{PWRGD}			1	µA	$V_{PWRGD} = 60$ V; PWRGD output high-Z

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC/SENSE+	−0.3 V to +66 V
VCAP	−0.3 V to +6 V
UV	−0.3 V to +6 V
OV	−0.3 V to +6 V
ISET	−0.3 V to VCAP + 0.3V
FLB	−0.3 V to +6 V
FB_PG	−0.3 V to +6 V
TIMER_OFF	−0.3 V to VCAP + 0.3V
TIMER	−0.3 V to VCAP + 0.3V
$\overline{\text{FAULT}}$	−0.3 V to +6 V
ENABLE	−0.3 V to +6 V
PWRGD	−0.3 V to +66 V
GATE	−0.3 V to V_{CC} + 0.3V
SENSE−	−0.3 V to V_{CC} + 0.3V
RPFG	−0.3 V to V_{CC} + 0.3V
V_{SENSE} (V_{SENSE+} – $V_{SENSE−}$)	±0.3 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16 Lead 3x3 LFCSP	TBD	°C/W
16 Lead QSOP	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

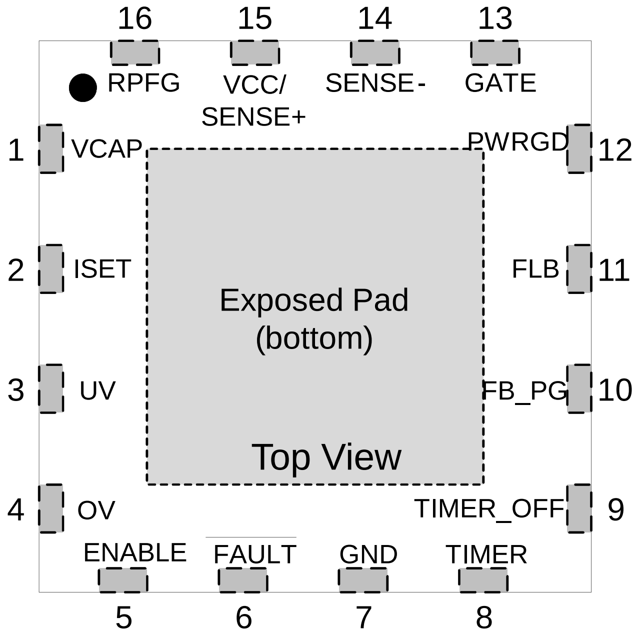


Figure 2. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
2	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
3	UV	Undervoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
4	OV	Overvoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
5	ENABLE	Enable Pin. This pin is a digital logic input. This input must be high to allow the ADM1270 controller to begin a power-up sequence. If this pin is held low, the ADM1270 is prevented from powering up. There is no internal pull-up on this pin.
6	$\overline{\text{FAULT}}$	Fault Output. This pin indicates that the device has shut down due to an Over Current fault condition. The device can be configured for automatic retry after shut down by connecting this pin directly to the ENABLE pin.
7	GND	Ground Pin.
8	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an SOA Over Current fault delay. The GATE pin is pulled off when the voltage on the TIMER pin exceeds the upper threshold.
9	TIMER_OFF	Timer Off Pin. An external capacitor, C_{TIMER_OFF}, sets an initial timing cycle delay and the SOA off-time delay. After an SOA Over Current fault has occurred, the GATE pin is pulled off until the voltage on the TIMER_OFF pin exceeds the threshold.
10	FB_PG	PWRGD Feedback Input Pin. An external resistor divider is connected from the Output Voltage to this pin to allow an internal comparator to detect when the Output Voltage is above the PWRGD threshold.
11	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback is used to reduce the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.
12	PWRGD	Power-Good Signal. Used to indicate that the supply is within tolerance. This signal is based on the voltage present on the FB_PG pin.
13	GATE	Gate Output Pin. This pin is the gate drive of an external P-channel FET. This pin is driven by the FET drive controller, which provides a pull-down current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held off when the supply is below UVLO.
14	SENSE–	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog

Pin No.	Mnemonic	Description
		current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
15	VCC/SENSE+	Positive Supply Input Pin. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held off when the supply is below UVLO. No sequencing is required. Positive Current Sense Input Pin. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$).
16	RPFG	Reverse Protection FET Gate driver output. Connect to the gate of the external Reverse Protection P-channel FET for low voltage drop operation.
EP	EP	Exposed Pad. The exposed pad is located on the underside of the LFCSP package. Solder the exposed pad to the printed circuit board (PCB) to improve thermal dissipation. The exposed pad can be connected to ground.

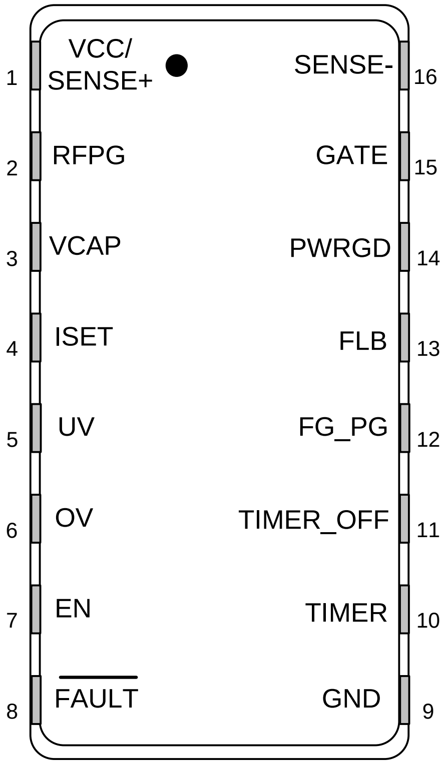


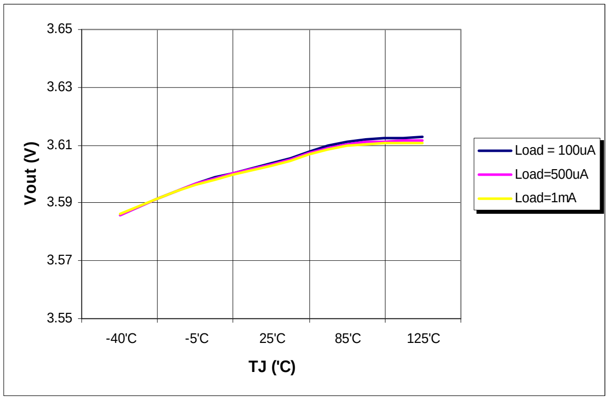
Figure 3. QSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC/SENSE+	Positive Supply Input Pin. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held off when the supply is below UVLO. No sequencing is required. Positive Current Sense Input Pin. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$).
2	RPFG	Reverse Protection FET Gate driver output. Connect to the gate of the external Reverse Protection P-channel FET for low voltage drop operation.
3	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
4	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
5	UV	Undervoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
6	OV	Overvoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
7	ENABLE	Enable Pin. This pin is a digital logic input. This input must be high to allow the ADM1270 controller to begin a

Pin No.	Mnemonic	Description
		power-up sequence. If this pin is held low, the ADM1270 is prevented from powering up. There is no internal pull-up on this pin.
8	$\overline{\text{FAULT}}$	Fault Output. This pin indicates that the device has shut down due to an Over Current fault condition. The device can be configured for automatic retry after shut down by connecting this pin directly to the ENABLE pin.
9	GND	Ground Pin.
10	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an SOA Over Current fault delay. The GATE pin is pulled off when the voltage on the TIMER pin exceeds the upper threshold.
11	TIMER_OFF	Timer Off Pin. An external capacitor, C_{TIMER_OFF}, sets an initial timing cycle delay and the SOA off-time delay. After an SOA Over Current fault has occurred, the GATE pin is pulled off until the voltage on the TIMER_OFF pin exceeds the threshold.
12	FB_PG	PWRGD Feedback Input Pin. An external resistor divider is connected from the Output Voltage to this pin to allow an internal comparator to detect when the Output Voltage is above the PWRGD threshold.
13	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback is used to reduce the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.
14	PWRGD	Power-Good Signal. Used to indicate that the supply is within tolerance. This signal is based on the voltage present on the FB_PG pin.
15	GATE	Gate Output Pin. This pin is the gate drive of an external P-channel FET. This pin is driven by the FET drive controller, which provides a pull-down current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held off when the supply is below UVLO.
16	SENSE−	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.

TYPICAL PERFORMANCE CHARACTERISTICS



Fig

Figure 4. V_{CAP} vs. Temperature, Different Loads

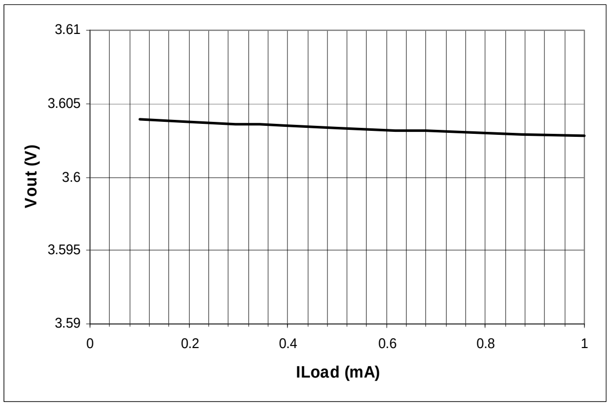


Figure 5. V_{CAP} vs Load Current

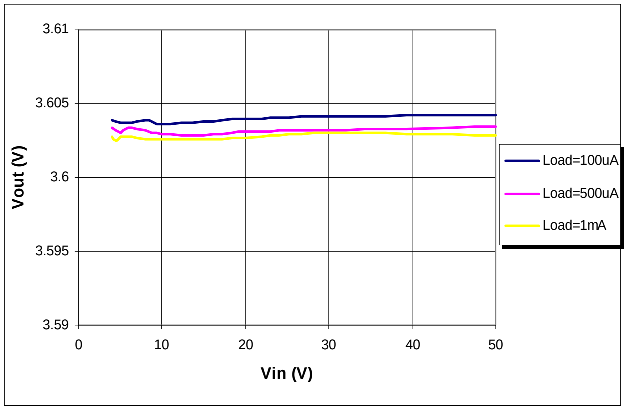


Figure 6. V_{CAP} vs Input Voltage, Different Loads

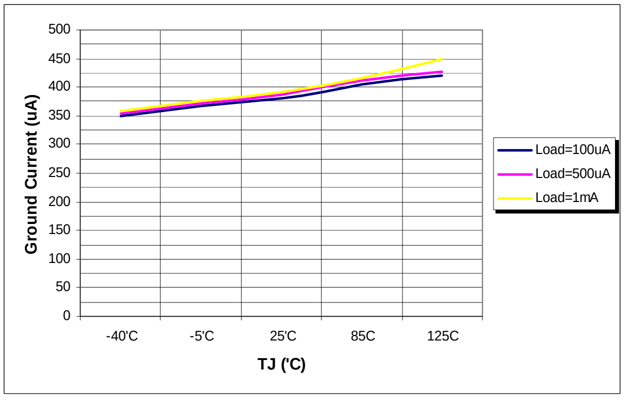


Figure 7. Supply Current (I_{CC}) vs. Temperature, Different Loads

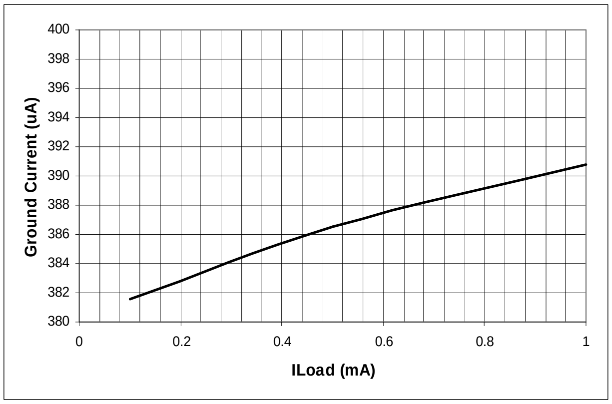


Figure 8. Supply Current (I_{CC}) vs. Load Current

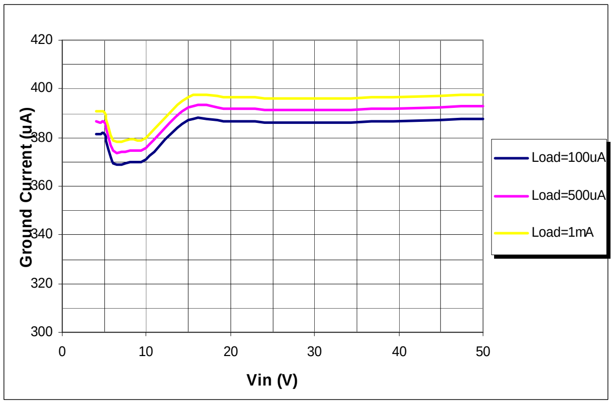


Figure 9. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC}), Different Loads

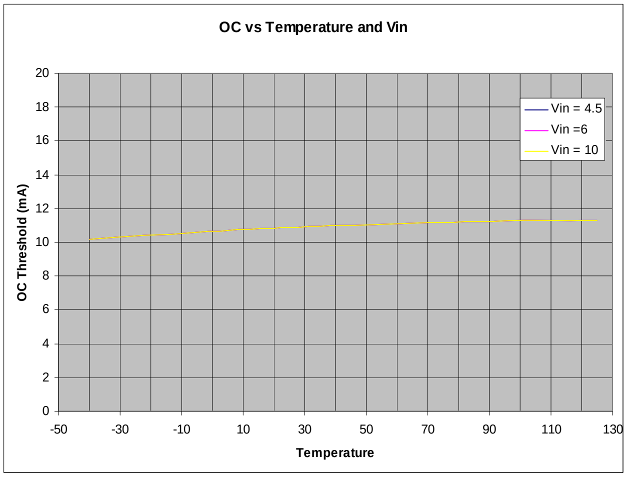


Figure 10. V_{CAP} Over Current Limit vs Temperature, Different Input Voltage

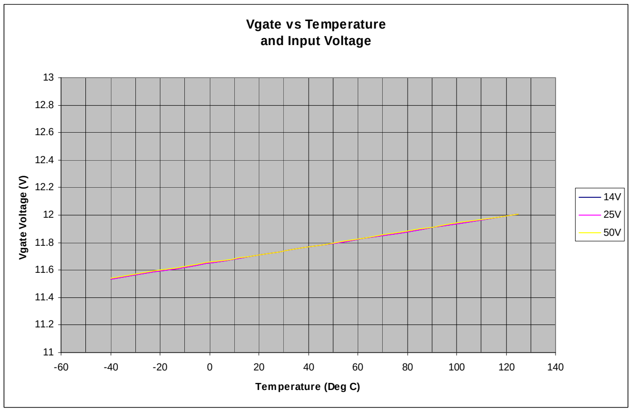


Figure 11. Gate Voltage vs. Temperature, Different Input Voltage

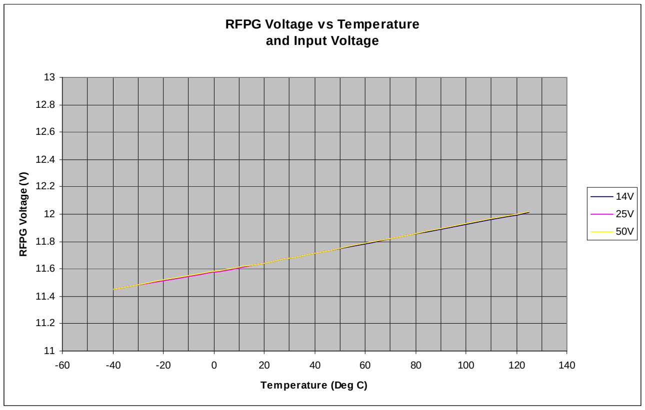


Figure 12. RFPG Voltage vs. Temperature, Different Input Voltage

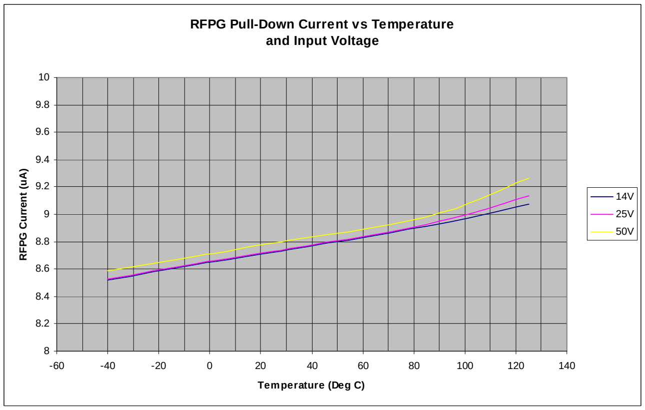


Figure 13. RFPG Pull-Down Current vs. Temperature, Different Input Voltage

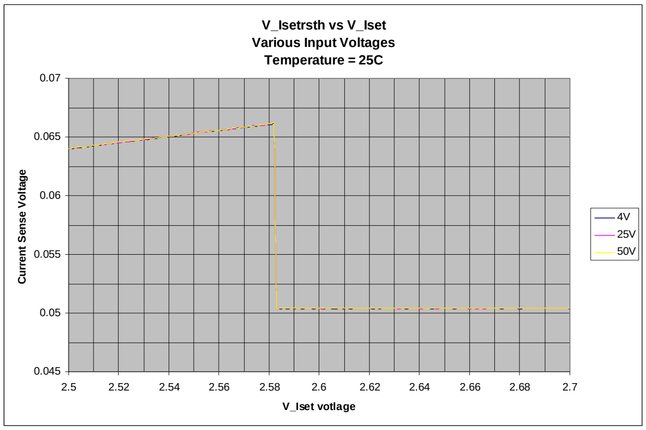


Figure 14. $V_{Isetrsth}$ vs V_{Iset}, Different Input Voltage

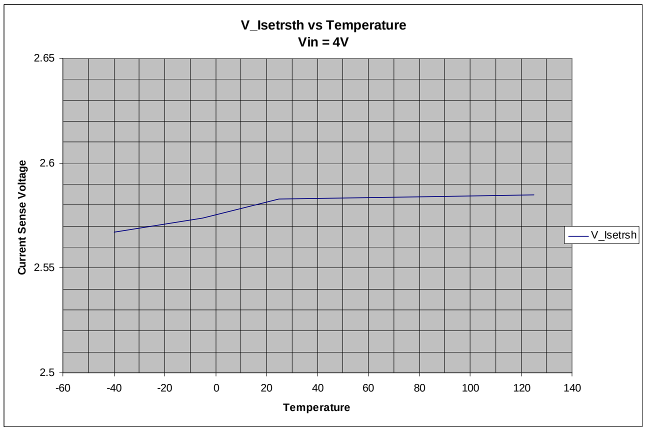


Figure 15. $V_{Isetrsth}$ vs Temperature, V_{IN} = 4V

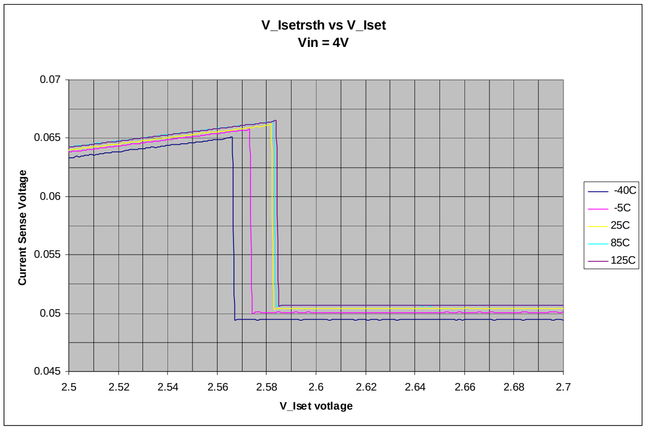


Figure 16. $V_{Isetrsth}$ vs V_{Iset}, Different Temperature

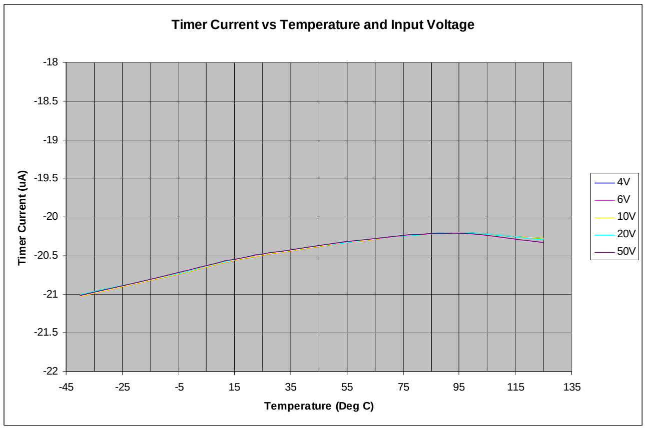


Figure 17. Timer Current vs Temperature, Different V_{IN}

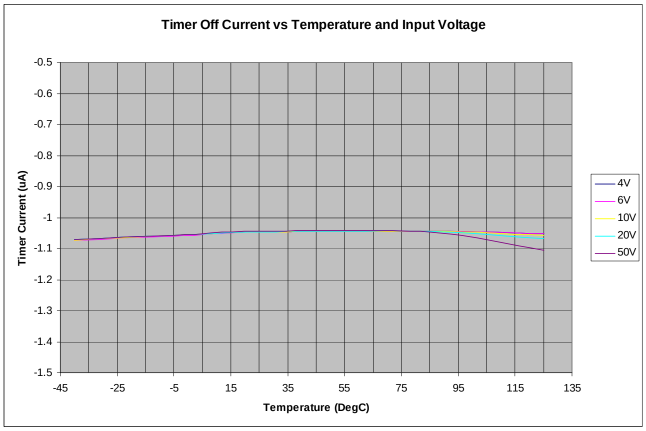


Figure 18. TimerOff Current vs Temperature, Different V_{IN}

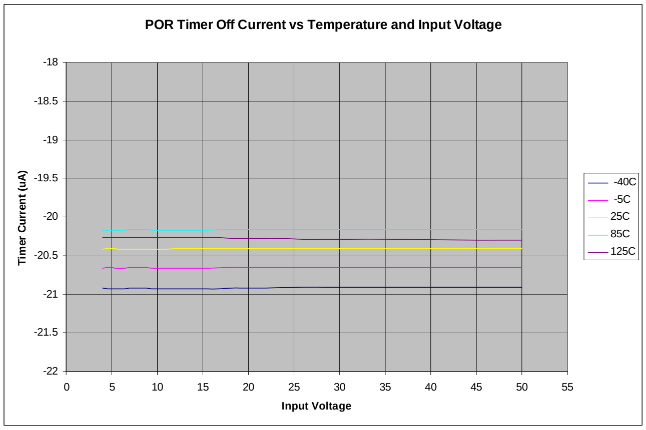


Figure 19. POR TimerOff Current vs V_{IN}, Different Temperature

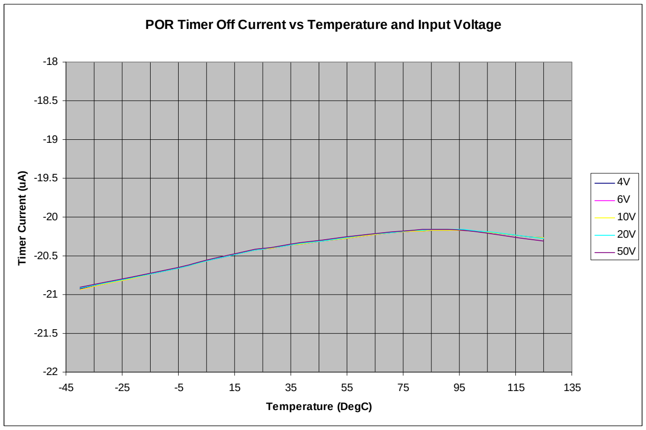


Figure 20. . POR TimerOff Current vs Temperature, Different V_{IN}

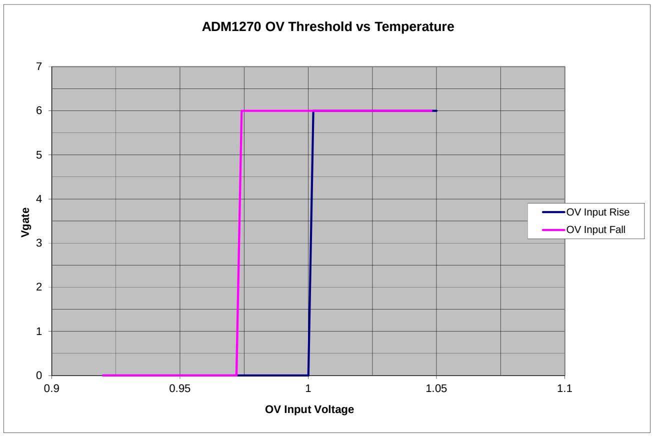


Figure 21. OV Threshold vs OV Input Voltage

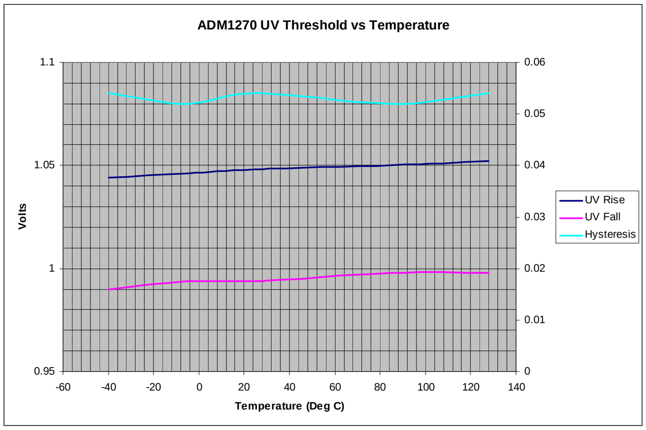


Figure 22. UV Threshold vs Temperature

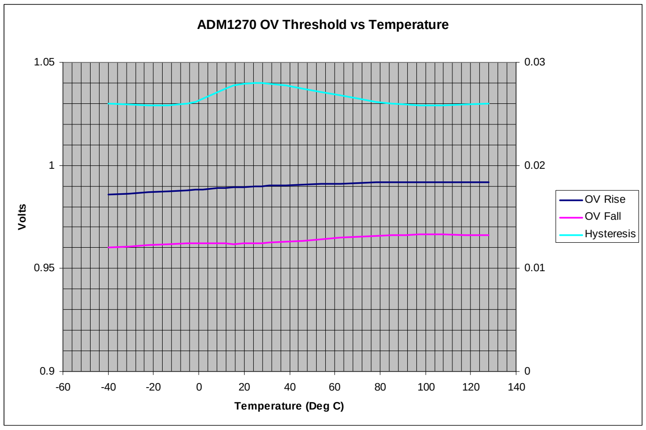


Figure 23. OV Threshold vs Temperature

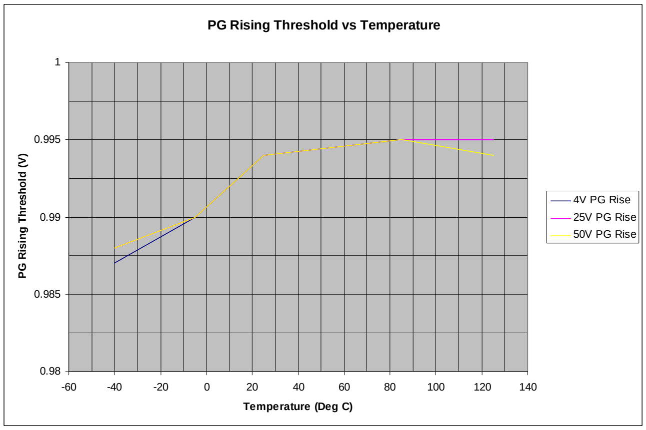


Figure 24. PG Rising Threshold vs Temperature, Different V_{IN}

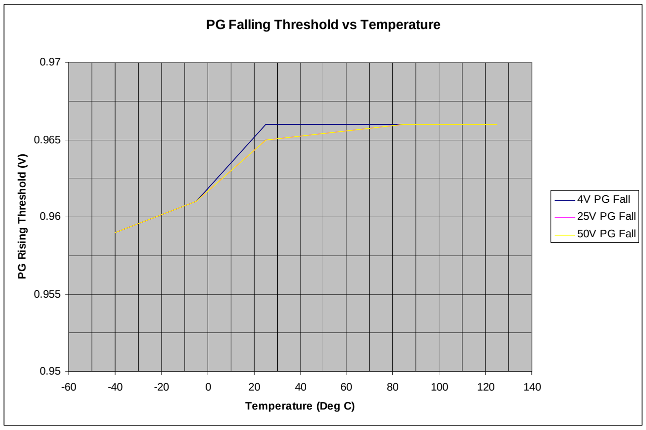


Figure 25. PG Falling Threshold vs Temperature, Different V_{IN}

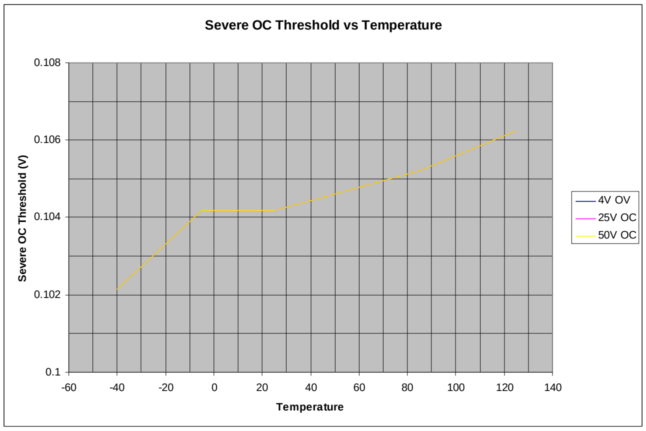


Figure 26. Severe OC Threshold vs Temperature, Different V_{IN}

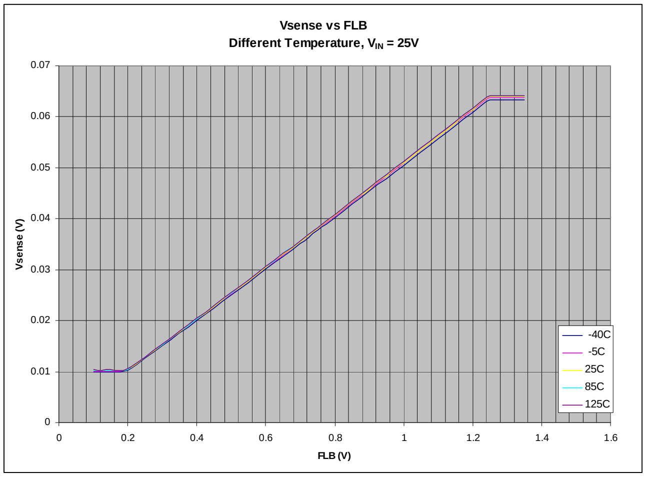


Figure 27. V_{SENSE} vs FLB, Different Temperatures

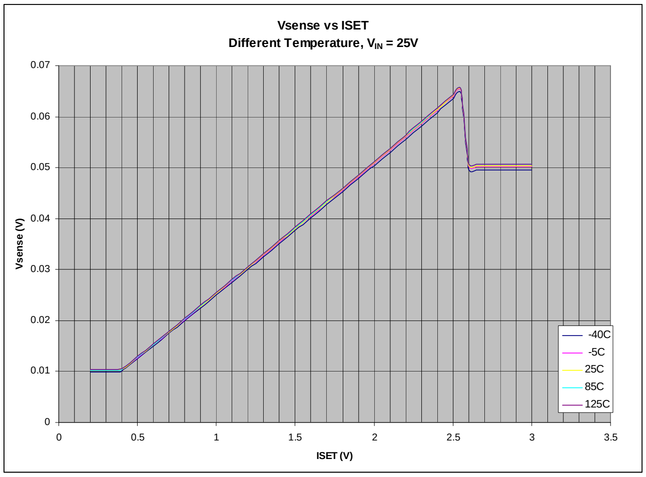


Figure 28. V_{SENSE} vs ISET, Different Temperatures

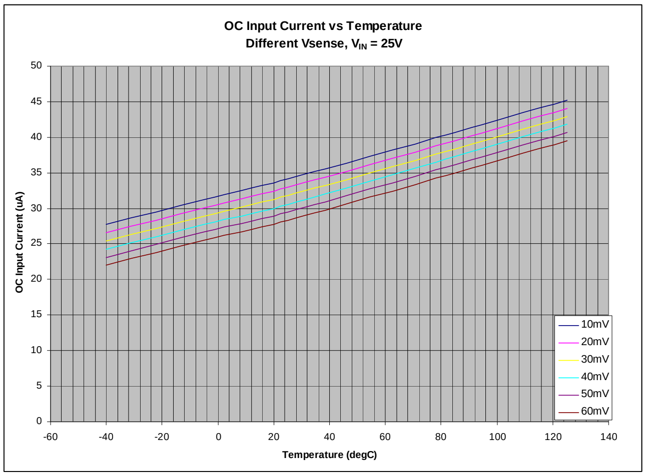


Figure 29. OC Input Current vs Temperature, Different V_{SENSE}

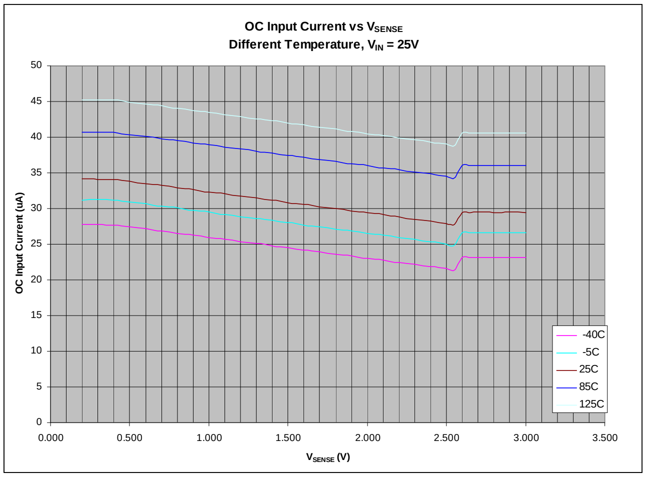


Figure 30. OC Input Current vs V_{SENSE}, Different Temperature

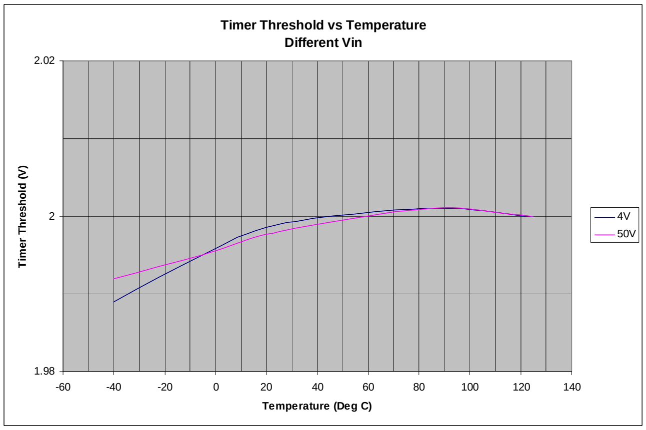


Figure 31. OC Timer Threshold vs Temperature, Different V_{IN}

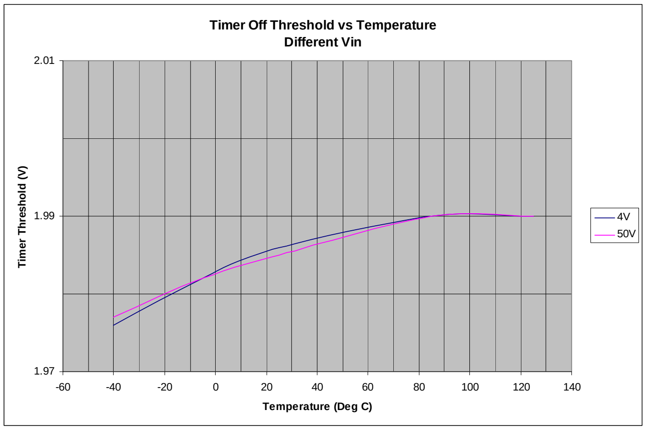


Figure 32. OC Timer Off Threshold vs Temperature, Different V_{IN}

TYPICAL APPLICATION CIRCUIT

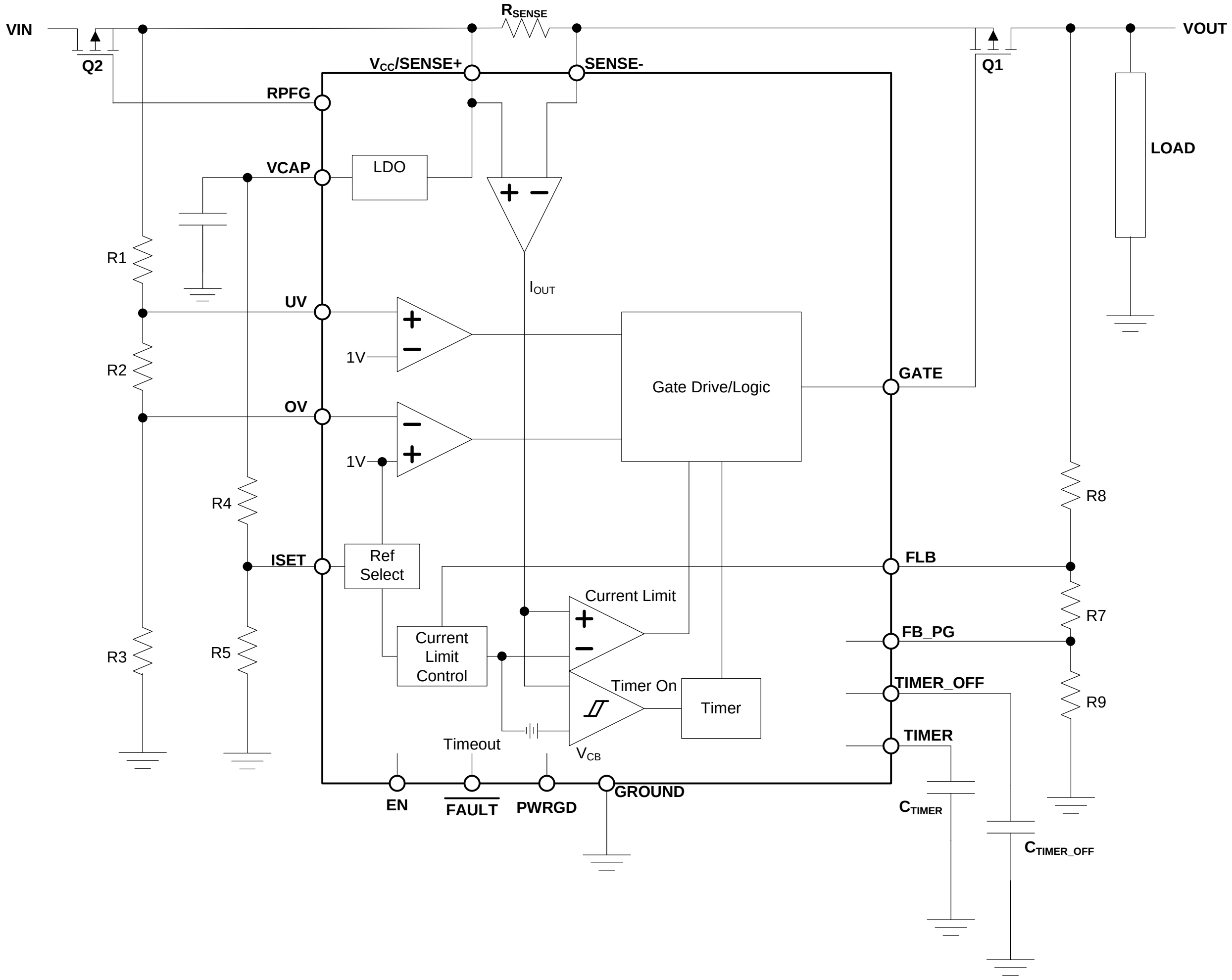


Figure 33. Typical Application Circuit

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as voltage dips on the backplane supply that can reset other boards in the system.

The ADM1270 is designed to control the in-rush current during the powering on of a system, allowing a board to be inserted into a live backplane by protecting it from excess currents.

The ADM1270 is a current limiting controller that is intended to provide inrush current limiting and overcurrent protection for modular or battery powered systems. The voltage developed across a sense resistor in the power path is measured with a current sense amplifier via the VCC/SENSE+ and SENSE− pins. A default limit of 50 mV is set, but this limit can be adjusted, if required, using a resistor divider network from the VCAP pin to the ISET pin.

The ADM1270 limits the current through the sense resistor by controlling the gate voltage of an external P-channel FET in the power path, via the GATE pin. The sense voltage and, therefore, the load current is maintained below the preset maximum. The ADM1270 protects the external FET by limiting the time that the FET remains on while the current is at its maximum value. This current-limit time is set by the choice of capacitors connected to the TIMER pin and the TIMER_OFF pin. This helps to maintain the FET in its safe operating area (SOA).

In addition to the timer, there is a foldback pin that is used to provide additional FET protection. The current limit is linearly reduced by the voltage on the FLB pin, so that for large Vds voltage drops, the actual current limit used by the part is lower, again helping to ensure the FET is kept within its SOA.

A minimum voltage clamp is used to ensure that even if the FLB voltage is 0 V, the current is never reduced to zero, which would otherwise prevent the device from powering up.

The ADM1270 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UV and OV pins.

A PWRGD signal can be used to detect when the output supply is greater than a voltage programmed using an external resistor divider on the FB_PG pin.

To protect the system from a reverse polarity input supply, there is a provision made to control an additional external P-channel FET with the RPFG pin. This feature allows for a low on-resistance, low voltage drop FET to be used in place of a diode to perform the same function, thus saving power losses and improving overall efficiency. The reverse voltage protection FET is intended to prevent negative input voltages that could damage the load or the ADM1270.

FUNCTIONAL BLOCK DIAGRAM

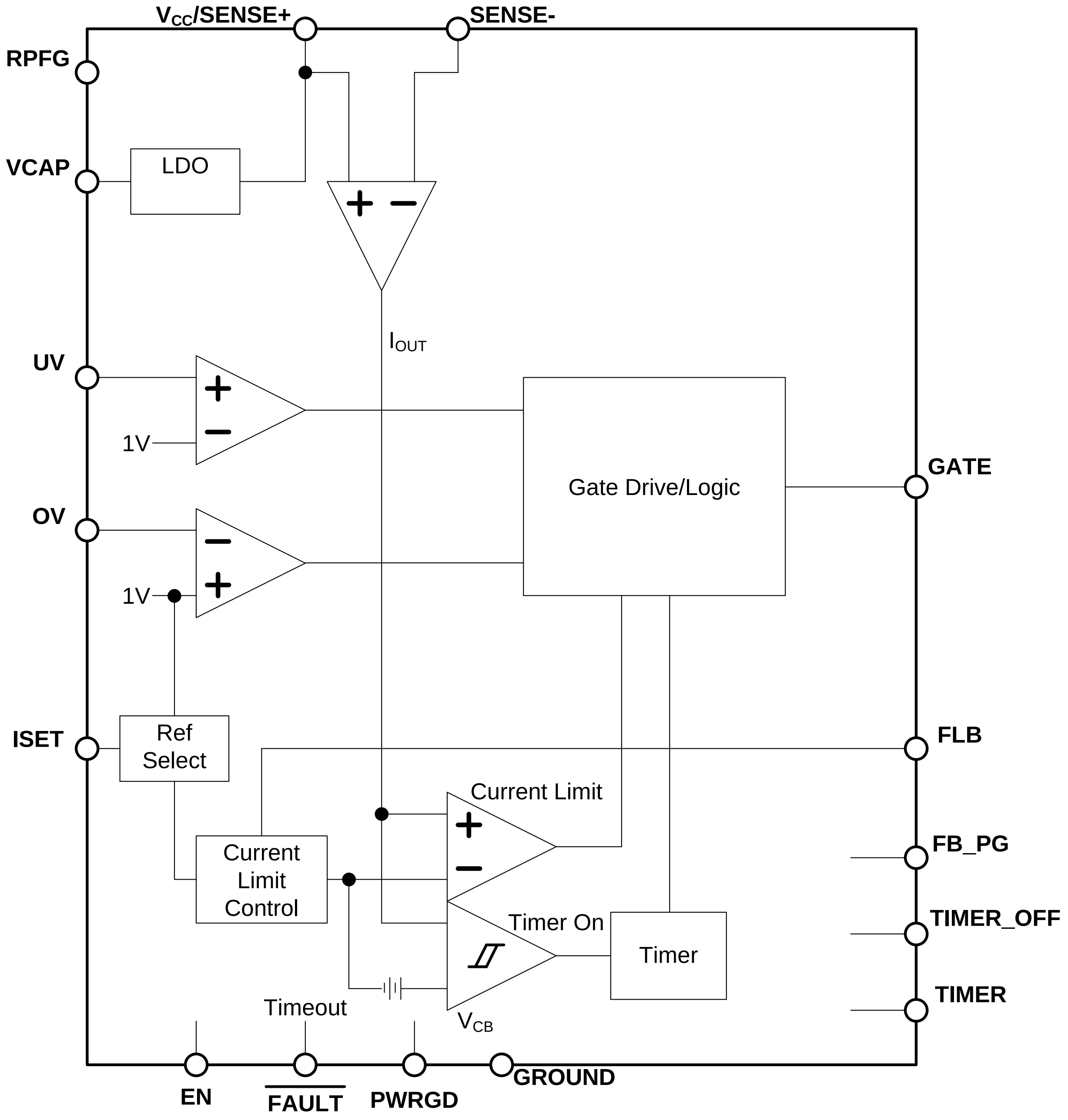


Figure 34. Functional Block Diagram

POWERING THE ADM1270

A supply voltage from 4 V to 60 V is required to power the ADM1270 via the VCC/SENSE+ pin. The VCC/SENSE+ pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and best regulate the V_{GS} voltage is supplied by the SENSE- pin.

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external current sense resistor, R_{SENSE} (see Figure 35). An internal current sense amplifier provides a gain of 40 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and is used by the hot swap control logic to detect an overcurrent condition.

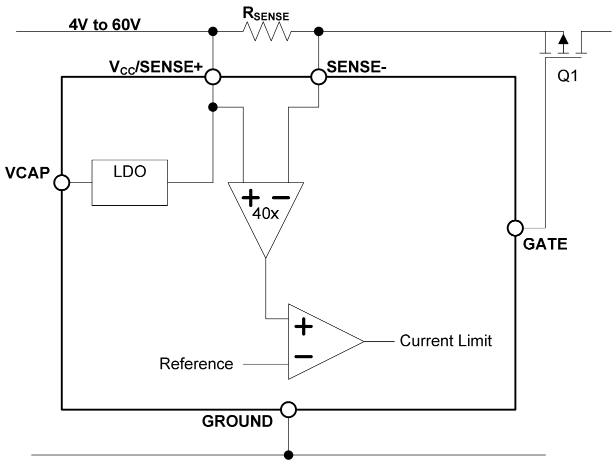


Figure 35. Hot Swap Current Sense Amplifier

CURRENT-LIMIT REFERENCE

The current-limit reference voltage determines the load current at which the ADM1270 limits the current during an over-current event. This reference voltage is compared to the amplified current sense voltage to determine when the current limit threshold is reached.

An internal current-limit reference selector block continuously compares the ISET and FLB (foldback) voltages to determine which voltage is the lowest at any given time; the lowest voltage is used as the current-limit reference. This ensures that the programmed current limit, ISET, is used in normal operation, and that the foldback feature reduces the current limit when required during startup and/or fault conditions.

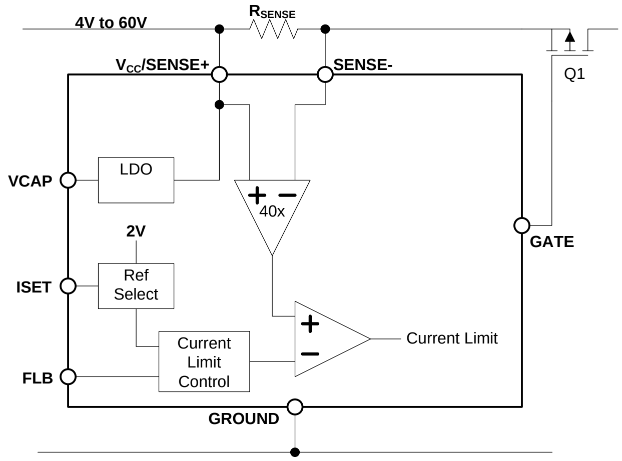


Figure 36. *Current-Limit Reference Selection*

The foldback voltage varies during different modes of operation and, therefore, is clamped to a minimum level of 200 mV. This is to prevent zero current flow due to the current limit being set too low. Figure 37 provides an example of how the FLB (foldback) and ISET voltages interact during startup as the ADM1270 is turning on the FET and charging the load capacitance. Depending on how the foldback feature is configured, the transition point can vary to ensure that the FET is being operated within the correct limits.

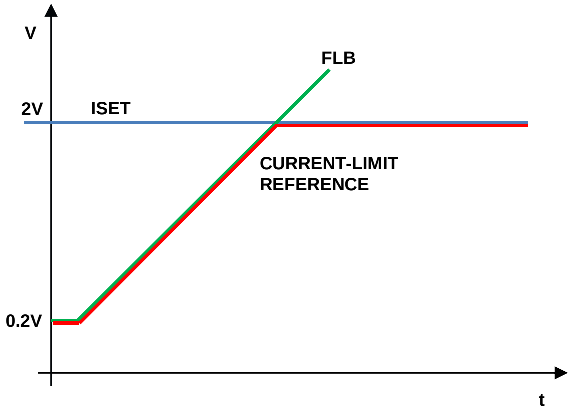


Figure 37. Interaction of Foldback and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor value decreases for a given current sense voltage. Choosing an appropriate current sense resistor can be difficult due to the limited selection of low value resistors. The ADM1270 provides an adjustable current sense voltage limit to handle this issue. The device allows the user to program the required current sense voltage limit from 12.5 mV to 62.5 mV.

The default value is 50 mV and is achieved by connecting the ISET pin directly to the VCAP pin. This configures the device to use an internal 2 V reference, which results in 50 mV at the sense inputs (see Figure 38).

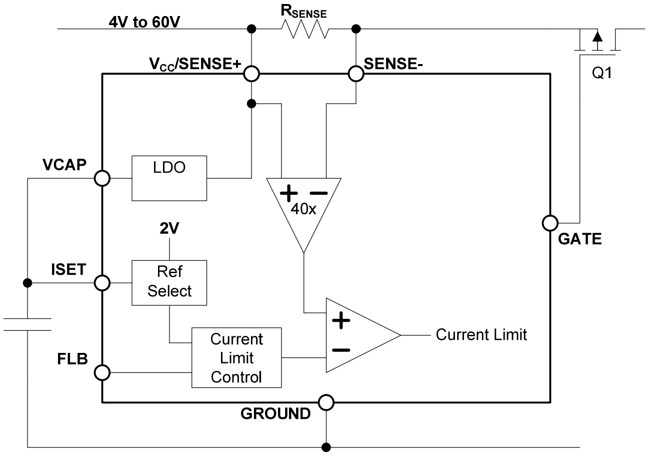


Figure 38. Fixed 50 mV Current Sense Limit

To program the sense voltage from 12.5 mV to 62.5 mV, an external resistor divider sets the reference voltage on the ISET pin (see Figure 39).

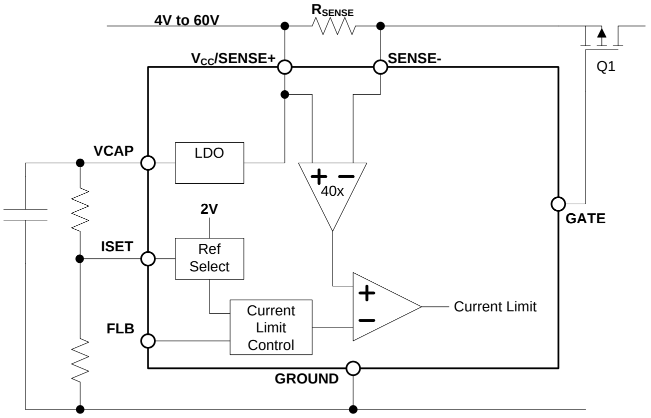


Figure 39. Adjustable 12.5 mV to 62.5 mV Current Sense Limit

The VCAP pin has a 3.6 V internally generated voltage that can be used to set a voltage at the ISET pin. Assuming that V_{ISET} equals the voltage on the ISET pin, select the resistor divider values to set the ISET voltage as follows:

$V_{ISET} = V_{SENSE} \times 50$

where V_{SENSE} is the current sense voltage limit.

The VCAP rail also can be used as the pull-up supply for setting other pins. In order to guarantee accuracy specifications, do not apply a load to the VCAP pin greater than 100 µA.

FOLDBACK

Foldback is a method to actively reduce the current limit as the voltage drop across the FET increases. This keeps the power dissipation in the FET at a minimum during power-up, overcurrent, or short-circuit events. It also reduces the need to oversize the FET to accommodate worst-case conditions, resulting in board size and cost savings.

The ADM1270 detects the voltage drop across the FET by sensing output voltage through a resistor divider. This assumes that the supply voltage remains constant and within tolerance. The device, therefore, relies on the principle that the drain of the FET is at the maximum expected supply voltage, and that the magnitude of the output voltage is relative to that of the V_{DS} of the FET. Using a resistor divider from the output voltage to the FLB pin, the relationship from V_{OUT}, and thus V_{DS}, to V_{FLB} can be derived.

Design the resistor divider to result in a voltage equal to $V_{ISET}/2$ when V_{OUT} falls below the desired level. This should be well below the working tolerance of the supply rail. As V_{OUT} continues to drop, the current-limit reference follows V_{FLB} because it is now the lowest voltage input to the current-limit reference selector block. This results in a reduction of the current limit and, therefore, the regulated load current. To prevent the current from decreasing to zero, a clamp activates when V_{FLB} reaches 200 mV. The current limit cannot drop below this level.

To ensure that the SOA characteristics of a particular FET are not violated, the minimum current for this clamp varies from design to design. However, the current-limit reference fixes this clamp at 200 mV, which equals 10 mV across the sense resistor. Therefore, the main ISET voltage can be adjusted to adjust the clamp to the required percentage current reduction. For example, if V_{ISET} equals 1.6 V, the clamp can be set at 25% of the maximum current.

TIMER

The TIMER pin handles the timing function with an external capacitor, C_{TIMER}. The TIMER pin comparator threshold is V_{TIMERH} (2.0 V) and the timing current source is a 20 µA pull-up.

These current and voltage levels, in combination with the user chosen value of C_{TIMER}, determine the fault current-limit time and the on-time of the hot swap retry duty cycle. The TIMER pin capacitor value is determined using the following equation:

$C_{TIMER} = (t_{ON} \times 20\ \mu A)/V_{TIMERH}$

where t_{ON} is the time that the FET is allowed to spend in regulation at the current limit.

The choice of FET is based on matching this time with the SOA characteristics of the FET. Foldback can also be used to simplify the selection.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 20 µA timer pull-up current is activated, and the ADM1270 begins to regulate the load current at the current limit. This initiates a rising voltage ramp on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH}, the 20 µA pull-up is disabled and the TIMER pin is discharged to GND.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which causes the timer to start a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 20 µA pull-up remains active and the FET remains in regulation.

This allows the TIMER pin to reach V_{TIMERH} and initiate the GATE shutdown and the $\overline{\text{FAULT}}$ pin is pulled low immediately.

In latch-off mode, the TIMER pin is discharged to GND when it reaches the V_{TIMERH} threshold. The TIMER_OFF pin begins to charge up. While the TIMER_OFF pin is being pulled up, the hot swap controller remains off and cannot be turned back on and the $\overline{\text{FAULT}}$ pin remains low. When the voltage on the TIMER_OFF pin goes above the $V_{TMROFFH}$ threshold, the hot swap controller can be re-enabled by toggling the ENABLE pin from high to low and then high again.

TIMER_OFF

The TIMER_OFF pin handles two timing functions with an external capacitor, C_{TIMER_OFF}. There is one TIMER_OFF pin comparator threshold at $V_{TMROFFH}$ (2.0 V). There are two timing current sourcesl, a 20 µA pull-up and a 1 µA pull-up.

These current and voltage levels, in combination with the user chosen value of C_{TIMER_OFF} , determine the initial power-on reset time and also set the fault current-limit off time.

When VCC is connected to the input supply, the internal supply (VCAP) of the ADM1270 must charge up. VCAP starts up and settles in a very short time, when the under-voltage lockout (UVLO) voltage is exceeded at VCAP, the device emerges from reset. During this first short reset period, the GATE and TIMER pins are both held low.

The ADM1270 then goes through an initial timing cycle. The TIMER_OFF pin is pulled high with 20 µA. When the TIMER_OFF pin reaches the $V_{TMROFFH}$ threshold (2.0 V), the initial timing cycle is complete. This initial power-on reset duration is determined by the following equation:

$$t_{INITIAL} = V_{TMROFFH} \times (C_{TIMER\_OFF}/20\ \mu A)$$

For example, a 100 nF capacitor results in a delay of approximately 10 ms. If the UV and OV inputs indicate that VCC is within the defined window of operation when the initial timing cycle terminates, the device is ready to start a hot swap operation.

At the completion of this initial power-on reset cycle, the TIMER_OFF pin is ready to perform a second function. When the voltage at the TIMER pin exceeds the fault current-limit time threshold voltage of V_{TIMERH} (2.0 V), the 1 µA pull-up current is activated on TIMER_OFF and C_{TIMER_OFF} begins to charge. This initiates a voltage ramp on the TIMER_OFF pin. When the TIMER_OFF pin reaches $V_{TMROFFH}$, the TIMER_OFF fault current-limit off time is complete.

This fault current-limit off time is determined by the following equation:

$$t_{TIMER\_OFF} = V_{TMROFFH} \times (C_{TIMER\_OFF}/1\ \mu A)$$

For example, a 100 nF capacitor results in an off time of approximately 200 ms from the time TIMER exceeds V_{TIMERH} to the time TIMER_OFF reaches $V_{TMROFFH}$.

HOT SWAP RETRY DUTY CYCLE

The ADM1270 turns off the FET after an overcurrent fault and then uses the capacitor on the TIMER_OFF pin to generate a delay before automatically retrying the hot swap operation. To configure the ADM1270 for auto-retry mode, tie the $\overline{\text{FAULT}}$ pin to the ENABLE pin. Note that a pull-up resistor to VCAP is required on the $\overline{\text{FAULT}}$ pin.

When an overcurrent fault occurs, the capacitor on the TIMER pin charges with a 20 µA pull-up current. When the TIMER pin reaches V_{TIMERH} (2.0 V), the GATE pin is pulled high turning off the FET. When the $\overline{\text{FAULT}}$ pin is tied to the ENABLE pin for auto-retry mode, the TIMER_OFF pin begins to charge with a 1 µA current source. When the the TIMER_OFF pin reaches $V_{TMROFFH}$ (2.0 V), it automatically restarts the hot swap operation.

The automatic retry duty cycle is set by the ratio of 1µA/20µA and the ratio of C_{TIMER}/C_{TIMER_OFF}. The retry duty cycle is set by the following equation:

$$\text{Duty\_cycle} = (C_{TIMER} \times 1\ \mu A)/(\ C_{TIMER\_OFF} \times 20\ \mu A)$$

The value of the C_{TIMER} and C_{TIMER_OFF} capacitors determine the on and off time of this cycle, which are calculated as follows:

$$t_{ON} = V_{TIMERH} \times (C_{TIMER}/20\ \mu A)$$

$$t_{OFF} = V_{TMROFFH}\ \times (C_{TIMER\_OFF}/1\ \mu A)$$

A 100 nF capacitor on the TIMER pin gives an on time of 10 ms. A 100nF capacitor on the TIMER_OFF pin gives an off time of 200 ms. The device retries continuously in this manner and can be disabled manually by holding the ENABLE pin low, or by disconnecting the $\overline{\text{FAULT}}$ pin. To prevent thermal stress in the FET, a capacitor on the TIMER_OFF pin can be used to extend the retry time to any desired level.

GATE AND RPFG CLAMPS

The circuits driving the GATE and RPFG pins are clamped to less than 14 V below the VCC/SENSE+ pin. These clamps ensure that the maximum V_{GS} rating of the external FETs is not exceeded.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1270 includes a separate, high bandwidth, current sense amplifier that is used to detect a severe overcurrent that is indicative of a short-circuit. The fast response time allows the ADM1270 to handle events of this type that could otherwise cause catastrophic damage if not detected, and dealt with very quickly. The fast response circuit ensures that the ADM1270 can detect an overcurrent event of approximately 200% of the normal current limit (ISET) and control the current within about 2 µs.

UNDERVOLTAGE AND OVERVOLTAGE

The ADM1270 monitors the supply voltage for undervoltage (UV) and overvoltage (OV) conditions. The UV and OV pins are connected to the inputs of voltage comparators and compared to an internal 1 V voltage reference.

Figure 40 illustrates the voltage monitoring input connections. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UV pin falls below 1 V, and the FET is turned off with the 10 mA pull-up device. Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the FET is turned off using the 10 mA pull-up device.

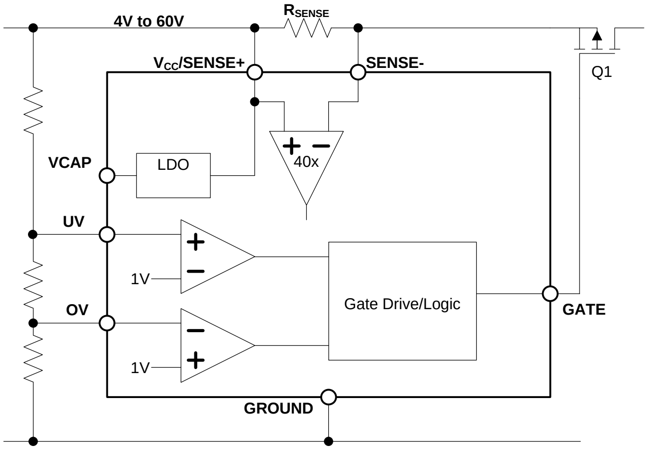


Figure 40. Undervoltage and Overvoltage Supply Monitoring

ENABLE INPUT

The ADM1270 provides a dedicated ENABLE digital input pin. The ENABLE pin allows the ADM1270 to remain off by using a hardware signal, even when the voltage on the UV pin is above 1.0 V and the voltage on the OV pin is less than 1.0 V.

Although the UV pin can be used to provide a digital enable signal, using the ENABLE pin for this purpose keeps the ability to monitor undervoltage conditions.

In addition to the conditions for the UV and OV pins, the ADM1270 ENABLE input pin must be high for the device to begin a power-up sequence.

A similar function can be achieved using the UV pin directly. Alternatively, if the UV divider function is still required, the configuration shown in Figure 41 can be used.

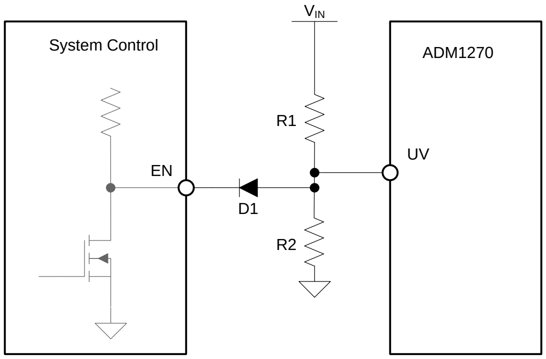


Figure 41. *Using the UV Pin as an Enable*

Diode D1 prevents the external driver pull-up from affecting the UV threshold. Select Diode D1 using the following criteria: $(V_F \times D1) + (V_{OL} \times EN) << 1.0\text{ V } (I_F = V_{IN}/R1)$

Ensure that the EN sink current does not exceed the specified V_{OL} value. If the open-drain device has no pull-up, the diode is not required.

POWER GOOD

The power good (PWRGD) output can be used to indicate whether the output voltage is above a user-defined threshold and can, therefore, be considered good. The PWRGD output is set by a resistor divider connected to the FB_PG pin (see Figure 42).

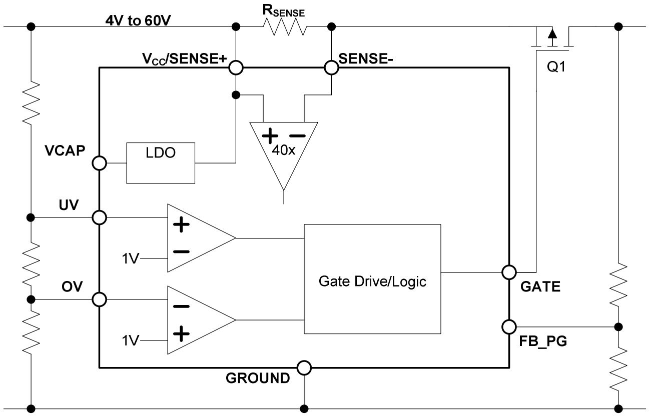
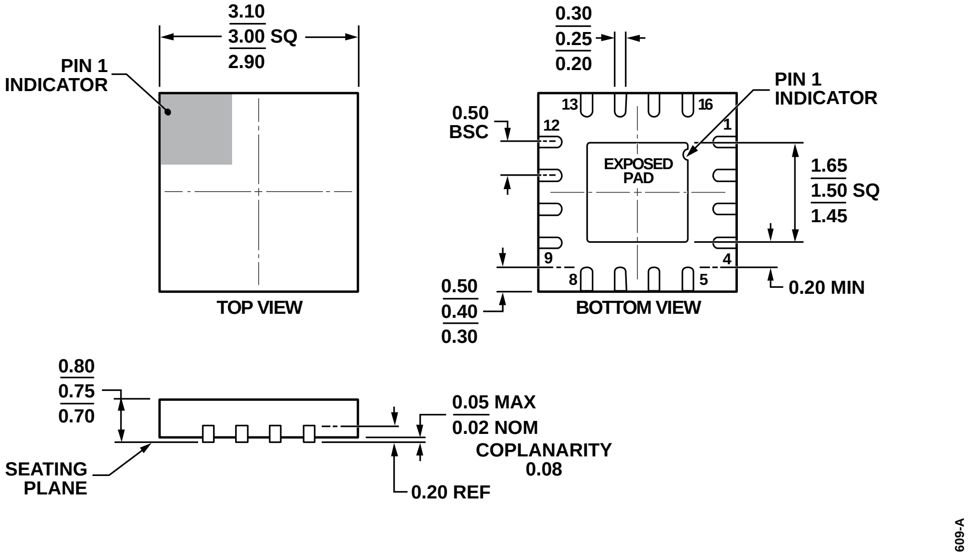


Figure 42. *Generation of PWRGD Signal*

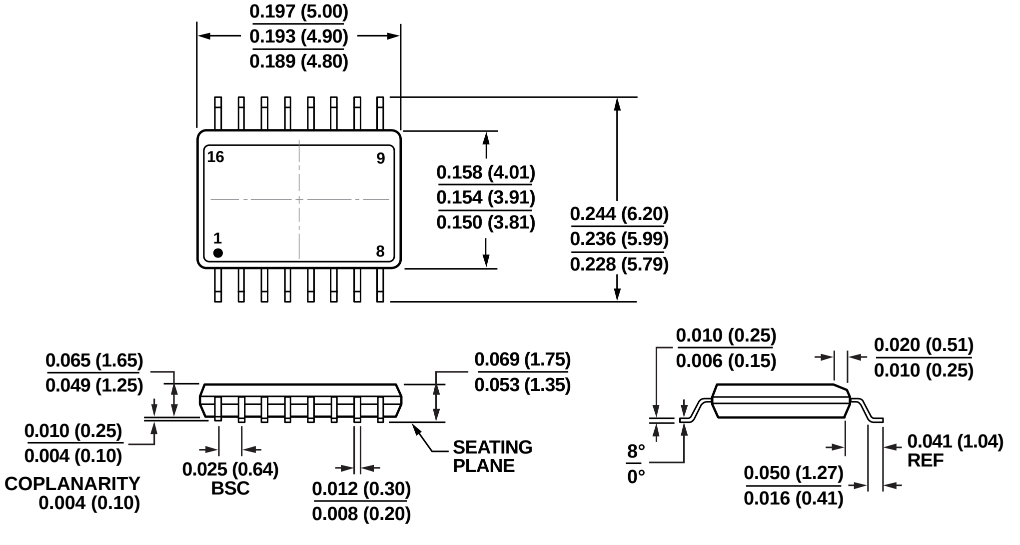
When the voltage at the FB_PG pin is above the 1 V threshold (indicating that the output voltage has risen), the open-drain pull-down is disabled, allowing PWRGD to be pulled high. The PWRGD pin is an open-drain output that pulls low when the voltage at the FB_PG pin is lower than the 1 V threshold minus the hysteresis (power bad). Hysteresis on the FB_PG pin is fixed at 30mV. PWRGD is guaranteed to be in a valid state for VCC ≥ 1.7 V.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229.

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very, Very Thin Quad
(CP-16-27)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 44. 16-Lead Body, Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Brand code
ADM1270ACPZ-R7	−40°C to +125°C	LFCSP	CP16-27	LNQ
ADM1270ARQZ-R7	−40°C to +125°C	QSOP	RQ-16	

Model[1]	Temperature Range	Package Description	Package Option	Brand code
ADM1270CP-EVALZ		Evaluation board		
ADM1270RQ-EVALZ		Evaluation board		

[1] Z = RoHS Compliant Part.

NOTES

PR12259-0-3/14(PrE)