AN3193
Application note

STM32L1xx
ultralow power features overview

Introduction

The STM32L1xx product line belongs to the STMicroelectronics ultralow power EnergyLite™ platform and complements the 8-bit STM8Lxx family with 32-bit high-performance Cortex™-M3 based microcontrollers offering an extended memory and bigger packages.

Both microcontroller families are based on the ST's proprietary 130 nm ultralow leakage process and have many analog and digital peripherals in common, which eases the transition from one architecture to the other and offers users the opportunity to capitalize on the knowledge acquired on one platform.

This application note describes the key low power features of the STM32L1xx family and explains their benefits for applications where energy consumption is a major concern.

Important note: This document is not intended to replace STM32L1xx datasheets. All values given in this document are for guidance only. Please refer to the related datasheet to get guaranteed values and up-to-date characterization data.

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1 STM32L1xx main features

Based on the solid foundations of the award-winning STM32F10x family, the STM32L1xx embeds various innovations which minimize the consumption in different configurations, while maintaining most of the existing peripherals and a quasi pin-to-pin compatibility.

For a given manufacturing process and die area, the consumption of a microcontroller largely depends on two factors which can be controlled dynamically: voltage and frequency. In the STM32L1xx devices, an internal low drop regulator supplies most of the logic circuitry with a fixed voltage: this guarantees that consumption is kept minimal whatever the supply voltage, along the lifetime of portable battery-supplied products, down to 1.65 V.

If we consider the clock sources, several cascaded clock prescalers, gating techniques and peripheral-by-peripheral clock management allow only the necessary logic gates to be activated, and at the adequate frequency. These are now design practices commonly used for reducing the consumption in Run mode. For the STM32L1xx, additional efforts have been done in this direction with the implementation of voltage scaling to reach an even higher processing efficiency.

However, all ultralow power requirements cannot be met by simply focusing on run time: for most applications, the challenge is to spend the minimum time and energy in this mode and find the adequate low power mode.

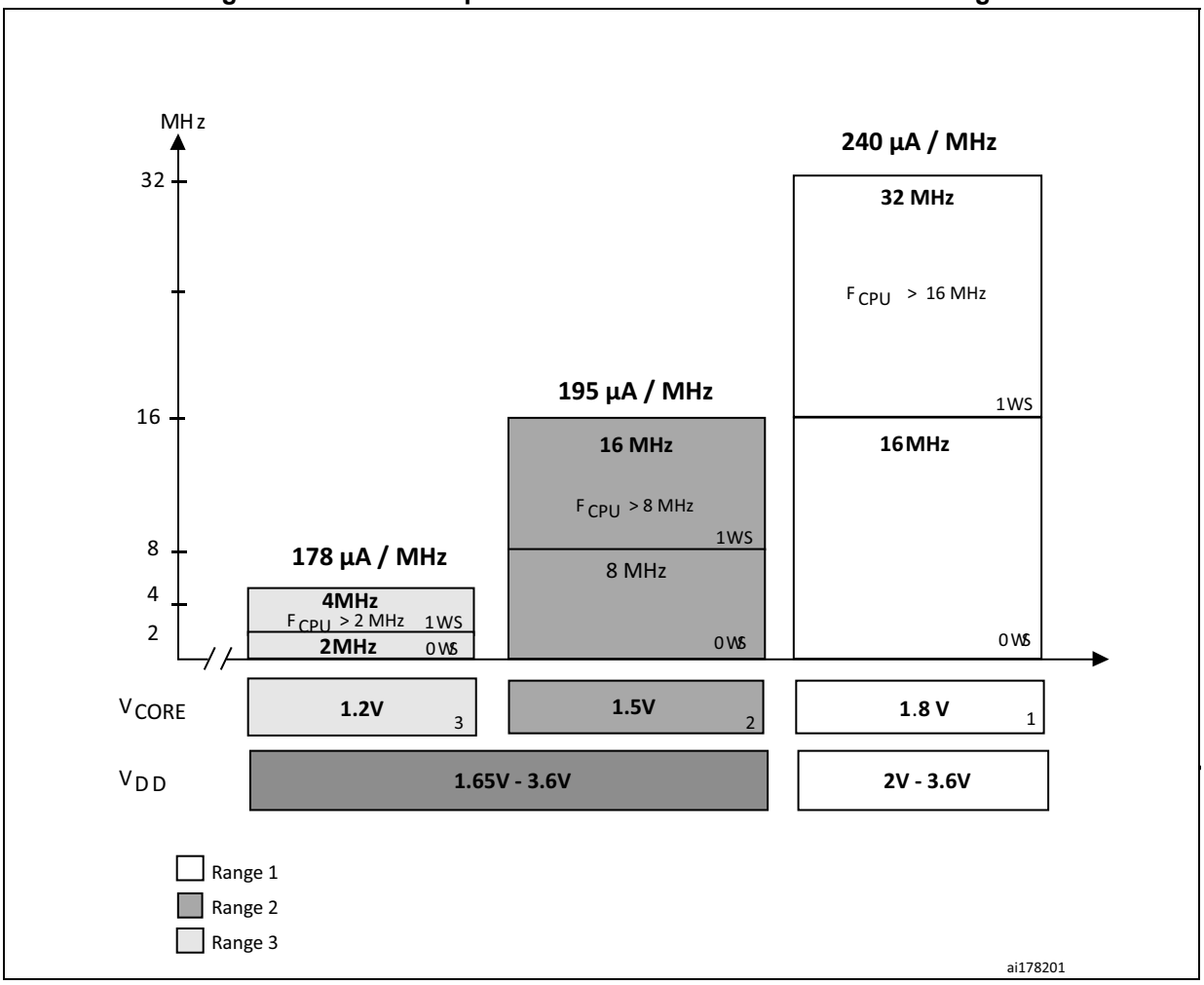
The improvements do not come only from the deep sleep modes optimized to eliminate every ten nA of leakage. The system has also been complemented with seven low power modes and a set of peripherals tuned for low power (such as the calendar real-time clock and glass LCD controller). These items are described in more detail hereafter.

2 Energy-efficient processing

The STM32L1 is built around the Cortex-M3, an industry standard 32-bit core, which has been designed, among other criteria, for low power applications. The Cortex-M3 offers a class-leading performance and code density. Although performance is not naturally linked with low current consumption, it is a key benefit for most of the low power applications which have to wake up periodically to execute software tasks. In this case, the Cortex-M3 spends less time in Run mode due to its processing performance, thus maximizing the time in deep sleep mode. If we consider only the processing consumption, expressed in mA/DMIPS (DMIPS standing for Dhrystone MIPS measured using the public benchmark Rev 2.0), the performance of the Cortex M3 is significantly better than that of the other architectures, in particular 16-bit microcontrollers.

The performance in DMIPS/MHz being given by the core and its memory interface, the processing consumption in mA/DMIPS can be maximized using voltage scaling. This method, also called undervolting, consists of adapting dynamically the supply voltage of the internal logic with the operating frequency. The STM32L1xx offers three dynamically selectable voltage ranges, as summarized in the following figure, from 1.8 V (range 1) down to 1.2 V (range 3), which offers a gain of more than 25% in terms of consumption.

Figure 1. STM32L1xx performance versus VDD and VCORE range



A typical example is portable healthcare equipment with USB device capability.

As long as it works in standalone mode, 4 MHz are sufficient to acquire and process the data from the analog front-end. In this case, the internal logic can be supplied with 1.2 V only.

However, executing a USB software stack when the system is connected to the USB interface of a PC requires more processing power: in this case, the device can be placed in "high-performance mode", where the internal voltage is 1.8 V. It can then execute code at 32 MHz while the USB peripheral is supplied by a 48-MHz clock. Voltage scaling is used to deal with the contradictory requirements of these two operating modes without having to compromise on the dynamic current consumption.

3 Numerous low power modes

At a higher architectural level, the power consumption of the STM32L1 can be modulated by entering one of seven low power modes. The power consumption can be reduced by progressively disabling the frequency-independent current sources (the clock sources, the non-volatile memory and the regulator) up to the point where most of the chip is powered down. The following table summarizes the features available for each mode and provides an indication of the current consumption.

Table 1. STM32L1xx low power mode overview

Low power mode	Consumption	CPU	Flash / EEPROM	RAM	DMA & Periph.	Clock	LCD	RTC
Sleep	100 µA/MHz (Range 1) 82 µA / MHz (Range 2) 65 µA/MHz (Range 3)	No	ON	ON	Active	Any	Available	
Low power run	10.4 µA (Flash OFF, 32 kHz)	Yes	ON or OFF	ON	Active	MSI	Available	
Low power sleep	5.1 µA (periph. OFF) 6.1 µA (1 timer ON)	No	OFF	ON	Active	MSI	Available	
Stop with RTC	1.3 µA (1.8 V) 1.6 µA (3 V)	No	OFF	ON	Frozen	LSE, LSI	Available	
Stop	500 nA	No	OFF	ON	Frozen	LSE, LSI	OFF	OFF
Standby with RTC	1.3 µA (3 V) 1 µA (1.8 V)	OFF	OFF	OFF	OFF	LSE, LSI	OFF	ON
Standby	270 nA	OFF	OFF	OFF	OFF	LSE, LSI	OFF	OFF

Two new modes have been implemented on the STM32L1xx in addition to the STM32F modes: the Low power run and Low power sleep modes. They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off (for instance communication peripherals or timers), or where the CPU is processing continuously at low speed to minimize current variations. Several functional blocks can be used to reach a very low current:

- The voltage regulator is in low power (LP) mode to reduce its quiescent current
- Non-volatile memory can be switched off, processing being done on the 16-Kbyte RAM
- The master clock source comes from the MSI internal RC oscillator, which can be reduced down to 1.5 µA.

The maximum current that the regulator can deliver in LP mode only limits the operating frequency and the number of peripherals that can be activated.

4 A set of peripherals tailored for low power

Several peripherals require special attention, either because of their intrinsic high consumption or because they are always powered up.

The STM32L1xx embeds a 12-bit / 1 MSps ADC. This very fast but accurate converter can jeopardize the battery lifetime if left powered-up continuously, with a 1.45 mA typical consumption. With its calibration-free architecture, fast power-up time of 3.5 µs and a conversion time of 1 µs, 6 conversions can be achieved within less than 10 µs, and the ADC can be shut down immediately afterwards. If this is done at a 1-kHz rate, it represents not more than 10.5 µA of the ADC related average consumption.

The time required to switch on and off a peripheral is negligible at high speed, but can become significant for a low operating frequency: at 1 MHz, each instruction lasts as long as the ADC conversion itself. When the ADC operates at such a low frequency, the conversion time is also significantly increased without benefits for the end application. To reduce the consumption and allow the most efficient use of this fast converter, the ADC digital interface has been designed to operate in a completely independent manner, at its maximum speed, whatever the CPU operating frequency (which can range from “sub-kHz” up to 32 MHz), using an internal 16 MHz clock source. It also includes auto shut-down modes to reduce the software overhead and to cope with a very low CPU frequency. At 32 kHz, each instruction lasts 30 µs: a burst of conversion can be launched between two cycles, with the ADC powered-off automatically, so that the ADC extra consumption can be limited to the necessary time only (for single conversions, during 4.5 µs out of the 30 µs CPU period).

Three peripherals have been developed to operate continuously even in Stop mode, where the system clock is stopped, with the main oscillator and memory powered down.

- A pair of ultralow comparators is available to monitor analog voltages with a current down to 3 µA. These comparators can wake up the MCU as soon as the external voltage reaches the selected threshold and they can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general purpose use.
- An RTC peripheral provides a clock/calendar with two alarms, includes a periodic wake-up unit and several application specific functions (timestamp, tamper detection …). It can remain enabled in the lowest power mode (standby) where most of the chip is powered down, and wake up the full MCU circuitry in case of an alarm or tamper detection for instance. It also contains 80 bytes of backup registers to store contextual information when exiting from standby mode. This peripheral has been designed using asynchronous design techniques to minimize its consumption (below 1 µA).
- The glass LCD is one of the most common displays in low power applications, because of its inherently low current consumption, low price and customization easiness. The STM32L1xx includes a versatile LCD controller, which can drive displays with up to 8 common lines and 40 segments, with the capability of selecting individually the I/O ports assigned to the LCD for an optimal use of the chip alternate functions. It also controls an optional internal step-up converter to maintain the LCD contrast on a wide range of V_{DD} values with consumptions as low as 5 µA (LCD consumption not included).

5 A versatile clock management

A reset and clock controller (RCC) peripheral manages the five possible clock sources of the STM32L1.

Two external oscillators can be used for applications requiring a high precision:

- The HSE clock (4-24 MHz high speed external clock), typically used to feed the PLL and to generate a CPU clock frequency of up to 32 MHz and a 48-MHz frequency for the USB controller.
- The LSE (typically 32.768 kHz low speed external clock) usually used to provide a low power clock source to the real time clock but which can also be used as LCD clock.

Three internal oscillators can be selected for various tasks:

- The LSI clock (37 kHz low speed internal clock) is a low accuracy ultralow power source that can feed the real time clock (with a limited accuracy), the LCD controller and the independent watchdog.
- The HSI clock (16 MHz high speed internal clock) is a high speed voltage-compensated oscillator.
- The MSI clock (64 kHz to 4 MHz multi speed internal clock) is a medium accuracy oscillator with adjustable frequency and low current consumption. It is designed to operate with a current proportional to the frequency, so as to minimize the internal oscillator consumption overhead for the low CPU frequencies. The following table summarizes the characteristics and uses of the various oscillators.

Table 2. STM32L1xx clock source characteristics (preliminary data(1))

Clock source	Use	Frequency	Consumption (typical)	Accuracy	Factory trimming	User trimmable
HSE	Master clock (+ RTC & LCD)	1-24 MHz	0.5 to 0.7 mA	Crystal dependent, down to tens of ppm	Not applicable	
LSE	RTC and LCD	32.768 kHz (typical)	0.45 µA (1.8 V) 0.6 µA (3 V)	Crystal dependent, down to a few ppm		
HSI	Master clock	16 MHz	100 µA	1% typical(2)	Yes(2)	Yes
MSI	Master clock	64 kHz 128 kHz 256 kHz 512 kHz 1.02 MHz 2.1 MHz 4.1 MHz	0.6 µA 0.9 µA 1.4 µA 2.2 µA 4 µA 7 µA 12 µA	0.5% typical	Yes	Yes
LSI	RTC, LCD & ind. WDG	38 kHz	0.4 µA (3 V)	-30% to +50%(3)	No	No, but f_{LSI} can be measured

1. Based on preliminary characterization or design simulations. See product datasheet for detailed electrical characteristics
2. On the Value Line family (STM32L100xx devices) the HSI oscillator is not trimmed, therefore please refer to device datasheet for the correct accuracy.
3. -10% to +4% drift after initial measurement

The price of a crystal oscillator may not be neglected in cost sensitive applications. For this reason, the STM32L1xx offers several options to measure the internal oscillators.

Although HSI and MSI are factory trimmed (except for the STM32L100 Value Line devices), they can be further trimmed by 0.5% steps during run time to compensate for frequency deviations due to temperature and voltage changes. Similarly, manufacturing process deviations of the LSI can be evaluated and compensated using a higher accuracy clock reference, either internally (HSI) or externally (LSE or HSE).

As an example, in an application where a 32.768 kHz crystal is used for the RTC, it is interesting to use the low power MSI oscillator which can provide a clock frequency of up to 4 MHz for the CPU with a typical consumption of 20 µA. Taking advantage of the high precision of the LSE crystals (typically a few tens of ppm), it is possible to determine the MSI frequency with the same resolution, and then to trim it on-the-fly.

6 Ultra-safe supply monitoring

The STM32L1xx includes a sophisticated supply supervisor module with several programmable options. This module is active during both power-on/down and run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) retrieved from the non-volatile memory to perform MCU initialization, even before the user's reset phase. This is also during this period that V_{DD} can be altered with glitches coming from the battery insertion or because of a weak power source.

The ultra safe power-on reset circuitry guarantees that the reset is released only if the V_{DD} is above 1.8 V, whatever the slope of the V_{DD} ramp-up phase, so that the circuit is within its guaranteed operating conditions when the program execution starts.

Once the power-up phase is completed, the user can choose to activate or not the brown-out reset (BOR) detector for a continuous battery monitoring, and select one of 5 thresholds. This is an option stored in the non-volatile memory to make this power supervision completely software independent. It is completed by a 7-level programmable voltage detector (PVD) that can be enabled by software to generate an early interrupt in case of a voltage drop.

The consumption of both the BOR and PVD modules is below 3 µA, when continuously powered, but it can remain significant in the deep sleep modes. If needed, the power supervision module can be programmed to have the BOR and the PVD disabled during the deep sleep phase and enabled again automatically on wake-up events. This minimizes the current consumption when the application is in idle mode (with usually a slightly higher and very stable supply due to an extremely light load). However, this does not jeopardize the safety when the execution starts again.

The STM32L1 is one of the few standard MCUs on the market with an operating range down to 1.65 V and only very few limitations (USB, ADC and DAC cannot be used but all other features are functional). A dedicated STM32L1xx device with permanently disabled BOR is available and can be used in applications with a voltage tolerance of 1.8 V $\pm$ 8%.

In this case, a "zero current" Power-on / Power-down reset (POR/PDR) module remains active and releases the reset after a hard-coded temporization. It is then up to the user to guarantee that the V_{DD} slope during the start-up is steep enough to reach at least 1.65 V when the reset vector is fetched.

7 Conclusion

The main features of the STM32L1xx devices are presented in this application note. They show the benefits offered by this microcontroller family to reduce the MCU's current consumption in embedded systems.

The STM32L1 family extends the ST's EnergyLite^{TM} platform for applications requiring additional memory sizes and bigger packages. It complements the STM32 portfolio keeping compatibility with other STM32 devices.

With its Cortex-M3 core and its energy-efficient architecture system, this microcontroller family supports low power modes without compromizing the processing performance.

Its rich set of peripherals can cover a wide range of applications, while numerous low power modes give a full flexibility to adjust on-the-fly the consumption to any task.

This results in an extended operating lifetime for today's and tomorrow's always greener applications.

8 Revision history

Table 3. Document revision history

Date	Revision	Changes
16-Apr-2010	1	Initial release.
20-Sep-2013	2	Changed to apply to all STM32L1 family.