



U74AHCT1G02

CMOS IC

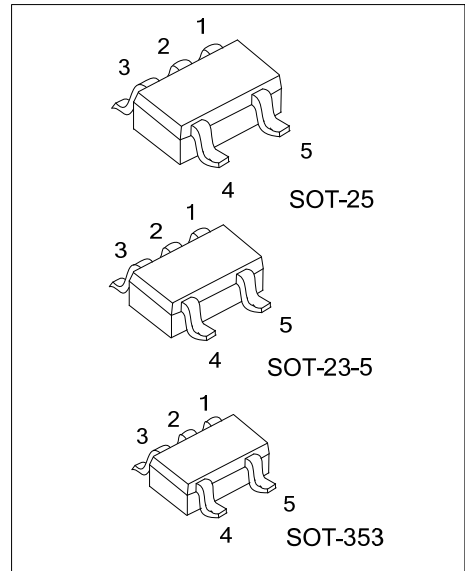
2-INPUT NOR GATE

DESCRIPTION

The **U74AHCT1G02** is a single 2-input NOR gate which provides the Function.

FEATURES

- * Operation Voltage Range: 2.0~5.5V
- * Low Power Dissipation
- * High noise immunity
- * Balanced propagation delays
- * Specified from -40 to +125°C

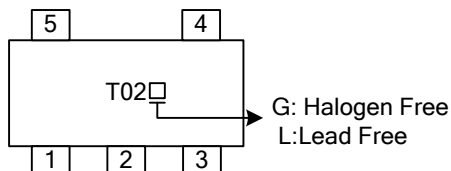


ORDERING INFORMATION

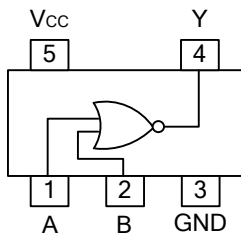
| Ordering Number | | Package | Packing |
|--------------------|--------------------|----------|-----------|
| Lead Free | Halogen Free | | |
| U74AHCT1G02L-AE5-R | U74AHCT1G02G-AE5-R | SOT-23-5 | Tape Reel |
| U74AHCT1G02L-AF5-R | U74AHCT1G02G-AF5-R | SOT-25 | Tape Reel |
| U74AHCT1G02L-AL5-R | U74AHCT1G02G-AL5-R | SOT-353 | Tape Reel |

| | |
|--|--|
| <p>U74AHCT1G02L-AF5-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p> | <p>(1) R: Tape Reel (2) AE5: SOT-23-5, AF5: SOT-25, AL5: SOT-353 (3) G: Halogen Free, L: Lead Free</p> |
|--|--|

MARKING



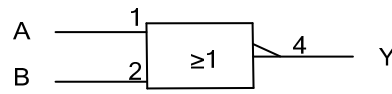
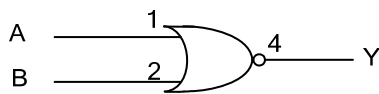
■ PIN CONFIGURATION



■ FUNCTION TABLE

| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

■ LOGIC DIAGRAM (positive logic)



IEC logic symbol

■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---------------------------|-----------|--------------------|------|
| Supply Voltage | V_{CC} | -0.5~7 | V |
| Input Voltage | V_{IN} | -0.5~7 | V |
| Output Voltage | V_{OUT} | -0.5~ $V_{CC}+0.5$ | V |
| Input Clamp Current | I_{IK} | ±20 | mA |
| Output Clamp Current | I_{OK} | ±20 | mA |
| Continuous Output Current | I_{OUT} | ±25 | mA |
| V_{CC} or GND Current | I_{CC} | ±50 | mA |
| Storage Temperature | T_{STG} | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------|-----------------------|-----|-----|----------|------|
| Supply Voltage | V_{CC} | | 4.5 | 5.0 | 5.5 | V |
| Input Voltage | V_{IN} | | 0 | | 5.5 | V |
| Output Voltage | V_{OUT} | | 0 | | V_{CC} | V |
| Input Transition Rise or Fall Times | t_R, t_F | $V_{CC}=3.3V\pm 0.3V$ | | | | ns/V |
| | | $V_{CC}=5V\pm 0.5V$ | | | 20 | |
| Operating Temperature | T_A | | -40 | 25 | 125 | °C |

■ ELECTRICAL CHARACTERISTICS

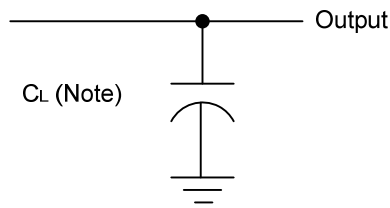
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---------------|---|------|-----|------|------|
| High-Level Input Voltage | V_{IH} | $V_{CC}=4.5V\sim 5.5V$ | 2.0 | | | V |
| Low-Level Input Voltage | V_{IL} | $V_{CC}=4.5V\sim 5.5V$ | | | 0.8 | V |
| High-Level Output Voltage | V_{OH} | $V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OH}=-50\mu A$ | 4.4 | 4.5 | | V |
| | | $V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OH}=-8mA$ | 3.94 | | | |
| Low-Level Output Voltage | V_{OL} | $V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OL}=50\mu A$ | | 0 | 0.1 | V |
| | | $V_{CC}=4.5V, V_{IN}=V_{IH}$ or $V_{IL}, I_{OL}=8mA$ | | | 0.36 | V |
| Input Leakage Current | $I_{I(LEAK)}$ | $V_{CC}=5.5V, V_{IN}=V_{IH}$ or V_{IL} | | | ±0.1 | μA |
| Quiescent Supply Current | I_Q | $V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$ | | | 1 | μA |
| Additional Quiescent Supply Current | ΔI_Q | $V_{CC}=5.5V, V_{IN} = 3.4 V$; other inputs at V_{CC} or GND, $I_{OUT}=0$ | | | 1.35 | mA |
| Input Capacitance | C_{IN} | | | 1.5 | 10 | pF |

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ SWITCHING CHARACTERISTICS (Input signal: $P_{RR}\leq 1MHz, Z_o=50\Omega, t_R\leq 3ns, t_F\leq 3ns.$)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--------------------|-------------------------------------|-----|-----|-----|------|
| Propagation Delay Times | t_{PLH}/ t_{PHL} | $V_{CC}=4.5V\sim 5.5V, C_L = 15 pF$ | | 3.5 | 5.5 | ns |
| | | $V_{CC}=4.5V\sim 5.5V, C_L = 50 pF$ | | 4.9 | 7.5 | ns |

■ TEST CIRCUIT AND WAVEFORMS



Note: CL includes probe and jig capacitance.

Fig.1 Load circuitry for switching times.

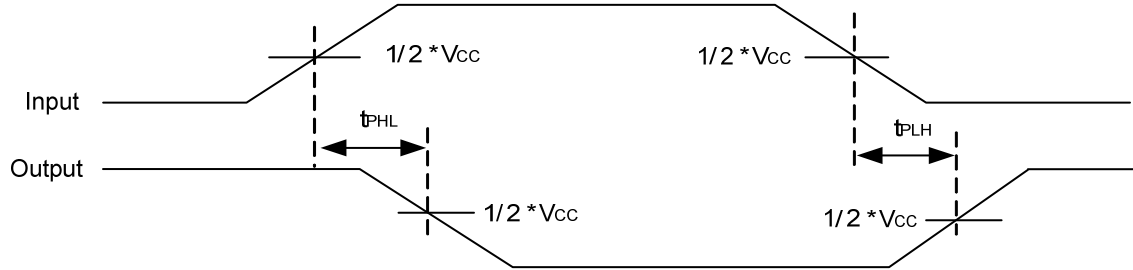


Fig. 2 Propagation delay from input(A and B) to output(Y)

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