2x20W Stereo Digital Audio Amplifier With 20 Bands EQ Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 99dB (PSNR), 104dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for at 24V
  10W x 2CH into 8Ω @0.17% THD+N for stereo
  20W x 2CH into 8Ω @0.26% THD+N for stereo
- Sound processing including：
  20 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step),
  Dynamic range control (DRC)
  Dual band dynamic range control
  Power clipping
  3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

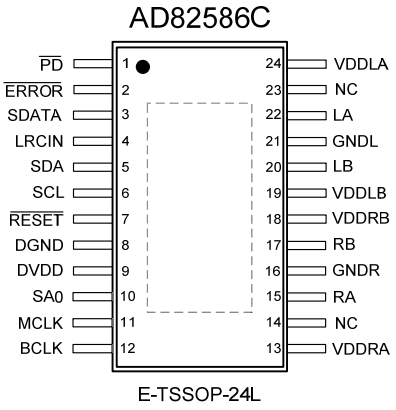
Description

AD82586C is a digital audio amplifier capable of driving a pair of 8Ω, 20W operating at 24V supply without external heat-sink or fan requirement with play music.

AD82586C can provide advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I^2C control interface.

Robust protection circuits are provided to protect AD82586C from damage due to accidental erroneous operating condition. AD82586C is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD82586C is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

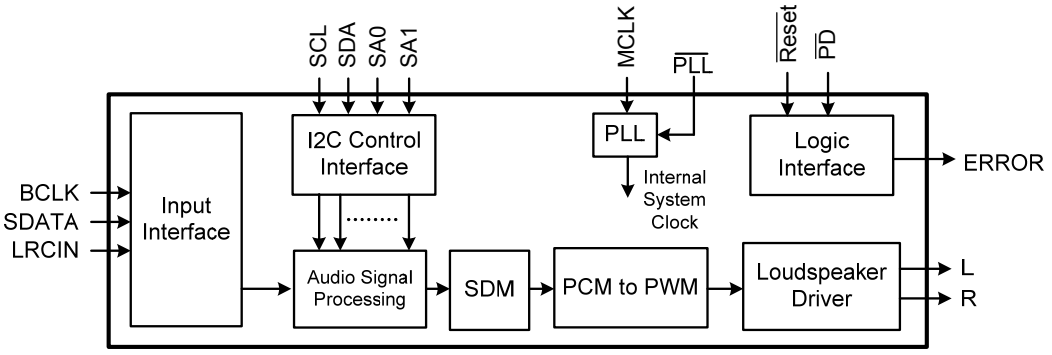
Pin Assignment



Pin Description

Pin	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
2	$\overline{ERROR}$	O	Error status, low active	Open-drain output
3	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
4	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
5	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
6	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
7	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
8	DGND	P	Digital Ground	
9	DVDD	P	Digital Power	
10	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
11	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
12	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
13	VDDRA	P	Right channel supply A	
14	N.C.	NC		
15	RA	O	Right channel output A	
16	GNDR	P	Right channel ground	
17	RB	O	Right channel output B	
18	VDDRB	P	Right channel supply B	
19	VDDLB	P	Left channel supply B	
20	LB	O	Left channel output B	
21	GNDL	P	Left channel ground	
22	LA	O	Left channel output A	
23	N.C.	NC		
24	VDDL	P	Left channel supply A	

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82586C-QG24NAT	E-TSSOP 24L	62 Units / Tube 100 Tubes / Small Box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-TSSOP 24L	AD82586C	26.8	0.24	27.1	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings (<100msec)* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
VDDL/R	Supply for Driver Stage	-0.3	30	V
DVDD	Supply for Digital Circuit	-0.3	3.6	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C