AN2485
Application note

400 W FOT-controlled PFC pre-regulator with the L6563

Introduction

This application note describes an evaluation board based on the Transition-mode PFC controller L6563 and presents the results of the bench evaluation. The board implements a 400 W, wide-range mains input, a PFC pre-conditioner suitable for ATX PSU, or a flat screen display. The chip is operated with Fixed-Off-Time control in order to use a low-cost device like the L6563 which is usually prohibitive at this power level. Fixed-Off-Time control allows Continuous Conduction Mode operation which is normally achieved with more expensive control chips and more complex control architectures.

L6563 400W FOT PFC Demo board (EVAL6563-400W)

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1 Main characteristics and circuit description

The main characteristics of the SMPS are:

- Line voltage range: 90 to 265 Vac
- Minimum line frequency (f_L): 47 Hz
- Regulated output voltage: 400 V
- Rated output power: 400 W
- Maximum $2f_L$ output voltage ripple: 10 V pk-pk
- Hold-up time: 22 ms (V_{DROP} after hold-up time: 300 V)
- Maximum switching frequency: 85 kHz (@Vin=90 Vac, Pout=400 W)
- Minimum estimated efficiency: 90% (@Vin=90 Vac, Pout=400 W)
- Maximum ambient temperature: 50 °C
- EMI: in acc. with EN55022 Class-B
- PCB type and size: Single side, 70 um, CEM-1, 148.5 x 132 mm
- Low profile design: 35 mm component maximum height

The evaluation board implements a Power Factor Correction (PFC) pre-regulator delivering 400 W continuous power on a regulated 400 V rail from a wide range mains voltage. The board provides for the reduction of the mains harmonics which allows meeting the standards of the European norm EN61000-3-2 or the Japanese norm JEIDA-MITI. This rail is the input for the cascaded isolated DC-DC converter that provides the output rails required by the load.

The board is equipped with enough heat sinking to allow full-load operation in still air. With an appropriate airflow, and without any change in the circuit, the evaluation board can easily deliver up to 450 W.

The controller is the L6563 (U1), integrating all the functions needed to control the PFC stage and to interface with the downstream converter. The L6563 controller chip is designed for Transition-Mode (TM) operation, where the boost inductor works next to the boundary between Continuous (CCM) and Discontinuous Conduction Mode (DCM). However, with a slightly different usage, the chip can operate so that the boost inductor works in CCM, surpassing the limitations of TM operation in terms of power handling capability. The gate-drive capability of the L6563 is also adequate to drive the MOSFETs used at higher power levels. This approach, which couples the simplicity and cost-effectiveness of TM operation with the high-current capability of CCM operation, is the Fixed-Off-Time (FOT) control. The control modulates the ON-time of the power switch, while its OFF-time is kept constant. More precisely, the Line-Modulated FOT (LM-FOT), where the OFF-time of the power switch is not rigorously constant but is modulated by the instantaneous mains voltage, will be used. Please refer to AN1792 ("Design of Fixed-Off-Time-Controlled PFC Pre-regulators with the L6562") for a detailed description of this technique as indicated in *Section 9: References* (point 2).

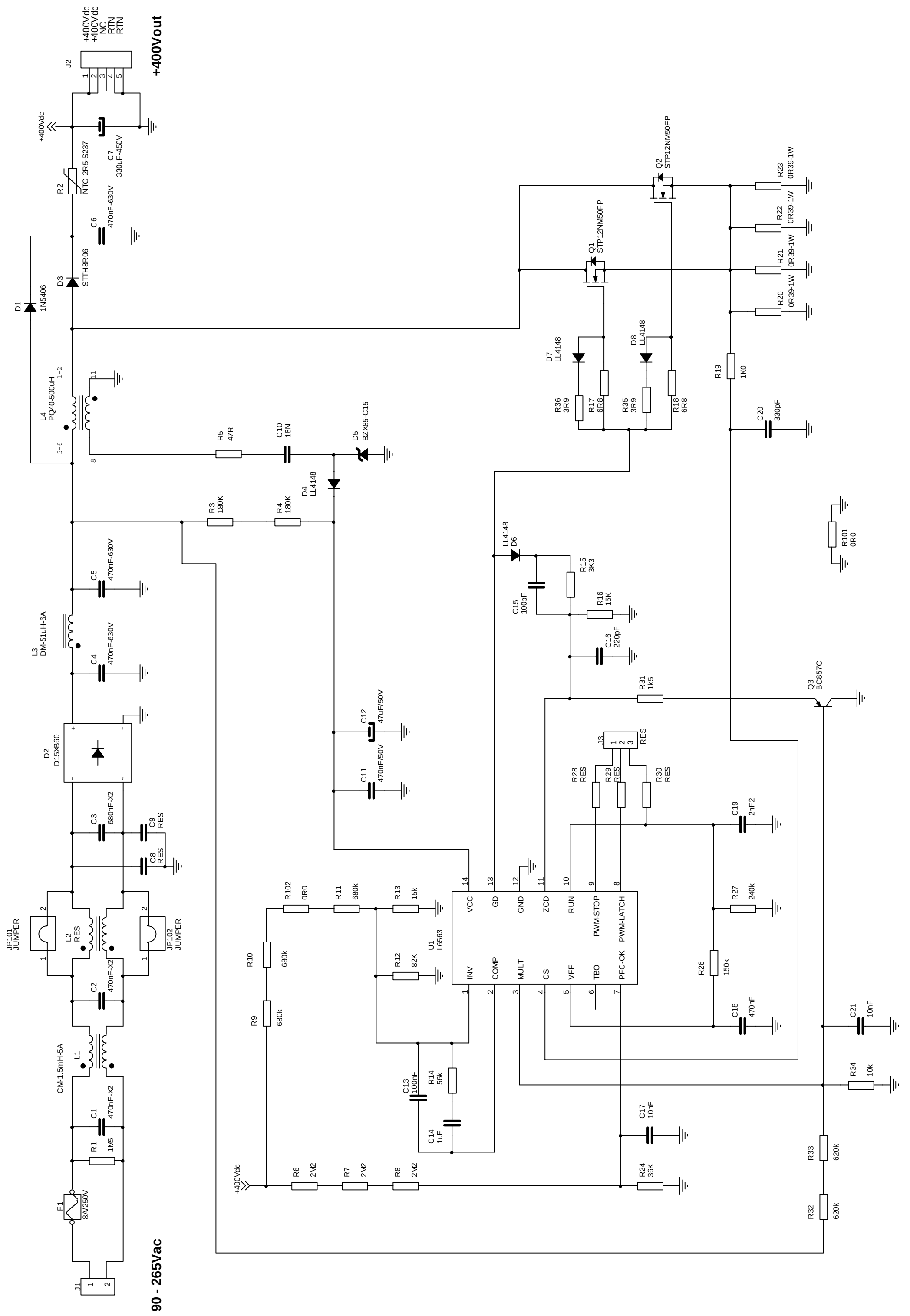
The power stage of the PFC is a conventional boost converter, connected to the output of the rectifier bridge D2. It includes the coil L4, the diode D3 and the capacitors C6 and C7. The boost switch is represented by the power mosfets Q1 and Q2. The NTC R2 limits the inrush current at switch on. It has been connected on the DC rail, in series to the output electrolytic capacitor, in order to improve efficiency during low line operation. Additionally, the splitting in two of output capacitors (C6 and C7) provides for managing the AC current mainly by the film capacitor C7 which allows for a less costly electrolytic to bear only the DC part.

At start-up the L6563 is powered by the Vcc capacitor (C12) that is charged via the resistors R3 and R4. The L4 secondary winding (pins #8-11) and the charge pump circuit (R5, C10, D5 and D4) generate the Vcc voltage powering the L6563 during normal operations.

The divider R32, R33 and R34 provides the L6563 multiplier with the information of the instantaneous voltage that is used to modulate the boost current. The instantaneous voltage information is also used to get the average value of the AC line by the V_{FF} (Voltage Feed-Forward) pin. Divider R9, R10, R11, R12, and R13 is dedicated to sense output voltage while divider R6, R7, R8, and R24 is dedicated to protect the circuit in case of voltage loop failures. The Line-Modulated FOT is obtained by the timing generator components D6, C15, R15, C16, R16, R31, and Q3.

The board is equipped with an input EMI filter designed for a 2-wire input mains plug. It is composed of two stages, a Common Mode Pi-filter connected at the input (C1, L1, C2, C3) and a Differential Mode Pi-filter after the input bridge (C4, L3, C5). The board also offers the possibility to easily connect a downstream converter and test the interface signals managed by the L6563.

Figure 1. EVAL6563-400W evaluation board: electrical schematic



2 Test results and significant waveforms

2.1 Harmonic content measurement

One of the main purposes of a PFC pre-conditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of European and Janapese regulations. The board has been tested according to European norm EN61000-3-2 Class-D and Japanese norm JEIDA-MITI Class-D, at full load and 70 W output power, at both the nominal input voltage mains.

As shown in *Figure 2*, *3*, *4*, and *5*, the circuit is able to reduce the harmonics well below the limits of both regulations from full load down to light load. 70 W of output power has been chosen because it is almost the lower power limit at which the harmonics must be limited according to these international norms.

Figure 2. EVAL6563-400W compliance to EN61000-3-2 at 230 Vac-full load

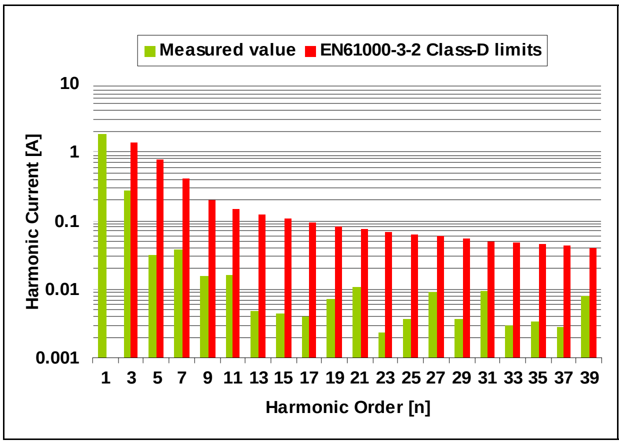


Figure 3. EVAL6563-400W compliance to JEIDA-MITI at 100 Vac-full load

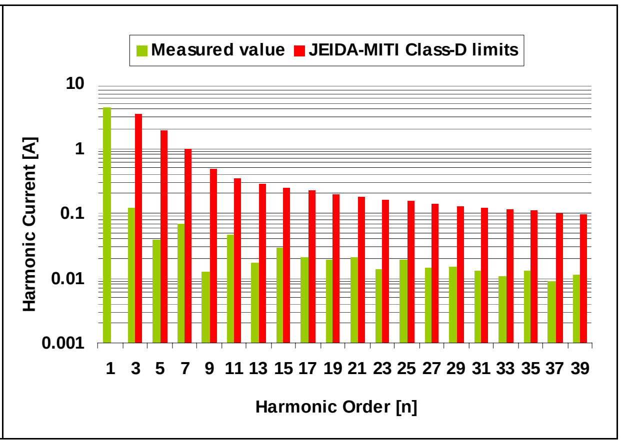


Figure 4. EVAL6563-400W compliance to EN61000-3-2 at 230 Vac-70 W load

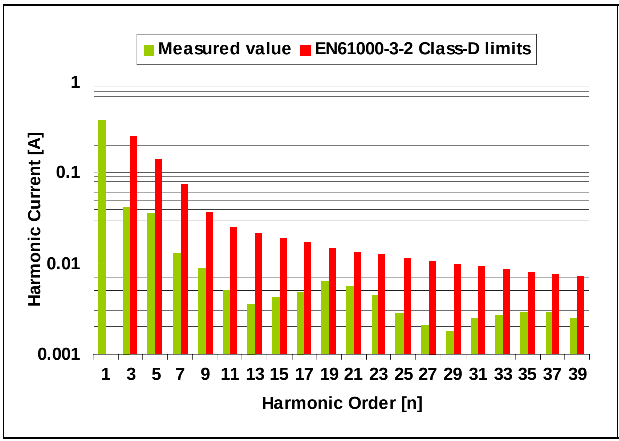
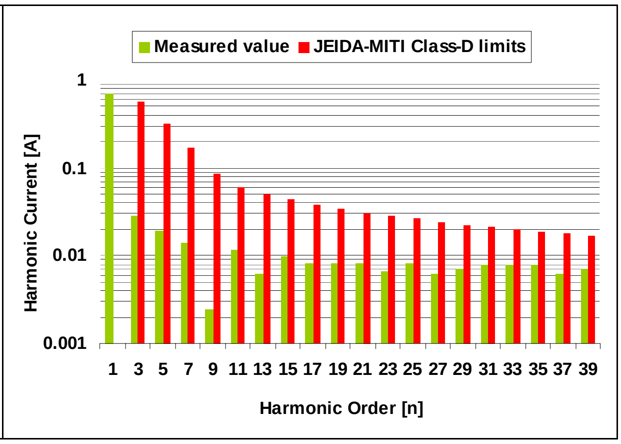


Figure 5. EVAL6563-400W compliance to JEIDA-MITI at 100 Vac-70 W load



For user reference, waveforms of the input current and voltage at the nominal input voltage mains and different load conditions are given in *Figure 6*, *7*, *8*, *9*, *10*, and *11*.

Figure 6. EVAL6563-400W Input current waveform at 100 V - 60 Hz - 400 W load

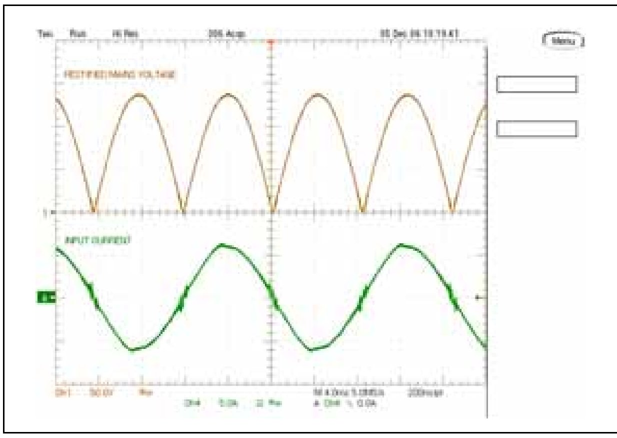


Figure 7. EVAL6563-400W Input current waveform at 230 V - 50 Hz - 400 W load

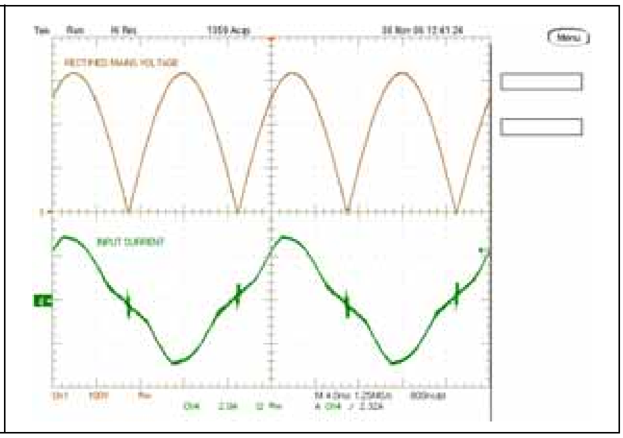


Figure 8. EVAL6563-400W Input current waveform at 100 V - 60 Hz - 200 W load

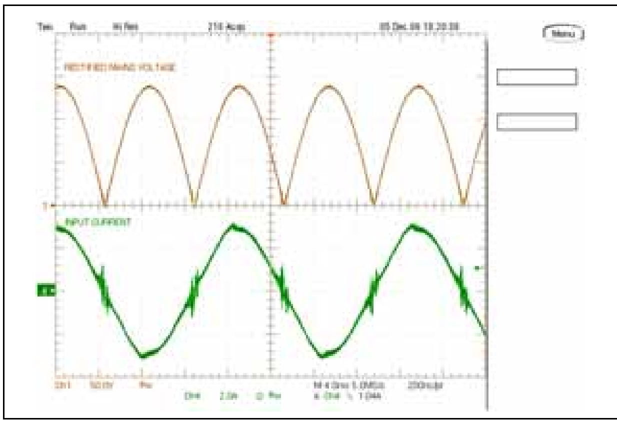


Figure 9. EVAL6563-400W Input current waveform at 230 V - 50 Hz - 200 W load

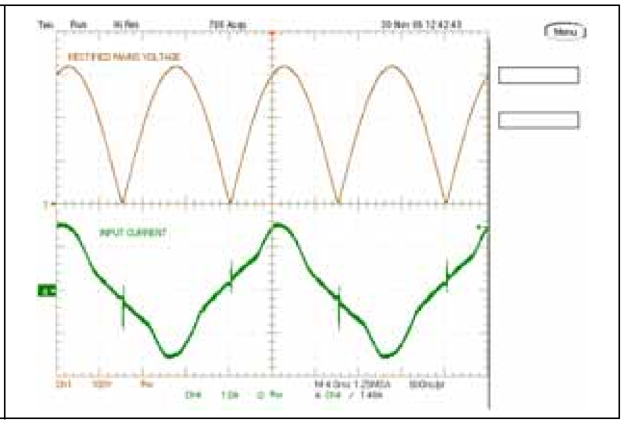


Figure 10. EVAL6563-400W Input current waveform at 100 V - 60 Hz - 70 W load

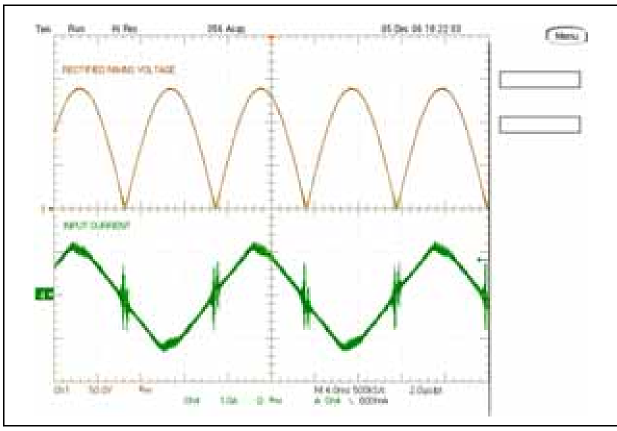
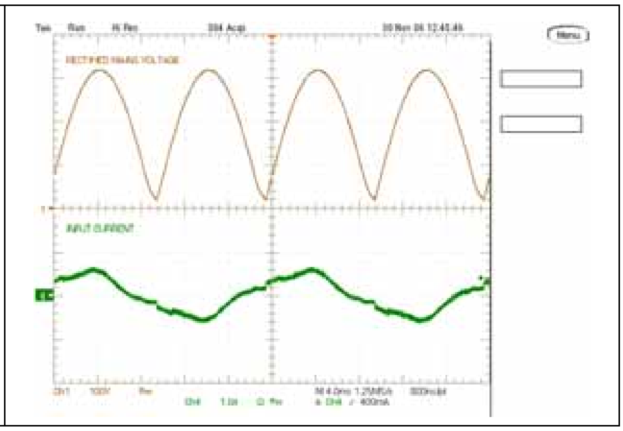


Figure 11. EVAL6563-400W Input current waveform at 230 V - 50 Hz - 70 W load



The Power Factor (PF) and the Total Harmonic Distortion (THD) have been measured too and the results are reported in *Figure 12.* and *Figure 13.* As shown, the PF at full load and half load remains close to unity throughout the input voltage mains range while it decreases at high mains range when the circuit is delivering 70 W. THD is low, remaining within 25% at maximum input voltage.

Figure 12. Power Factor vs. Vin and load

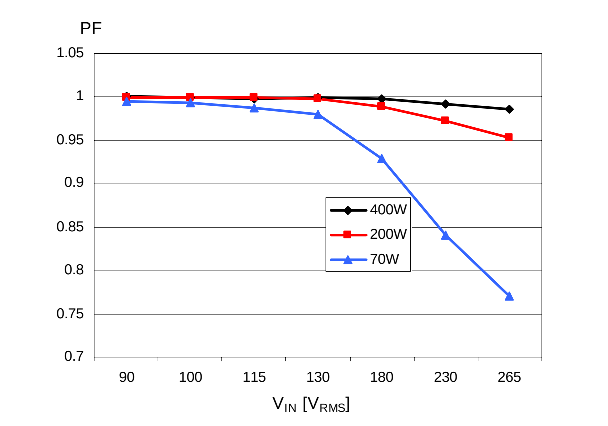
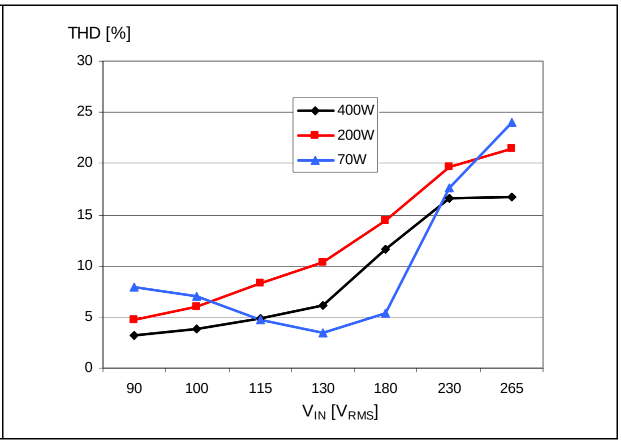


Figure 13. THD vs. Vin and load



Efficiency is very good at all load and line conditions. At full load it is always significantly higher than 90%, making this design suitable for high efficiency power supply.

The measured output voltage variation at different line and load conditions is given in *Figure 15.* As shown, the voltage is perfectly stable over the input voltage range due to the Voltage Feed-Forward function embedded in the L6593. Only at 265 Vac and light load, there is a negligible deviation of 1 V due to the intervention of the burst mode (for the "static OVP") function.

Figure 14. Efficiency vs. Vin and load

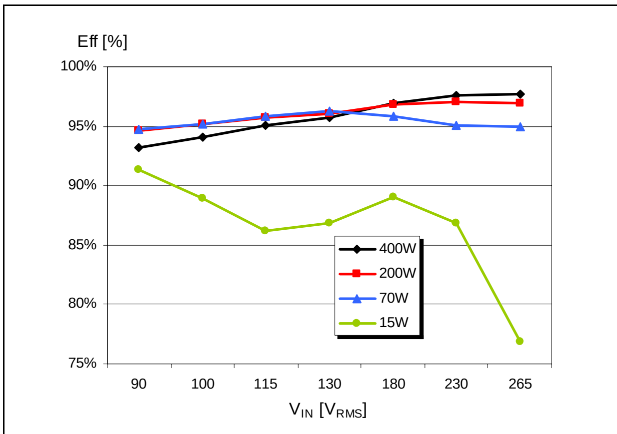
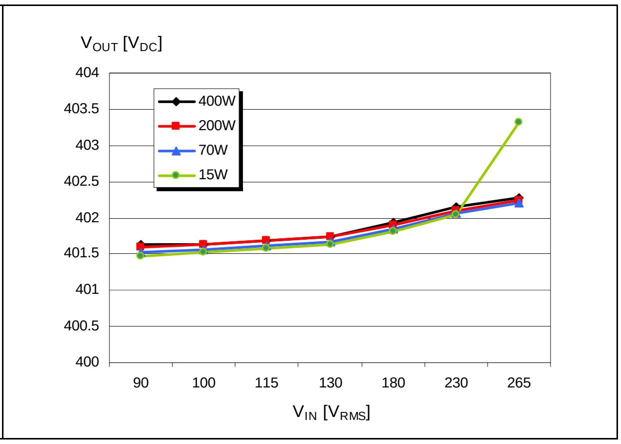


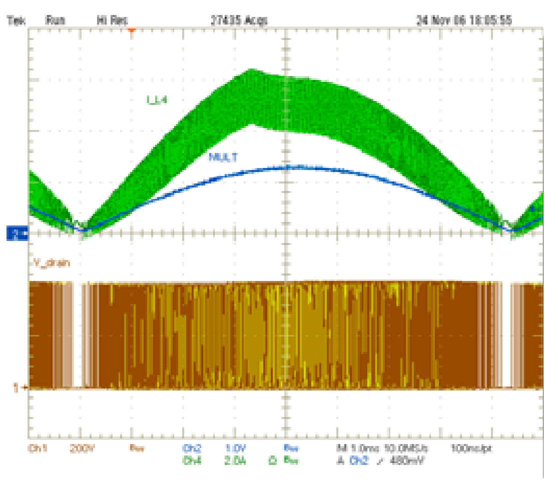
Figure 15. Static Vout regulation vs. Vin and load



2.2 Inductor current in FOT and L6563 THD optimizer

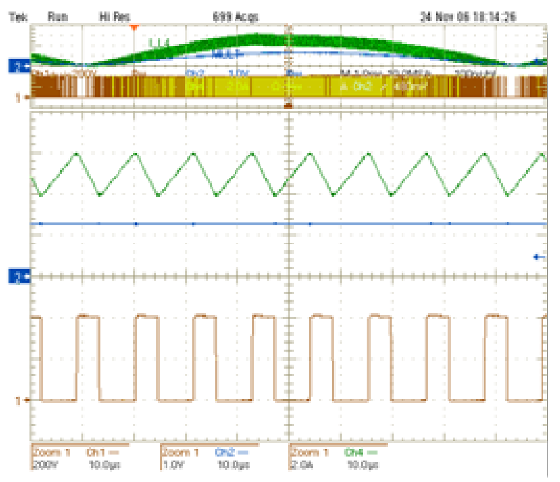
Figure 16, *17*, *18*, and *19* show the waveforms relevant to the inductor current at different voltage mains. As shown in *Figure 16.* and *Figure 18.*, the inductor current waveform over a line half-period is very similar to that of a CCM PFC. It is also possible to note the transition angle from DCM to CCM that occurs closer to the zero crossing of the current sine wave at low mains and move toward the top if the circuit is working at high mains. In *Figure 17.* and *Figure 19.* the magnification of the waveforms at the peak of the sine wave, shows the different ripple current and Off-times, which is modulated by the input mains voltage.

Figure 16. EVAL6563-400W Inductor current ripple envelope at 115 Vac - 60 Hz - full load



CH1: Q1/Q2 Drain voltage
CH2: MULT voltage - pin #3
CH4: L4 inductor current ripple envelope

Figure 17. EVAL6563-400W Inductor current ripple (detail) at 115 Vac - 60 Hz - full load



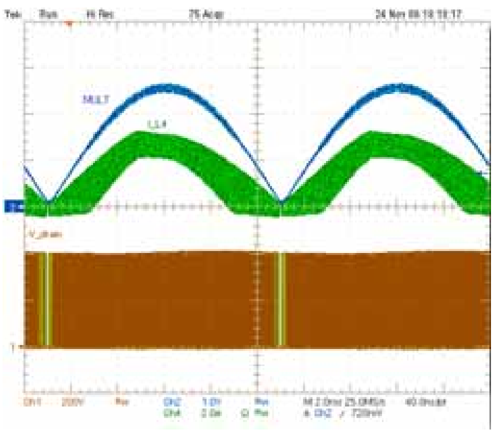
CH1: Q1/Q2 Drain voltage
CH2: MULT voltage - pin #3
CH4: L4 inductor current ripple envelope

On both the drain voltage traces reported in *Figure 16.* and *Figure 18.*, close to the zero crossing points of the sine wave, it is possible to note the action of the THD optimizer embedded in the L6563. It is a circuit that minimizes the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way, the THD (Total Harmonic Distortion) of the current is considerably reduced. A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop. To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop.

The result is both a minimization of the time interval where energy transfer is lacking and a full discharge of the high-frequency filter capacitor after the bridge. Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. The offset is modulated by the voltage on the V_{FF} pin, so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

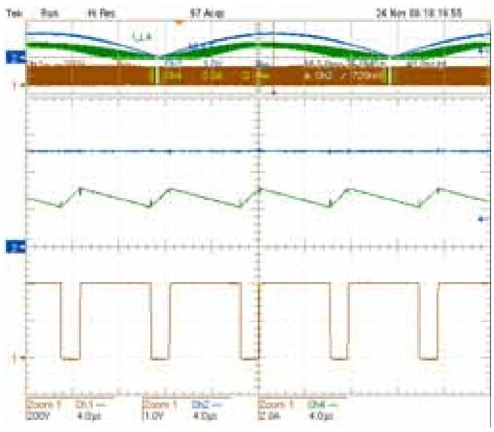
In order to maximize the benefit from the THD optimizer circuit, the high-frequency filter capacitors after the bridge rectifier should be minimized, compatible with EMI filtering needs. A large capacitance in fact introduces a conduction dead-angle of the AC input current in itself thus reducing the effectiveness of the optimizer circuit.

Figure 18. EVAL6563-400W Inductor current ripple envelope at 230 Vac - 50 Hz - full load



CH1: Q1/Q2 Drain voltage
CH2: MULT voltage - pin #3
CH4: L4 inductor current ripple envelope

Figure 19. EVAL6563-400W Inductor current ripple (detail) at 230 Vac - 50 Hz - full load



CH1: Q1/Q2 Drain voltage
CH2: MULT voltage - pin #3
CH4: L4 inductor current ripple envelope

2.3 Voltage feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage as well as the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get fc = 20 Hz at 264 Vac means having fc = 4 Hz at 88 Vac, which results in sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. A fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

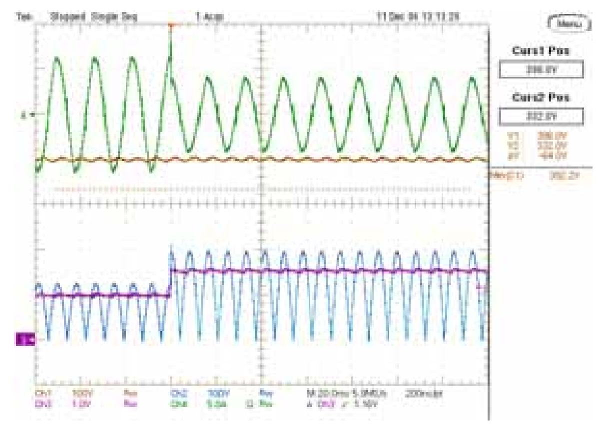
Voltage Feedforward can compensate for the gain variation with the line voltage and provides a solution to the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop. In this way a change of the line voltage will cause an inversely proportional change of the half sine amplitude at the output of the multiplier so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

The L6563 achieves Voltage Feedforward with a technique that makes use of just two external parts and limits the feedforward time constant trade-off issue to only one direction. A capacitor C_{FF} (C18) and a resistor R_{FF} (R26 + R27), both connected to the V_{FF} pin (#5), complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (pin #3). R_{FF} provides a means to discharge C_{FF} when the line voltage decreases. In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode and no appreciable overshoot is visible at the pre-regulator's output. In case of line voltage drop, C_{FF} is discharged with the time constant $R_{FF}\cdot C_{FF}$, which can be in the hundred ms to achieve an acceptably low steady-state ripple and have low current distortion. The dynamics of the voltage feed-forward input is limited downwards at 0.5 V, that is, the output of the multiplier no longer increases if the voltage on the V_{FF} pin is below 0.5 V. This helps to prevent excessive power flow when the line voltage is lower than the minimum specified value.

The behavior of the EVAL6563-400W demo board in case of an input voltage surge from 90 to 140 Vac is shown in *Figure 20.* The graph shows that the V_{FF} function provides for the stability of the output voltage which is not affected by the input voltage surge. In fact, thanks to the V_{FF} function, the compensation of the input voltage variation is very fast and the output voltage remains perfectly stable at its nominal value. The opposite is confirmed in *Figure 21.* which shows the behavior of a PFC using the L6562 working in FOT and delivering a similar output power. In case of a mains surge the controller cannot compensate for it, and the output voltage stability is guaranteed by the feedback loop only. Unfortunately, as previously stated, its bandwidth is poor therefore the output voltage has a significant deviation from the nominal value.

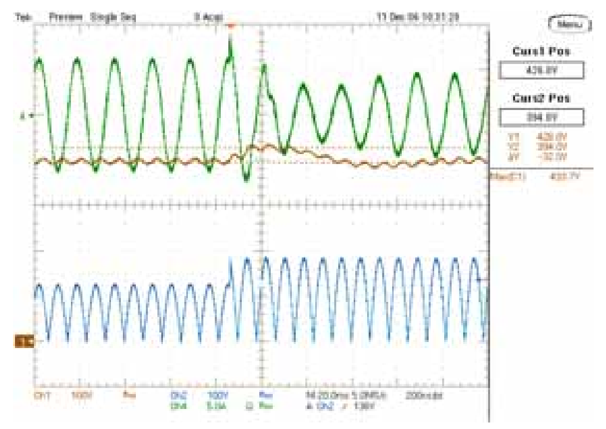
The circuit has the same behavior in case of mains surge at any input voltage, and it is not affected if the input mains surge happens at any point on the input sine wave.

Figure 20. EVAL6563-400W Input mains surge from 90 Vac to 140 Vac - full load - C_{FF} = 470 nF



CH1: Output voltage
CH2: Input rectified mains voltage
CH3: V_{FF} voltage - pin #5
CH4: Input current

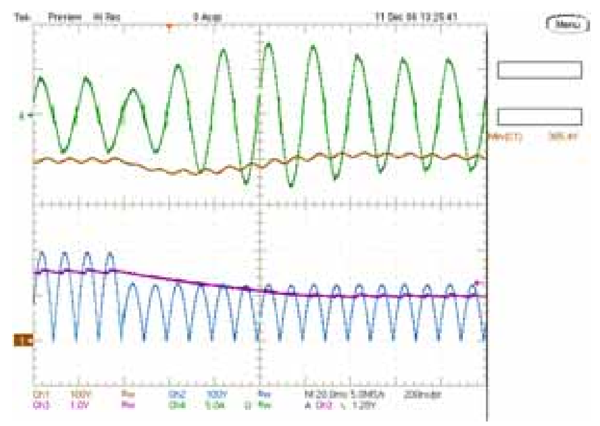
Figure 21. L6562 FOT Input mains surge from 90 Vac to 140 Vac - full load - NO V_{FF} input



CH1: Output voltage
CH2: Input rectified mains voltage
CH3: V_{FF} voltage - pin #5
CH4: Input current

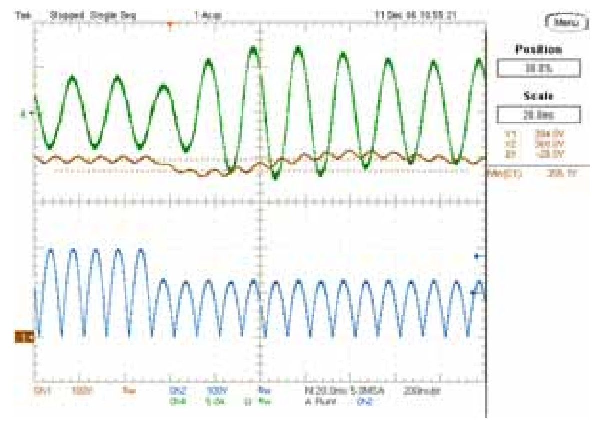
Figure 22. shows the circuit behavior in case of mains dip. As previously described, the time constant of the V_{FF} pin provides a very fast compensation in case of surge, which is the most critical transition, and a slower compensation in case of mains dip. As shown, in that case the output voltage changes, but in few mains cycles it returns to the nominal value. A controller without the V_{FF} function will instead perform differently. In *Figure 23.* the behavior of a PFC using the L6562 working in FOT and delivering a similar output power is shown. In case of a mains dip, the output voltage variation is larger and the output voltage requires more time to return to the original value.

Figure 22. EVAL6563-400W Input mains dip from 140 Vac to 90 Vac - full load - C_{FF} = 470 nF



CH1: Output voltage
CH2: Input rectified mains voltage
CH3: V_{FF} voltage - pin #5
CH4: Input current

Figure 23. L6562 FOT Input mains dip from 90 Vac to 140 Vac - full load - NO V_{FF} input

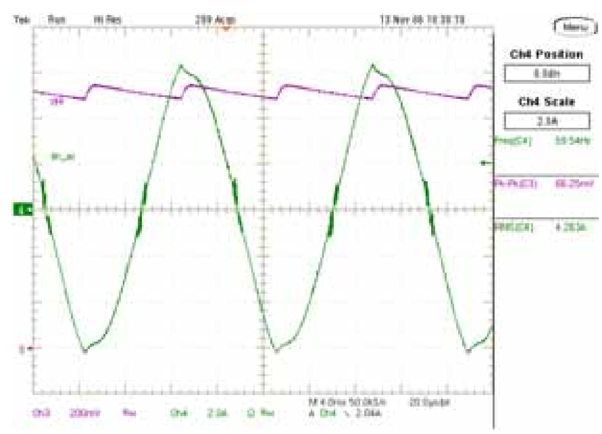


CH1: Output voltage
CH2: Input rectified mains voltage
CH3: V_{FF} voltage - pin #5
CH4: Input current

Deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If the time constant is too small the voltage generated will be affected by a considerable amount of ripple at twice the mains frequency so causing distortion of the current reference (resulting in high THD and poor PF). If the time constant is too large there will be a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot or undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly, a trade-off is required.

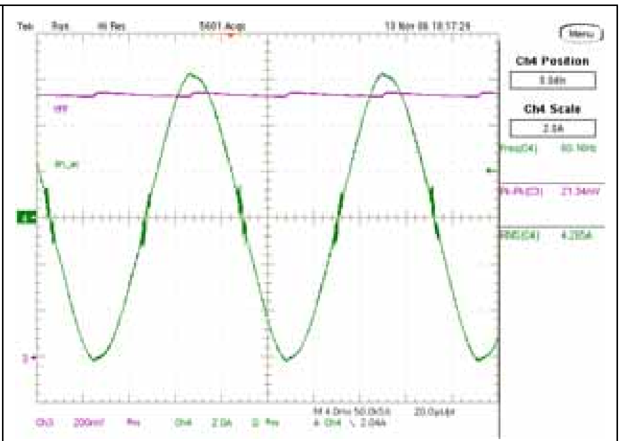
For reference, *Figure 24.* and *Figure 25.* compare the input current shape and the measurement of the THD and 3^{RD} Harmonic amplitude for different C_{FF} values. *Figure 25.* shows that increasing 3 times the C_{FF} capacitor improves the current shape and both the THD and the third harmonic current are also decreased, but not very significantly. The time constant used for V_{FF} (C_{FF} = 470 nF, R_{FF} = 150 K+240 K) is a good compromise.

Figure 24. EVAL6563-400W Input current shape at 100 Vac-60 Hz vs. V_{FF} ripple - C_{FF} = 470 nF



THD [%]: 3.39% - 3RD harmonic: 0.126 A
CH3: V_{FF} voltage - pin #5
CH4: Input current

Figure 25. EVAL6563-400W Input current shape at 100 Vac-60 Hz vs. V_{FF} ripple - C_{FF} = 1.5 uF

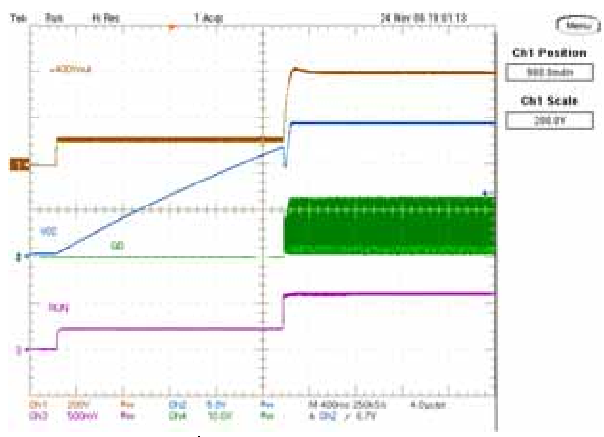


THD [%]: 2.75% - 3RD harmonic: 0.109 A
CH3: V_{FF} voltage - pin #5
CH4: Input current

2.4 Start-up and RUN pin

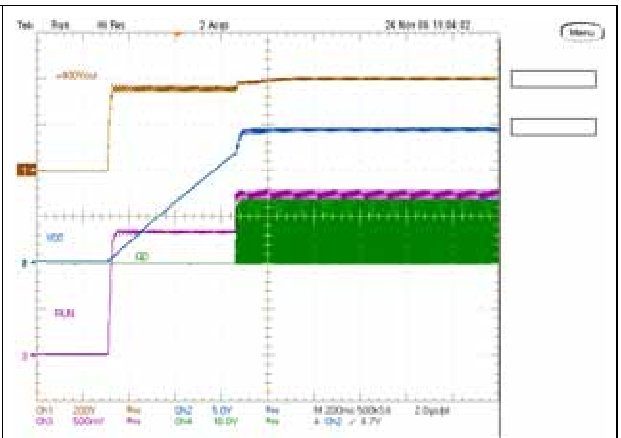
Figure 26. and *Figure 27.* detail the waveforms during the start-up of the circuit, at mains plug-in. The Vcc voltage rises to the turn-on threshold, and the L6563 starts the operation. For a short time the energy is supplied by the Vcc capacitor, then the auxiliary winding and the charge pump circuit take over. At the same time, the output voltage rises from peak value of the rectified mains to the nominal value of the PFC output voltage. The good margin phase of the compensation network allows a clean start-up, without any large overshoot that would trigger the Dynamic and Static over voltage protection.

Figure 26. EVAL6563-400W start-up at 90 Vac-60 Hz - full load



CH1: Output voltage
CH2: Pin #14 - Vcc voltage
CH3: Pin #10 - RUN
CH4: Pin #13 - Gate drive

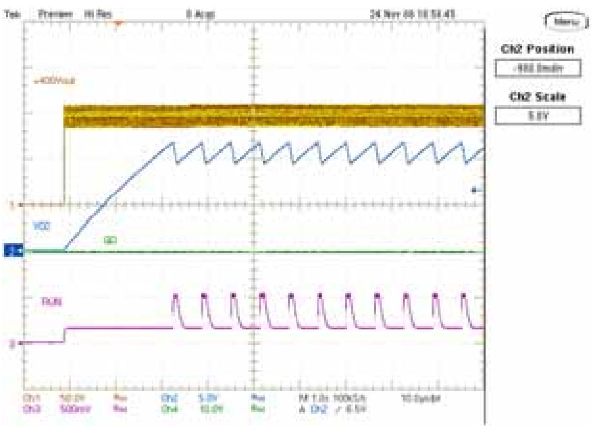
Figure 27. EVAL6563-400W start-up at 265 Vac-50 Hz - full load



CH1: Output voltage
CH2: Pin #14 - Vcc voltage
CH3: Pin #10 - RUN
CH4: Pin #13 - Gate drive

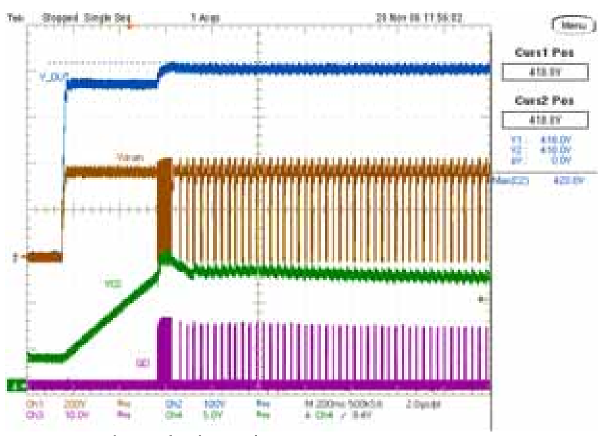
A dangerous event for any PFC is the operation during an undervoltage of the mains. This condition may cause overheating of the primary power section due to an excess of RMS current. To prevent the PFC from this abnormal operation a brownout protection is needed. It is basically a not-latched shutdown function that must be activated when a condition of mains under voltage is detected. The L6563 has a dedicated inhibit pin (RUN, #10), embedding a comparator with hysteresis, stopping the L6563 operation if the voltage applied is below its threshold. Because the L6563 V_{FF} pin delivers a voltage signal proportional to the input mains, the complete brownout function can be easily implemented using a simple resistor divider connected between the V_{FF} and the RUN pins. In this demo board, the divider resistors setting the turn-on threshold are R26 and R27 on the schematic in *Figure 1.* In *Figure 28.* a start-up tentative below the threshold shows that the RUN pin does not allow the IC operation.

Figure 28. EVAL6563-400W start-up at 80 Vac-60 Hz - full load



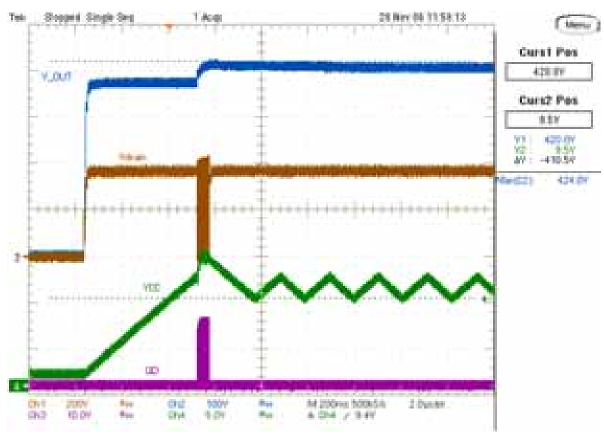
2.5 Start-up at light load

Figure 29. EVAL6563-400W Start-up at 265 V - 50 Hz - 30 mA load



CH1: Q1/Q2 drain voltage
CH2: Output voltage
CH3: Pin #13 - Gate drive
CH4: Pin #14 - Vcc voltage

Figure 30. EVAL6563-400W start-up at 265 V - 50 Hz - no load

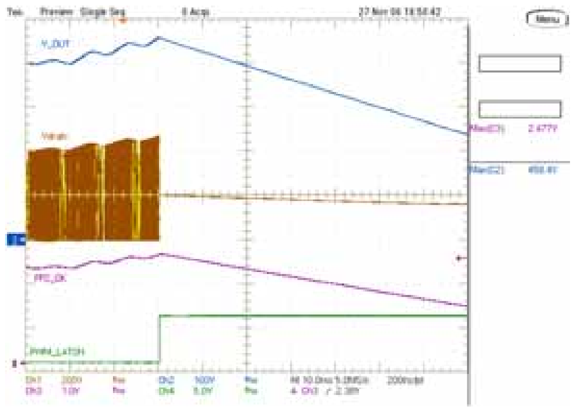


CH1: Q1/Q2 drain voltage
CH2: Output voltage
CH3: Pin #13 - Gate drive
CH4: Pin #14 - Vcc voltage

The board, as is, is able to properly handle an output load as low as 12 W. With lower load levels the system will not start up correctly at high line because burst pulses last so long that the Vcc voltage drops below the UVLO of the L6563. In that condition, if the load increases suddenly, the PFC output voltage drops until the IC resumes normal operation. Supplying the L6563 from an external source (typically it's the auxiliary voltage powering the controller of the downstream converter or of an auxiliary power supply), the minimum load that can be properly handled goes to virtually zero.

2.6 Open loop protection

Figure 31. EVAL6563-400W open loop at 115 Vac-60 Hz - full load



The L6563 is equipped with an OVP, which monitors the current flowing through the compensation network and entering in the error amplifier (pin COMP, #2). When this current reaches about 18 µA, the output voltage of the multiplier is forced to decrease, thus reducing the energy drawn from the mains. If the current exceeds 20 µA, the OVP is triggered (Dynamic OVP), and the external power transistor is switched off until the current falls approximately below 5 µA. However, if the overvoltage persists (in case the load is completely disconnected, for example), the error amplifier eventually saturates low and triggers an internal comparator (Static OVP) that keeps the external power switch turned off until the output voltage returns close to the regulated value.

The OVP function is able to handle "normal" overvoltage conditions, that is, those resulting from an abrupt load/line change or occurring at start-up. It cannot handle the overvoltage generated, for instance, when the upper resistor of the output divider fails open. The voltage loop can no longer read the information on the output voltage and forces the PFC pre-regulator to work at maximum ON-time, causing the output voltage to rise with no control. A pin of the L6563 (PFC_OK, #7) is dedicated to providing an additional monitoring of the output voltage with a separate resistor divider (R6, R7, R8 high, R24 low, see *Figure 1.*). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum Vo that can be expected (including worst-case load/line transients).

If V_O = 400 V, Vox = 460 V, select R6+R7+R8 = 6.6 MΩ. Three resistor in series have been chosen according to their voltage rating, so R24 = 6.6 MΩ ·2.5/(460-2.5) = 36 KΩ

When the OVP function is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 250 µA, and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. At the same time the pin PWM_LATCH (pin #8) is asserted high. PWM_LATCH is an open source output able to deliver 3.7 V min. with 0.5 mA load, intended for tripping a latched shutdown function of the PWM controller IC in the cascaded DC-DC converter, so that the entire unit is latched off. To restart the system, it is necessary to recycle the input power, so that the Vcc voltages of both the L6563 and the PWM controller go below their respective UVLO thresholds.

The PFC_OK pin doubles its function as a not-latched IC disable. A voltage below 0.2 V shuts down the IC, reducing its consumption below 1 mA. In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin go above 0.26 V.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open (or the PFC_OK (#7) pin is floating) results in shutting down the L6563 and stopping the pre-regulator.

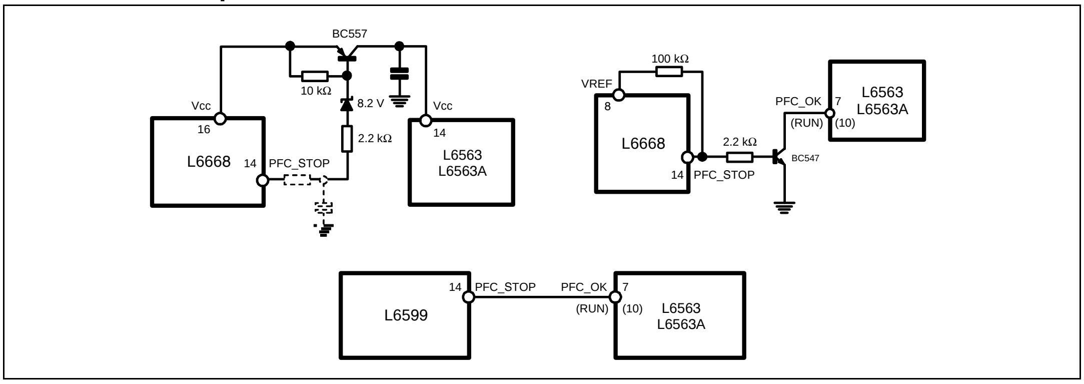
The event of an open loop is shown in *Figure 31.* The protection intervention stops the operation of the L6563 and the activation of the PWM_LATCH pin.

2.7 Power management/housekeeping functions

A special feature of the L6563 is that it facilitates the implementation of the "housekeeping" circuitry needed to coordinate the operation of the PFC stage to that of the cascaded DCDC converter. The housekeeping circuitry functions ensure that transient conditions like power-up or power down sequencing or failures of power stage are properly handled. The L6563 provides some pins for these functions.

One communication line between the L6563 and the PWM controller of the cascaded DC-DC converter is the PWM_LATCH pin (#8), which is normally open when the PFC works properly. It goes high if the L6563 loses control of the output voltage (because of a failure of the control loop) or if the boost inductor saturates. Its aim is to latch off the PWM controller from the cascaded DC-DC converter as well. A second communication line can be established via the disable function included in the RUN pin. Typically, this line is used to allow the PWM controller of the cascaded DC-DC converter to shut down the L6563 in case of light load, in order to minimize the no-load input consumption of the power supply.

Figure 32. L6563 On/Off control by a cascaded converter controller via PFC_OK or RUN pin

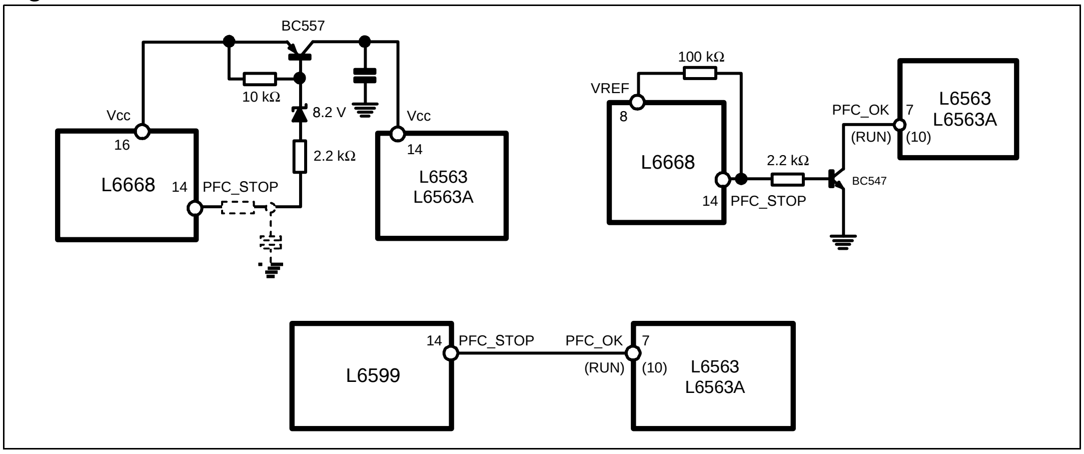


The third communication line is the PWM_STOP pin (pin #9), which works in conjunction with the RUN pin (pin #10). The purpose of the PWM_STOP pin is to inhibit the PWM activity of both the PFC stage and the cascaded DC-DC converter.

The PWM_STOP pin is an open collector, normally open, that goes low if the device is disabled by a voltage lower than 0.52 V on the RUN pin (#10). It is important to point out that this function works correctly in systems where the PFC stage is the master and the cascaded DC-DC converter is the slave or, in other words, where the PFC stage starts first, powers both controllers and enables/disables the operation of the DC-DC stage. This function is quite flexible and can be used in different ways. In systems comprising an auxiliary converter and a main converter (e.g. desktop PC's silver box or Hi-end Flat-TV or monitor), where the auxiliary converter also powers the controllers of the main converter, the pin RUN (#10) can be used to start and stop the main converter. In the simplest case, to enable/disable the PWM controller the PWM_STOP (#9) pin can be connected to either the output of the error amplifier or, if the chip is provided with it, to its soft-start pin.

The EVAL6563-400W offers the possibility to test the housekeeping functions by connecting them to the cascaded converter via the series resistors R28, R29, R30. Regarding the PWM_STOP (#9) pin that is an open collector type, if it needs a pull-up resistor, connect it close to the cascaded PWM for better noise immunity.

Figure 33. Interface circuits that let the L6563/A switch on or off a PWM controller



3 Layout hints

The layout of any converter is a very important phase in the design process which may not always have the necessary attention required by the engineers. Even if it the layout phase appears time-consuming, a good layout does save time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages and subsequently provides consistent cost savings.

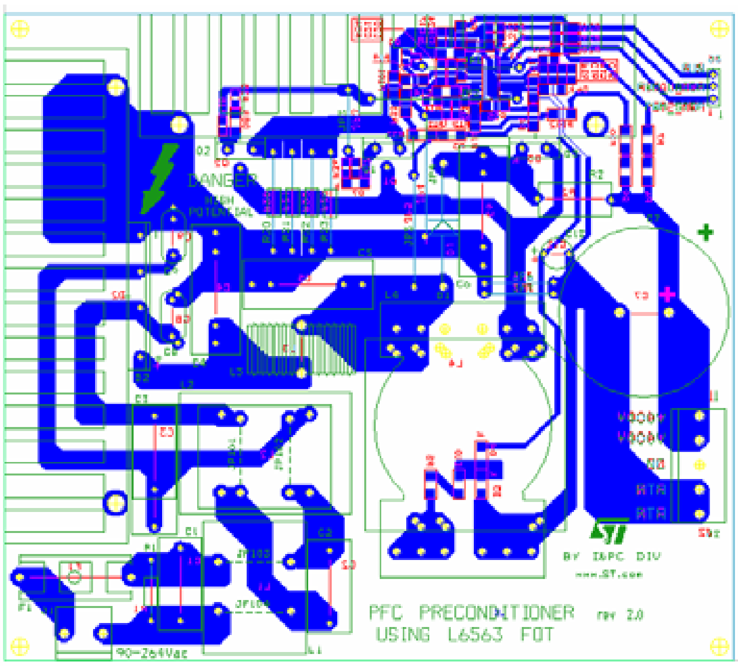
The L6563 does not need any special attention to the layout, but the general layout rule for any power converter must be applied carefully. Basic rules using the EVAL6563-400W schematic as a reference are listed below. They can be used for other PFC circuits having any power level, working either in FOT or TM control.

1. Keep power and signal RTN separated. Connect the return pins of components carrying high current such as C4, C5, sense resistors, C6 and C7 as close as possible.

This point is the RTN star point. A downstream converter must be connected to this return point.

2. Minimize the length of the traces relevant to L3, boost inductor L4, boost rectifier D4 and output capacitor C6 and C7.
3. Keep signal components as close as possible to L6563 pins. Keep the tracks relevant to the pin #1 (INV) net as short as possible. Components and traces relevant to the Error Amplifier must be placed far from traces and connections carrying signals with high dv/dt like Mosfet Drains (Q1 and Q2).
4. Connect heat sinks to Power GND.
5. Add an external shield to the boost inductor and connect it to Power GND.
6. Connect the RTN of signal components including the feedback, PFC_OK and MULT dividers close to the L6563 pin #12 (GND).
7. Connect a ceramic capacitor (100÷470 nf) to pin #14 (Vcc) and to pin #12 (GND), close to the L6563 connect this point to the RTN star point (see point *1.*).

Figure 34. EVAL6563-400W PCB layout (not 1:1 scaled)



4 Audible noise

Differential mode currents in a circuit with high frequency and low frequency components (like in a PFC) may produce audible noise due to inter-modulation between operating frequency and mains line frequency.

The phenomenon is produced because of mechanical vibration of reactive components like capacitors and inductors. Current flowing in the winding can cause vibration of wires or ferrite which produces buzzing noise, therefore, to avoid this boost and filter inductors have to be wound with correct wire tension, and the component has to be varnished or dipped. Frequently, X-Capacitors and Filter Capacitors after bridge generate acoustic noise because of AC current that causes the electrodes to vibrate and produce buzzing (noise). Thus, minimize AC current inserting a differential mode, Pi-filter between the bridge and the boost inductor helps to reducing the acoustic noise and additionally the EMI filter will benefit too. Such actions decrease significantly the ripple current that otherwise has to be filtered by the EMI filter. The capacitors selected are polypropylene, preferably dipped type, because boxed ones are generally more at risk to generate acoustic noise.

The acoustic noise can also be due to an incorrect circuit behavior for an abnormal current modulation. It can be due to the Dynamic OVP intervention that stops the IC switching cycles which consequently creates a discontinuity of the input line current shape that can produce vibrations as described above, occurring typically at light load. In this case, only a board re-layout can help, taking into consideration the points outlined in *Section 3: Layout hints*. In addition, grounding the boost inductor may help, because in this case we decrease the emissions from the most efficient "antenna" of our circuit. In fact, in case of improper layout some picofarads of layout parasitic capacitance together with the very high dV/dt of the MOSFET Drain voltage may inject noise somewhere in the circuit.

5 Thermal measures

In order to check the design reliability, a thermal mapping by means of an IR Camera was done. *Figure 35.* and *Figure 36.* show thermal measures on board component side at nominal input voltages and full load. Captions visible on the pictures placed across key components show the relevant temperature. *Table 1.* provides the correlation between measured points and components for both thermal maps. The ambient temperature during both measurements was 27°C. According to these measurement results all components of the board are working within their temperature limits.

Figure 35. Thermal map at 115 Vac-60 Hz - full load

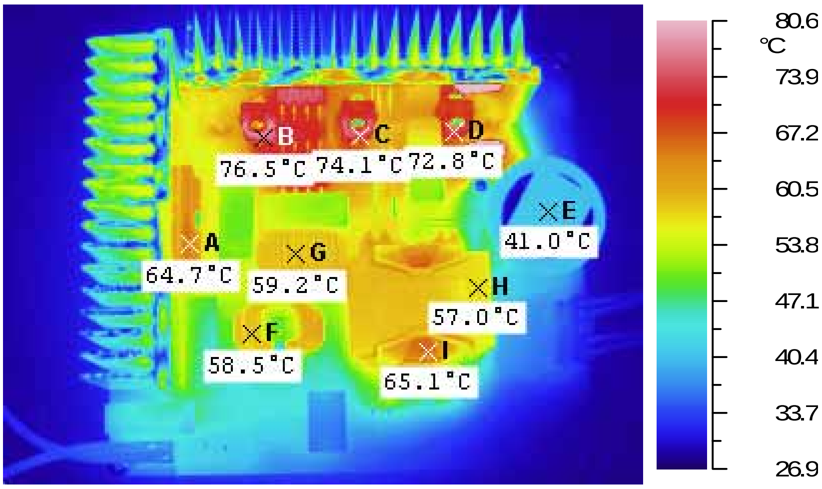


Figure 36. Thermal map at 230 Vac-50 Hz - full load

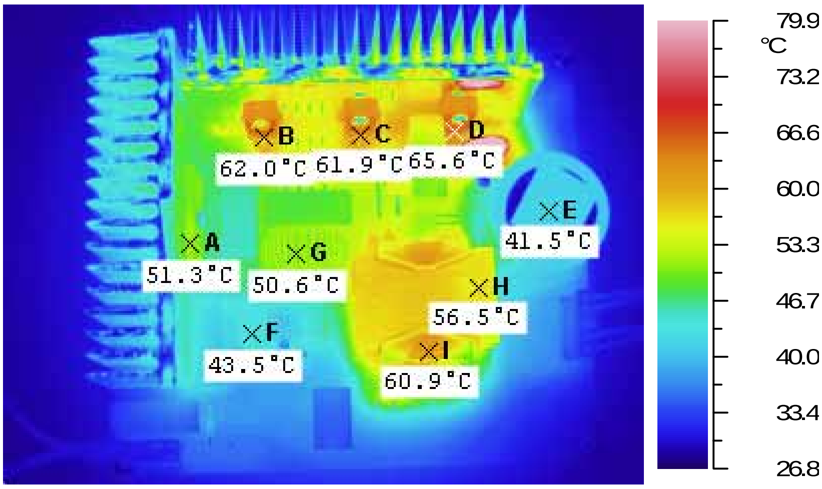


Table 1. Measured temperature table at 115 Vac and 230 Vac - full load

Point	Component	Temperature @115 Vac	Temperature @230 Vac
A	D2	64.7°C	51.3°C
B	Q2	76.5°C	62.0°C
C	Q1	74.1°C	61.9°C
D	D3	72.8°C	65.6°C
E	C7	41.0°C	41.5°C
F	L1	58.5°C	43.5°C
G	L3	59.2°C	50.6°C
H	L4 – CORE	57.0°C	56.5°C
I	L4 - WINDING	65.1°C	60.9°C

6 Conducted emission pre-compliance test

Figure 37, *38*, *39*, and *40* show the peak measurement of the conducted noise at full load and nominal mains voltages. The limits shown on the diagrams are EN55022 Class-B, which is the most common norm for domestic equipment using a two-wire mains connection. As shown on the graphs, under all test conditions there is a good margin of the measures with respect to the limits.

Figure 37. 115 Vac and full load - phase

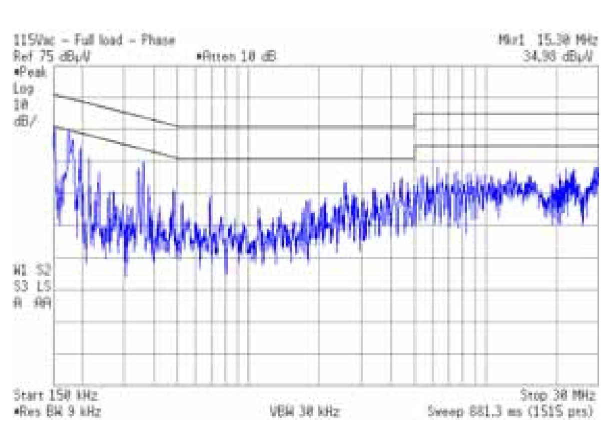


Figure 38. 115 Vac and full load - neutral

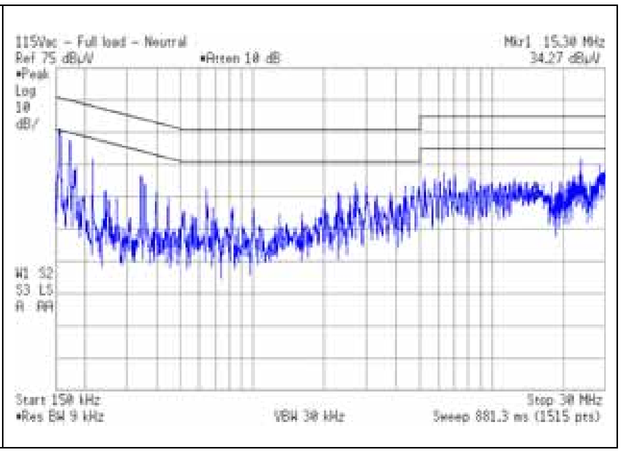


Figure 39. 230 Vac and full load - phase

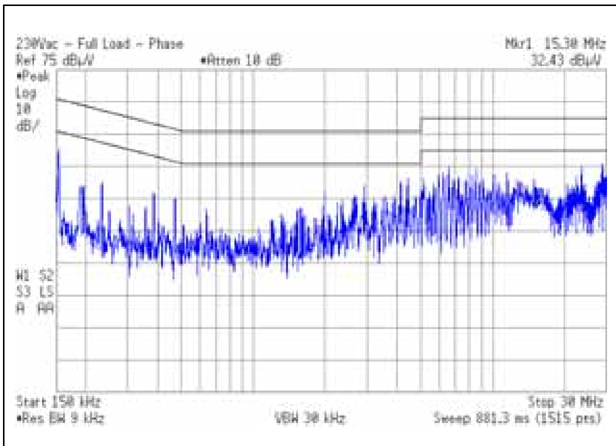
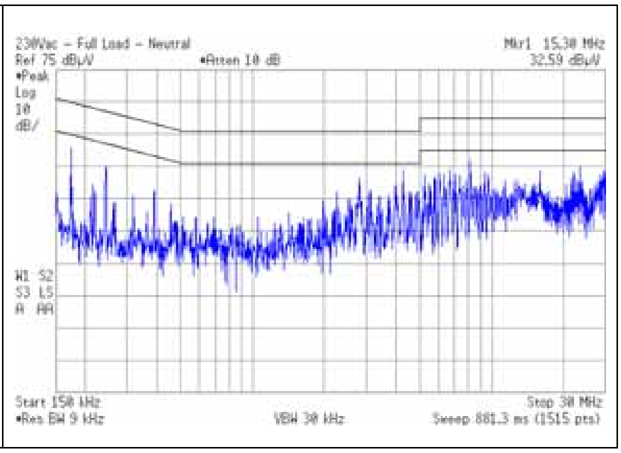


Figure 40. 230 Vac and full load - neutral



7 Bill of material

Table 2. **Bill of material**

Ref. des.	Part type- part value	Case/ package	Description	Supplier
C1	470 nF-X2	DWG	X2 FILM CAPACITOR R46-I 3470--M1-	ARCOTRONICS
C10	18 N	1206	100V SMD CERCAP - GEN. PURPOSE	AVX
C11	470 nF/50 V	1206	50V SMD CERCAP - GEN. PURPOSE	AVX
C12	47 uF/50 V	DIA6.3X11	ALUMINIUM ELCAP - YXF SERIES - 105°C	RUBYCON
C13	100 nF	0805	50V SMD CERCAP - GEN. PURPOSE	AVX
C14	1 µF	1206	50V SMD CERCAP - GEN. PURPOSE	AVX
C15	100 pF	0805	50V SMD CERCAP - GEN. PURPOSE	AVX
C16	220pF	0805	50V SMD CERCAP - GEN. PURPOSE	AVX
C17	10 nF	0805	50V SMD CERCAP - GEN. PURPOSE	AVX
C18	470 nF	1206	50V SMD CERCAP - GEN. PURPOSE	AVX
C19	2 nF2	0805	50V SMD CERCAP - GEN. PURPOSE	AVX
C2	470 nF-X2	DWG	X2 FILM CAPACITOR R46-I 3470--M1-	ARCOTRONICS
C20	330 pF	0805	50V SMD CERCAP - GEN. PURPOSE	AVX
C21	10 nF	1206	50V SMD CERCAP - GEN. PURPOSE	AVX
C3	680nF-X2	DWG	X2 FILM CAPACITOR R46-I 3680--M1-	ARCOTRONICS
C4	470 nF-630 V	DWG	FILM CAPACITOR MKP - B32653A6474J	EPCOS
C5	470 nF-630 V	DWG	FILM CAPACITOR MKP - B32653A6474J	EPCOS
C6	470 nF-630 V	DWG	FILM CAPACITOR MKP- B32653A6474J	EPCOS
C7	330 µF-450 V	DIA35x35	ALUMINIUM ELCAP - LLS SERIES - 85°C	NICHICON
D1	1N5406	DO-201	STD RECOVERY RECTIFIER	VISHAY
D2	D15XB60	DWG	RECTIFIER BRIDGE	SHINDENGEN
D3	STTH8R06	TO-220FP	ULTRAFAST HIGH VOLTAGE RECTIFIER	STMicroelectronics
D4	LL4148	MINIMELF	FAST SWITCHING DIODE	VISHAY
D5	BZX85-C15	MINIMELF	ZENER DIODE	VISHAY
D6	LL4148	MINIMELF	FAST SWITCHING DIODE	VISHAY
D7	LL4148	MINIMELF	FAST SWITCHING DIODE	VISHAY
D8	LL4148	MINIMELF	FAST SWITCHING DIODE	VISHAY
F1	8 A/250 V	5x20MM	8A MAINS INPUT FUSE	WICKMANN
J1			3-PINS CONN. (CENTRAL REM.) P 3.96 KK SERIES	MOLEX
J2			5-PINS CONN. (CENTRAL REM.) P 3.96 KK SERIES	MOLEX

Table 2. Bill of material (continued)

Ref. des.	Part type- part value	Case/ package	Description	Supplier
JP101	JUMPER		WIRE JUMPER	
JP102	JUMPER		WIRE JUMPER	
L1	1.5 mH-5A	DWG	CM CHOKE - LFR2205B	DELTA ELECTRONICS
L3	DM-51 µH-6 A	DWG	FILTER INDUCTOR - LSR2306-1	DELTA ELECTRONICS
L4	PQ40-500 µH	DWG	PFC INDUCTOR - 86H-5410B	DELTA ELECTRONICS
Q1	STP12NM50FP	TO-220FP	N-CHANNEL POWER MOSFET	STMicroelectronics
Q2	STP12NM50FP	TO-220FP	N-CHANNEL POWER MOSFET	STMicroelectronics
Q3	BC857C	SOT-23	SMALL SIGNAL BJT - PNP	VISHAY
R1	1 M5	AXIAL	HV RESISTOR	BC COMPONENTS
R10	680 K	1206	SMD STD FILM RES - 1% - 250ppm/°C	BC COMPONENTS
R11	680 K	1206	SMD STD FILM RES - 1% - 250ppm/°C	BC COMPONENTS
R12	82 K	0805	SMD STD FILM RES - 1% - 250ppm/°C	BC COMPONENTS
R13	15 K	0805	SMD STD FILM RES - 1% - 250ppm/°C	BC COMPONENTS
R14	56 K	0805	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R15	3K3	0805	SMD STD FILM RES - 1% - 100ppm/°C	BC COMPONENTS
R16	15 K	0805	SMD STD FILM RES - 1% - 100ppm/°C	BC COMPONENTS
R17	6R8	0805	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R18	6R8	0805	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R19	1K0	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R2	NTC 2R5-S237	DWG	NTC RESISTOR 2R5 S237	EPCOS
R20	0R39-1 W	AXIAL	AXIAL RES - 5% - 250ppm/°C	BC COMPONENTS
R21	0R39-1 W	AXIAL	AXIAL RES - 5% - 250ppm/°C	BC COMPONENTS
R22	0R39-1 W	AXIAL	AXIAL RES - 5% - 250ppm/°C	BC COMPONENTS
R23	0R39-1 W	AXIAL	AXIAL RES - 5% - 250ppm/°C	BC COMPONENTS
R24	36 K	0805	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R26	150 K	1206	SMD STD FILM RES - 1% - 250ppm/°C	BC COMPONENTS
R27	240 K	0805	SMD STD FILM RES - 1% - 100ppm/°C	BC COMPONENTS
R3	180 K	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R31	1K5	0805	SMD STD FILM RES - 1% - 100ppm/°C	BC COMPONENTS
R32	620 K	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R33	620 K	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R34	10 K	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R35	3R9	0805	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R36	3R9	0805	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS

Table 2. Bill of material (continued)

Ref. des.	Part type- part value	Case/ package	Description	Supplier
R4	180 K	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R5	47R	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R6	2M2	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R7	2M2	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R8	2M2	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R9	680 K	1206	SMD STD FILM RES - 1% - 250ppm/°C	BC COMPONENTS
R101	0R0	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
R102	0R0	1206	SMD STD FILM RES - 5% - 250ppm/°C	BC COMPONENTS
U1	L6563	SO-14	ADVANCED TM PFC CONTROLLER	STMicroelectronics

8 PFC coil specification

8.1 General description and characteristics

- Application type: consumer, home appliance
- Inductor type: open
- Coil former: horizontal type, 6+6 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temp.: 60 °C

8.2 Electrical characteristics

- Converter topology: Boost PFC Preregulator, FOT control
- Core type: PQ40-30 material grade PC44 or equivalent
- Max operating freq: 100 KHz
- Primary inductance: 500 µH ±10% @1 KHz-0.25 V (see *Note: 1*)
- Primary RMS current: 4.75 A

Note: 1 Measured between pins #1-2 and #5-6

Figure 41. Electrical diagram

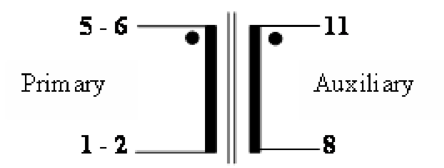


Table 3. Winding charactericstics

Start PINS	End PINS	Number of turns	Wire type	Wire diameter	Notes
11	8	5 (spaced)	Single	Ø 0.28 mm	Bottom
5 - 6	1 - 2	65	Multistrand – G2	Litz Ø 0.2 mm x 30	Top

8.3 Mechanical aspect and pin numbering

- Maximum Height from PCB: 31 mm
- Ferrite: two symmetrical half cores, PQ40-30
- Material grade: PC44 or equivalent
- Central leg air gap: to be defined, in order to get the required inductance value
- Coil former type: vertical, 6+6 pins
- Pin distance: 5 mm
- Row distance: 45.5 mm
- Cut pins: #9-12
- External copper shield: not insulated (for EMI reasons), connected to pin #11 (GND)

Figure 42. Pin side view

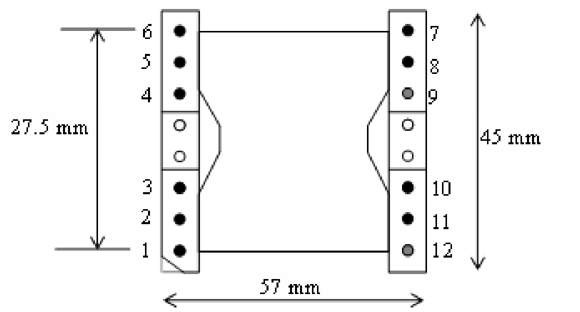
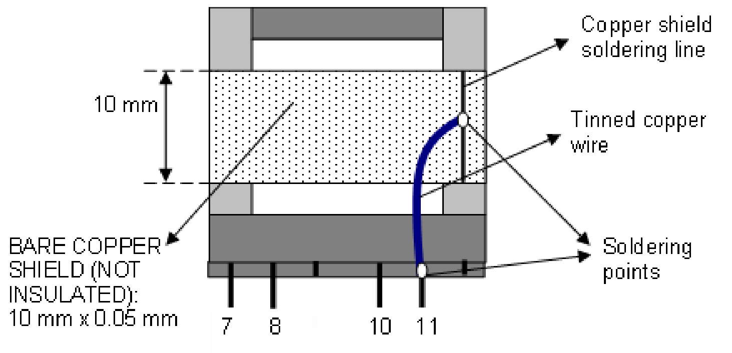


Figure 43. Mechanic aspect



- Manufacturer: DELTA ELECTRONICS
- P/N: 86H-5410B

9 References

1. "L6563 Advanced transition-mode PFC controller" Datasheet
2. "Design of Fixed-Off-Time-Controlled PFC Pre-regulators with the L6562", AN1792
3. "EVAL6562-375W Evaluation Board L6562-based 375W FOT-controlled PFC Pre-regulator" AN1895
4. "L6561, Enhanced Transition-Mode Power Factor Corrector", AN966

10 Revision history

Table 4. Revision history

Date	Revision	Changes
22-Mar-2007	1	First issue