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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR NP60N04MUG

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP60N04MUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP60N04MUG-S18-AY Note	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K) typ. 1.9 g

Note Pb-free (This product does not contain Pb in the external electrode).

FEATURES

• Super low on-state resistance

 $R_{DS(on)} = 6.3 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 30 \text{ A})$

Channel temperature 175 degree rated

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGs = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±60	А
Drain Current (pulse) ^{Note1}	D(pulse)	±240	А
Total Power Dissipation (Tc = 25° C)	PT1	88	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	Pt2	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Repetitive Avalanche Current Note2	lar	30	А
Repetitive Avalanche Energy ^{Note2}	Ear	90	mJ



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Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Tch \leq 150°C, Vdd = 20 V, Rg = 25 $\Omega,$ Vgs = 20 \rightarrow 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.70	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

(TO-220)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	ldss	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	lgss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V _{DS} = V _{GS} , I _D = 250 μA	2.0		4.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 5 V, I _D = 30 A	19	38		S
Drain to Source On-state Resistance Note	RDS(on)	Vgs = 10 V, Id = 30 A		5.0	6.3	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		3200		pF
Output Capacitance	Coss	V _{GS} = 0 V,		320		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		210		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 30 A,		21		ns
Rise Time	tr	V _{GS} = 10 V,		10		ns
Turn-off Delay Time	td(off)	R _G = 0 Ω		48		ns
Fall Time	tr			10		ns
Total Gate Charge	QG	V _{DD} = 32 V,		60		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V,		15		nC
Gate to Drain Charge	QGD	ID = 60 A		21		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 60 A, VGS = 0 V		0.95	1.5	V
Reverse Recovery Time	trr	IF = 60 A, VGS = 0 V,		33		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		40		nC

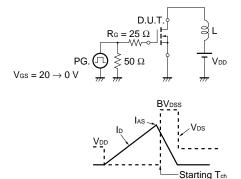
ELECTRICAL CHARACTERISTICS (TA = 25°C)

<R>

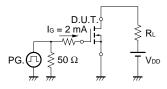
Note Pulsed

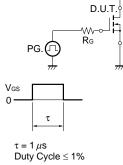
TEST CIRCUIT 1 AVALANCHE CAPABILITY

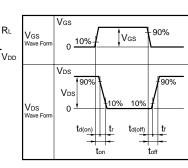
TEST CIRCUIT 2 SWITCHING TIME



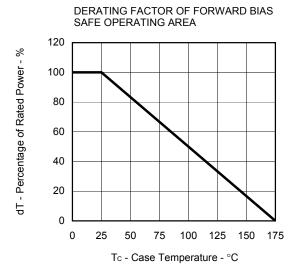
TEST CIRCUIT 3 GATE CHARGE



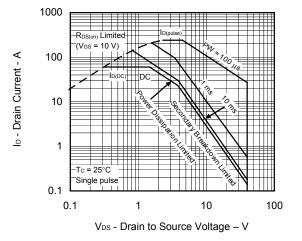


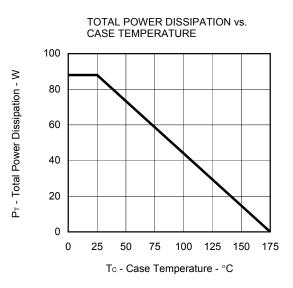


TYPICAL CHARACTERISTICS (TA = 25°C)

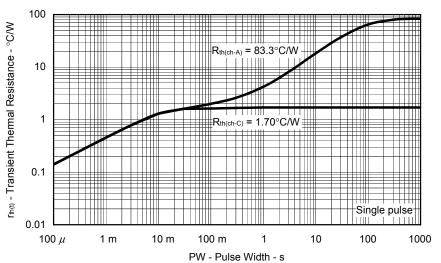




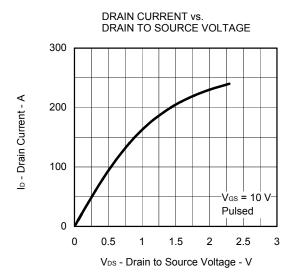




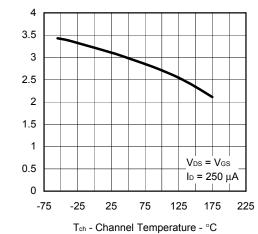
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



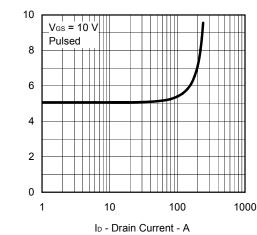
Data Sheet D18663EJ2V0DS





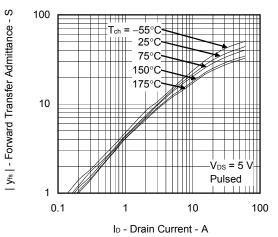


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

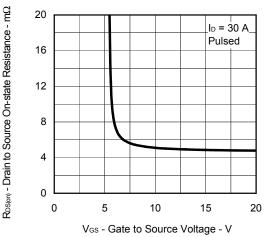


1000 100 ID - Drain Current - A Tch = -55°C 25°C 75°C 150°C 10 175°C 1 Vps = 10 V Pulsed 0.1 0 1 2 3 4 5 6 VGS - Gate to Source Voltage - V

<R> FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



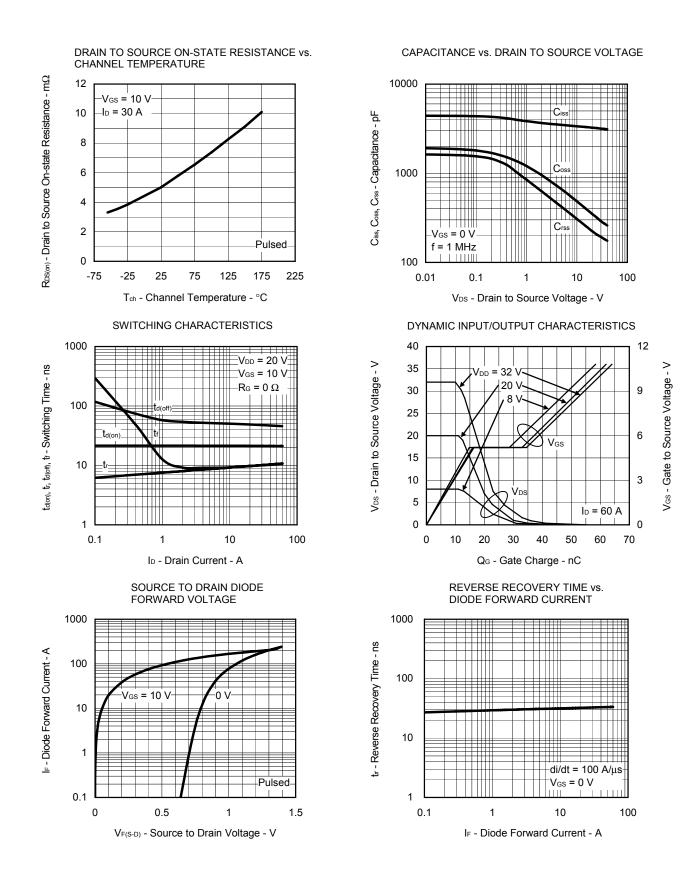
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



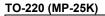
FORWARD TRANSFER CHARACTERISTICS

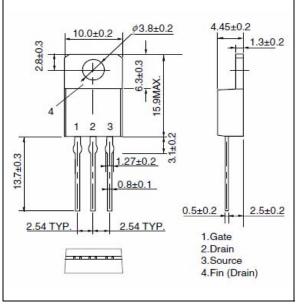
 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

V_{GS(th)} - Gate to Source Threshold Voltage - V

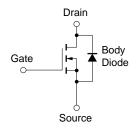


PACKAGE DRAWING (Unit: mm)



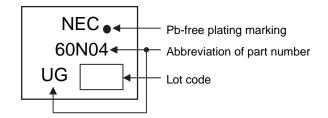


EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP60N04MUG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering	Maximum temperature (Solder temperature): 260°C or below	
MP-25K	Time: 10 seconds or less	THDWS
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	
MP-25K	Time (per side of the device): 3 seconds or less	P350
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Caution Do not use different soldering methods together (except for partial heating).

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