SPXXHC113
SPXXHC173
SPXXHC174
SPXXHC175
SPXXHC374
SPXXHC574

54/74 Series Flip Flops

Ordering Information

Plastic DIP, Industrial Temp Range	Ceramic DIP, Industrial Temp Range	Ceramic DIP, Military Temp Range
SP74HCXXXN	SP74HCXXXJ	SP54HCXXXJ

Features

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- Speed, function and pin-out compatible to 74LS series Logic.
- High Noise Immunity.
- Low quiescent power consumption.
- Wide power supply range.
- Operates over V_{CC} range of 2.0 to 6.0 Volts.
- Symmetric current drive.
- All Inputs are fully buffered.
- All devices have Input Protection diodes to V_{CC} and ground.
- All devices have Logic Input voltage levels consistent with CMOS.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).

Absolute Maximum Ratings

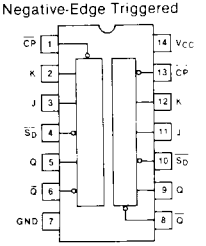
	Parameter	Min	Max	Units
V_{CC}	DC Supply Voltage	−0.5	+7.0	V
V_I, V_O	Input or Output Voltage	−0.5	V_{CC} +0.5	V
I_L	DC Current Per Pin Any Input or Output	—	25	mA
I_{CC}	DC Current Drain, V_{CC} or GND	—	50	mA
T_S	Storage Temperature	−65	+150	°C
P_D	Power Dissipation (Note 1)	—	500	mW
T_L	Lead Temperature (1/16" from mounting surface for 10 sec)	—	+300	°C

Note 1: Derate at 12mW/°C over +45 to +85°C for Plastic "N" Package.

Recommended Operating Conditions

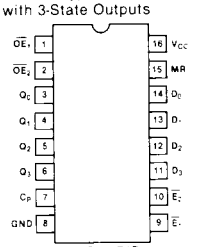
		SP74HCXXX		SP54HCXXX		
	Parameter	Min	Max	Min	Max	Units
V_{CC}	DC Supply Voltage Range	2.0	6.0	2.0	6.0	V
V_I, V_O	Input Voltage, Output Voltage	0	V_{CC}	0	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	−55	+125	°C

SPXXHC113
Dual J K Flip-Flop with Preset, Negative-Edge Triggered



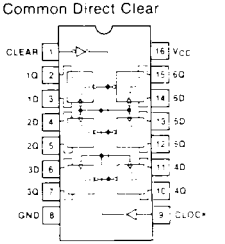
14 PIN DIP
TOP VIEW

SPXXHC173
Quad D-Type Flip-Flop with 3-State Outputs



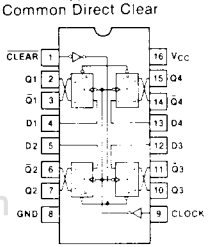
16 PIN DIP
TOP VIEW

SPXXHC174
Hex D-Type Flip-Flops with Common Direct Clear



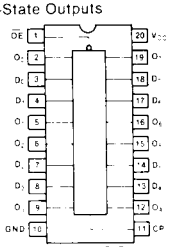
16 PIN DIP
TOP VIEW

SPXXHC175
Quad D-Type Flip-Flops with Common Direct Clear



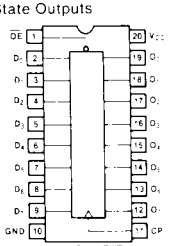
16 PIN DIP
TOP VIEW

SPXXHC374
Octal D-Type Flip-Flop 3-State Outputs



20 PIN DIP
TOP VIEW

SPXXHC574
Octal D-Type Flip-Flop 3-State Outputs



20 PIN DIP
TOP VIEW

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DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	Typ T = 25 °C	Guaranteed Limits SP74HC −40 to +85 °C	Guaranteed Limits SP54HC −55 to +125 °C	Units
V_{IH}	Minimum High Level Input Voltage	V_O = 0.1V or V_{CC} −0.1V $I_O \leq 20\ \mu A$	2.0V		1.5	1.5	V
			4.5V		3.15	3.15	
			6.0V		4.2	4.2	
V_{IL}	Maximum Low Level Input Voltage	V_O = 0.1V or V_{CC} −0.1V $I_O \leq 20\ \mu A$	2.0V		0.3	0.3	V
			4.5V		0.9	0.9	
			6.0V		1.2	1.2	
V_{OH}	Minimum High Level Output Voltage	$I_{OH} = 20\ \mu A$ $V_I = V_{CC}$ or GND	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	
			6.0V	6.0	5.9	5.9	
		I_{OH} = * $V_I = V_{CC}$ or GND	4.5V		3.7	3.7	V
			6.0V		5.2	5.2	
V_{OL}	Maximum Low Level Output Voltage	$I_{OL} = 20\ \mu A$ $V_I = V_{CC}$ or GND	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	
			6.0V	0	0.1	0.1	
		I_{OL} = * $V_I = V_{CC}$ or GND	4.5V	0.1	0.3	0.4	V
			6.0V		0.3	0.4	
I_{IN}	Input Leakage Current	$V_I = V_{CC}$ or GND V_{CC} = 2.0 to 6.0V			±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_I = V_{CC}$ or GND T_A = 25 °C $I_O = 0\ \mu A$ T_A = 85 °C	5.0V	0.1	2.0	2.0	μA
		T_A = 125 °C	5.0V		20.0	20.0	
			5.0V			40.0	
I_{OZH} I_{OZL}	Output Off Current	V_{OUT} = V_{CC} or GND T_A = 25 °C	5.0V	0.1	1.0	1.0	μA
		T_A = 85 °C	5.0V		5.0	5.0	
		T_A = 125 °C	5.0V			10.0	

* 4ma STD outputs 6ma Bus-Drivers

AC Electrical Characteristics (V_{CC} = 5.0V, $t_r = t_f$ = 6ns, T_A = 25 °C, unless otherwise specified)

Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
113	t_{PHL}, t_{PLH}	Clock to Q_A	C_L = 15pF C_L = 50pF	24 26		ns
	t_{PHL}, t_{PLH}	Clock to $\overline{Q}_A$	C_L = 15pF C_L = 50pF	22 24		ns
	t_{PHL}, t_{PLH}	Clock to Q_B	C_L = 15pF C_L = 50pF	22 24		ns
	t_{PHL}, t_{PLH}	Clock to $\overline{Q}_B$	C_L = 15pF C_L = 50pF	22 24		ns
	t_w	Minimum Clock Pulse Width		7		ns
	t_w	Minimum Set Pulse Width		8		
	f_{max}	Maximum Clock Frequency		40		MHz
	C_{in}	Input Capacitance		2		pF
173	t_{PHL}, t_{PLH}	Clock to Q	C_L = 15pF C_L = 50pF	23 25		ns
	t_w	Minimum Clock Pulse Width		10		ns
	f_{max}	Maximum Clock Frequency		50		MHz
	C_{in}	Input Capacitance		2		pF
174	t_{PHL}, t_{PLH}	Clock to Output	C_L = 15pF C_L = 50pF	25 27		ns
	t_{PHL}, t_{PLH}	$\overline{MR}$ to Output	C_L = 15pF C_L = 50pF	25 27		ns
	t_w	Minimum Clock Pulse Width		9		ns
	t_w	Minimum $\overline{MR}$ Pulse Width		8		
	f_{max}	Maximum Clock Frequency		40		MHz
	C_{in}	Input Capacitance		2		pF

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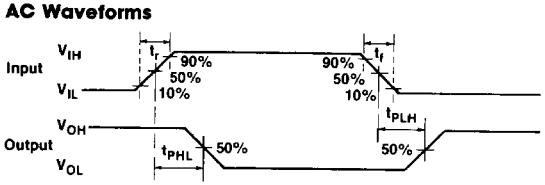
CONTINUED ON NEXT PAGE

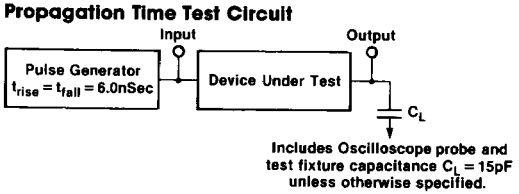
AC Electrical Characteristics (V_{CC} = 5.0V, $t_r = t_f$ = 6ns, T_A = 25°C, unless otherwise specified) CONTINUED

Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
175	t_{PHL}, t_{PLH}	Clock to Q	C_L = 15pF C_L = 50pF	18 21		ns
	t_{PHL}, t_{PLH}	$\overline{MR}$ to Q	C_L = 15pF C_L = 50pF	15 18		ns
	t_{PHL}, t_{PLH}	$\overline{MR}$ to $\overline{Q}$	C_L = 15pF C_L = 50pF	20 22		ns
	t_w	Minimum Clock Pulse Width		8		ns
	t_w	Minimum $\overline{MR}$ Pulse Width		7		
	f_{max}	Maximum Clock Frequency		40		Mhz
	C_{in}	Input Capacitance		2		pF
374	t_{PHL}, t_{PLH}	Clock to Output	C_L = 15pF C_L = 50pF	23 26		ns
	t_{PZL}, t_{PZL}	Enable to High/Low	C_L = 15pF C_L = 50pF	14 17		ns
	t_{PHZ}, t_{PLZ}	Disable from High/Low	C_L = 15pF C_L = 50pF	14 17		ns
	f_{max}	Maximum Clock Frequency		30		MHz
	C_{in}	Input Capacitance		2		pF
574	t_{PHL}, t_{PLH}	Clock to Output	C_L = 15pF C_L = 50pF	17 20		ns
	t_{PHL}, t_{PLH}	Enable to High/Low	C_L = 15pF C_L = 50pF	19 22		ns
	t_{PHL}, t_{PLH}	Disable from High/Low	C_L = 15pF C_L = 50pF	18 21		ns
	f_{max}	Maximum Clock Frequency		30		MHz
	C_{in}	Input Capacitance		2		pF

AC Waveforms

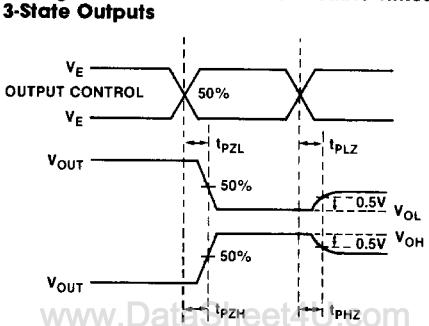


Propagation Time Test Circuit



Includes Oscilloscope probe and test fixture capacitance C_L = 15pF unless otherwise specified.

Voltage Waveforms Enable & Disable Times, 3-State Outputs



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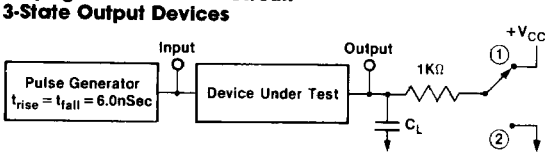
Propagation Time Test Circuit 3-State Output Devices



1 t_{PZL} or t_{PLZ}
2 t_{PZH} or t_{PHZ}

Mode Select and Function Tables

HC113

Operating Mode	Inputs $\overline{S}_D$	$\overline{CP}$	J	K	Outputs Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

HC173

Register Operating Modes	Inputs MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Outputs Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel Load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (No change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

HC173

3-State Buffer Operating Modes	Inputs Q_n (Register)	$\overline{OE}_1$	$\overline{OE}_2$	Outputs Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

HC374

Operating Modes	Inputs $\overline{OE}$	CP	D_n	Internal Register	Outputs Q_0-Q_7
Load & read register	l	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

HC174

Operating Mode	Inputs $\overline{MR}$	CP	D_n	Outputs Q_n
Reset (clear)	L	X	X	L
Load "I"	H	↑	h	H
Load "O"	H	↑	l	L

HC17

Operating Mode	Inputs MR	CP	D_n	Outputs Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "I"	H	↑	h	H	L
Load "O"	H	↑	l	L	H

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition
(Z) = HIGH impedance "off" state.
↑ = LOW to HIGH clock transition.

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