2-W STEREO AUDIO POWER AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS

GENERAL DESCRIPTION

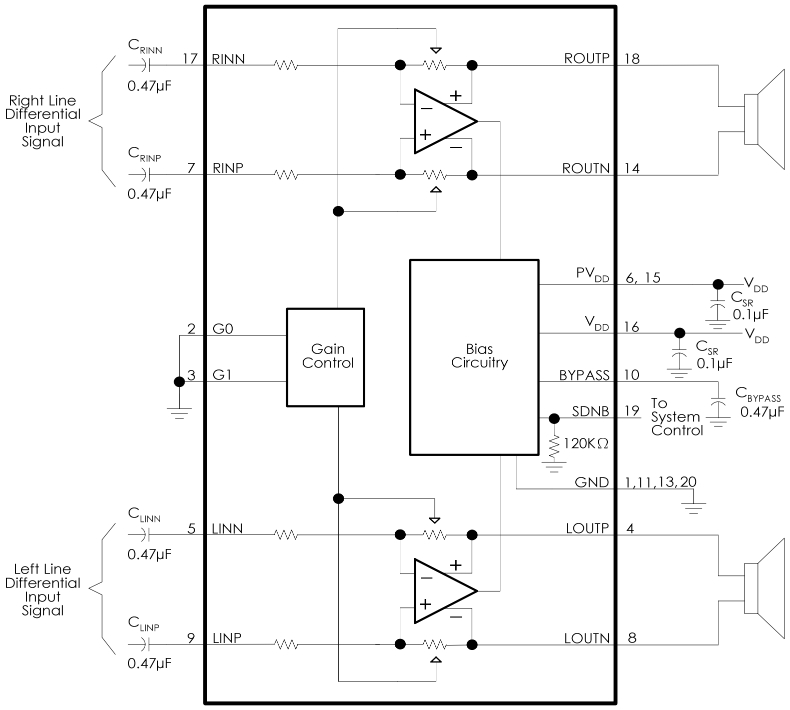
The EMA2217 is a stereo audio power amplifier in a 20-pin TSSOP thermally enhanced package capable of driving 2W of continuous RMS power per channel into 4Ω loads. Internal gain control minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. Amplifier gain is internally configured and controlled by way of two terminals (G0 and G1). Gain settings of 6 dB, 10 dB, 15.6 dB, and 21.6 dB are provided. EMP products are Pb-free and RoHS compliant.

FEATURES

- Internal Gain control Which Eliminates External Gain-Setting Resistors
- Fully Differential Configuration
- Low Supply Current (6mA Typical)
- De-pop Citcuitry

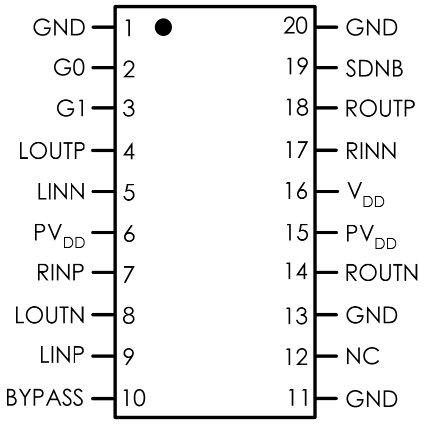
APPLICATIONS

- Notebook Computers, PDAs, and Other Portable Audio devices



CONNECTION DIAGRAM

TSSOP-20



ORDER INFORMATION

EMA2217-50QE16GRR

50	5.0V Operation
QE16	TSSOP-20FD Package
G	Lead-free Package; SnBi (Pb Free)
R	Commercial Grade Temperature Rating: -40 to 85°C
R	Package in Tape & Reel

MARKING & PACKING INFORMATION

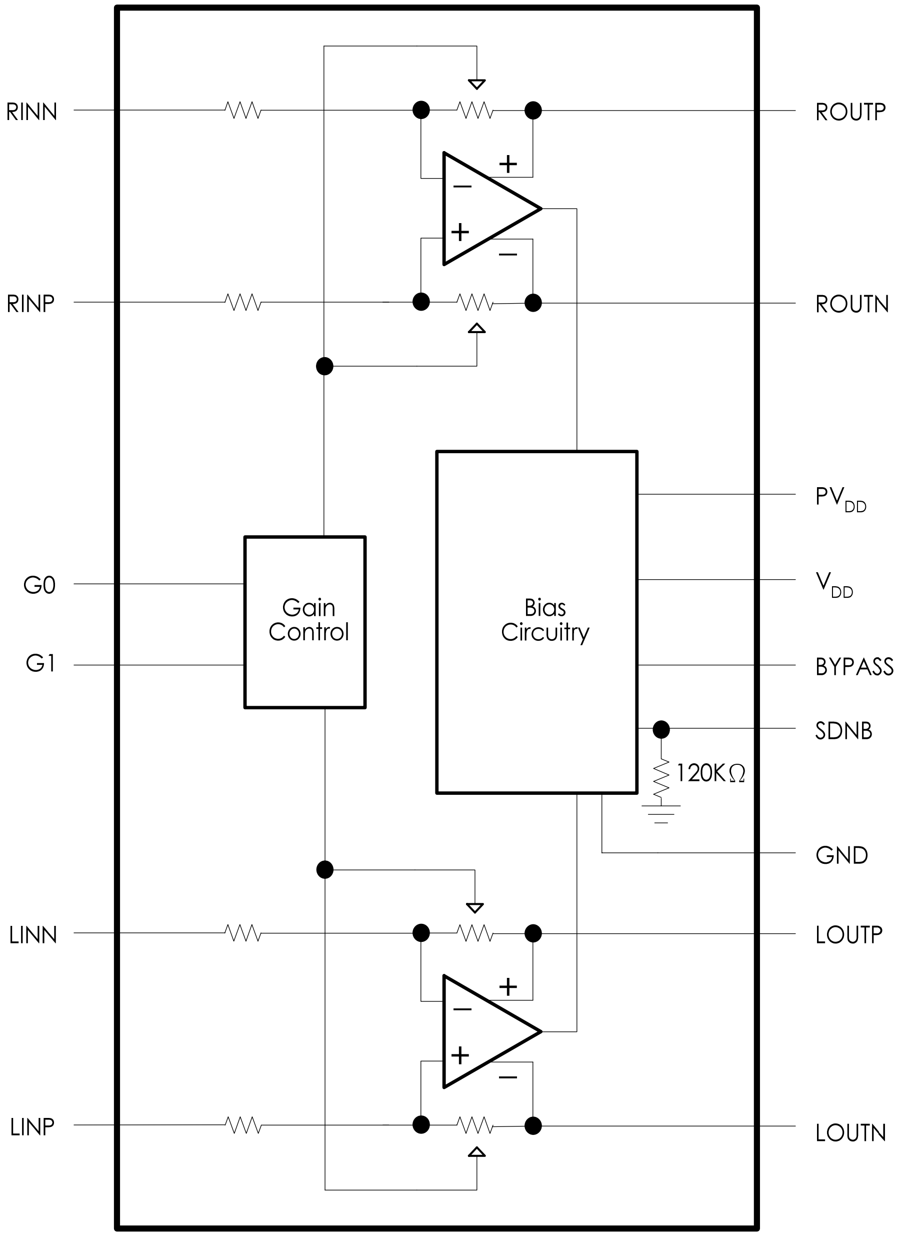
Package Type	Product ID	Package Marking	Transport Media
TSSOP-20	EMA2217-50QE16GRR	EMP EMA2217 DATE CODE	3K units Tape & Reel

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BYPASS	10	-	Tap to voltage divider for internal midsupply bias generator
G0	2	I	Bit 0 of gain select
G1	3	I	Bit 1 of gain select
GND	1,11,13,20	-	Ground
LINN	5	I	Left channel negative differential input
LINP	9	I	Left channel positive differential input
LOUTN	8	O	Left channel negative output
LOUTP	4	O	Left channel positive output
NC	12	-	No connection
PV_{DD}	6,15	I	Supply voltage terminal

ROUTN	14	O	Right channel negative output
ROUTP	18	O	Right channel positive output
RINN	17	I	Right channel negative differential input
RINP	7	I	Right channel positive differential input
SDNB	19	I	Places IC in shutdown mode when held low
V_{DD}	16	I	Supply voltage terminal

FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to VDD +0.3V
Power Dissipation	Internally Limited
ESD Susceptibility	HBM 2kV, MM 200V
Junction Temperature	150°C

Thermal Resistance	
θ_{JA} (TSSOP-20 FD)	55°C/W
Operating Ratings	
Temperature Range	-40°C ≦ T_A ≦ 85°C
Supply Voltage	2.5V ≦ V_{DD} ≦ 5.5V

ELECTRICAL CHARACTERISTICS

Apply for V_{DD} = 5V, A_V=6dB, R_L = 8Ω and T_A = 25°C (unless otherwise noted)

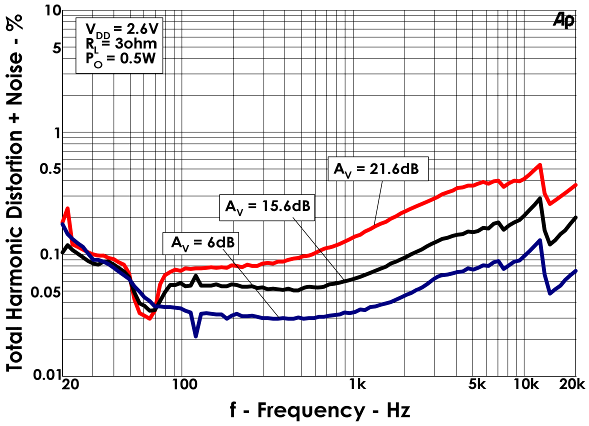
Symbol	Parameter	Conditions	EMA2217			Units
			Min	Typ	Max	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load		6	10	mA
I_{SD}	Shutdown Current	V_{SDNB} = 0.4V		0.1	1.0	μA
I_{IH}	High-level Input Current	SDNB = 1.2V		10		μA
		G0 = G1 = 5V			0.1	
I_{IL}	Low-level Input Current	SDNB = 0.4V		3.3		μA
		G0 = G1 = 0V			0.1	
V_{IH}	High-level Input Voltage	SDNB	1.2			V
		G0/G1		5		
V_{IL}	Low-level Input Voltage	SDNB			0.4	V
		G0/G1		0		
Z_I	Input Impedance		20	25	30	kΩ
V_{OS}	Output Offset Voltage	V_{IN} = 0V, no load, measure differentially		5	25	mV
P_O	Output Power	THD + N = 1 %, f = 1kHz				W
		R_L = 3Ω		2.3		
		R_L = 4Ω		2		
		R_L = 8Ω		1.32		
		THD + N = 10 %, f = 1kHz				
		R_L = 3Ω		2.9		
		R_L = 4Ω		2.45		
		R_L = 8Ω		1.6		
THD+N	Total Harmonic Distortion + Noise	f = 1kHz				%
		R_L = 3Ω, P_O = 1.75W		0.07		
		R_L = 4Ω, P_O = 1.5W		0.06		
		R_L = 8Ω, P_O = 1W		0.015		
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, sine wave, input ac-grounded f = 20 to 20kHz,		-75		dB
CMRR	Common-mode Rejection Ratio	V_I = 1V_{PP}, f = 20 to 20kHz		-62		dB

Apply for V_{DD} = 2.6V, A_V=6dB, R_L = 8Ω and T_A = 25°C (unless otherwise noted)

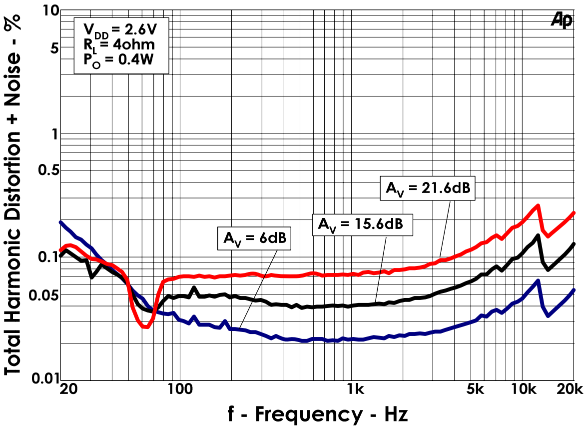
Symbol	Parameter	Conditions	EMA2217			Units
			Min	**Typ**	**Max**	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load		4	10	mA
I_{SD}	Shutdown Current	V_{SDNB} = 0.4V		0.1	1.0	μA
I_{IH}	High-level Input Current	SDNB = 1.2V G0 = G1 = 2.6V		10	0.1	μA
I_{IL}	Low-level Input Current	SDNB = 0.4V G0 = G1 = 0V		3.3	0.1	μA
V_{IH}	High-level Input Voltage	SDNB G0/G1	1.2	2.6		V
V_{IL}	Low-level Input Voltage	SDNB G0/G1		0	0.4	V
Z_I	Input Impedance		20	25	30	kΩ
V_{OS}	Output Offset Voltage	V_{IN} = 0V, no load, measure differentially		5	25	mV
P_O	Output Power	THD + N = 1 %, f = 1kHz R_L = 3Ω R_L = 4Ω R_L = 8Ω		0.55 0.5 0.32		W
		THD + N = 10 %, f = 1kHz R_L = 3Ω R_L = 4Ω R_L = 8Ω		0.68 0.6 0.4		
THD+N	Total Harmonic Distortion + Noise	f = 1kHz R_L = 3Ω, P_O = 0.5W R_L = 4Ω, P_O = 0.4W R_L = 8Ω, P_O = 0.25W		0.03 0.02 0.03		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, sine wave, input ac-grounded f = 20 to 20KHz,		-62		dB
CMRR	Common-mode Rejection Ratio	V_I = 1V_{PP}, f = 20 to 20kHz		-70		dB

TYPICAL PERFORMANCE CHARACTERISTICS

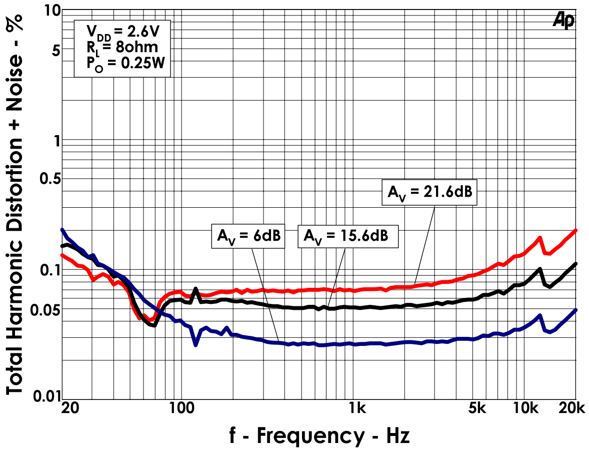
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



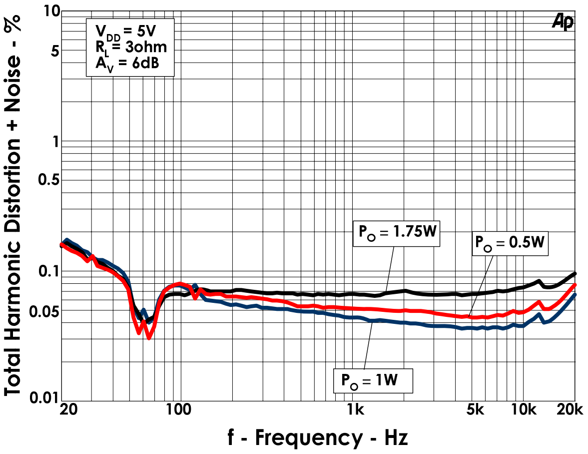
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



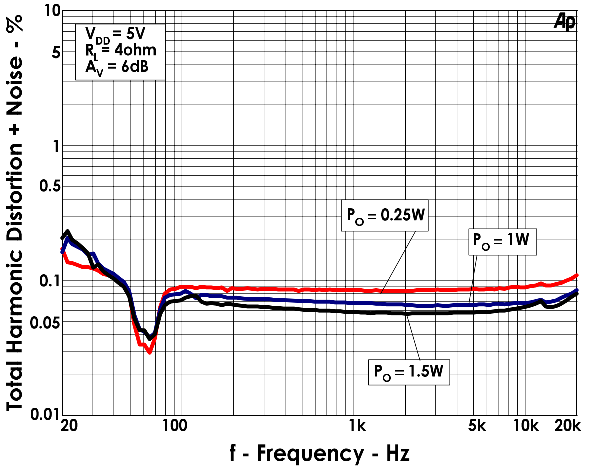
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



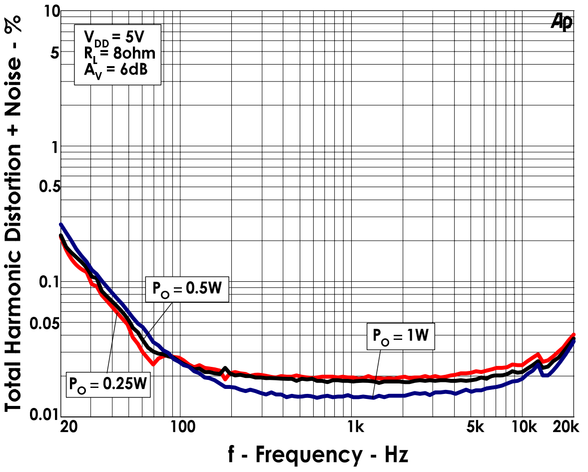
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



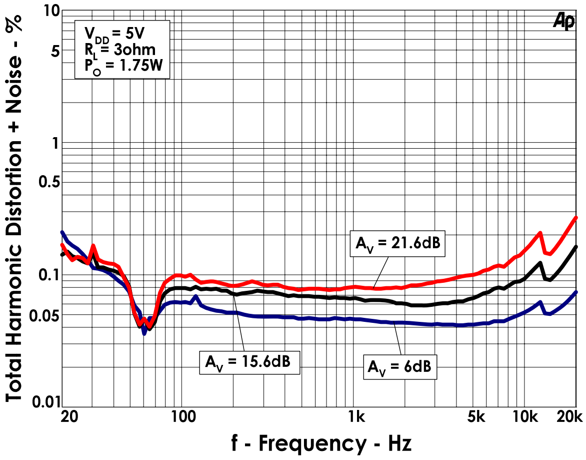
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY



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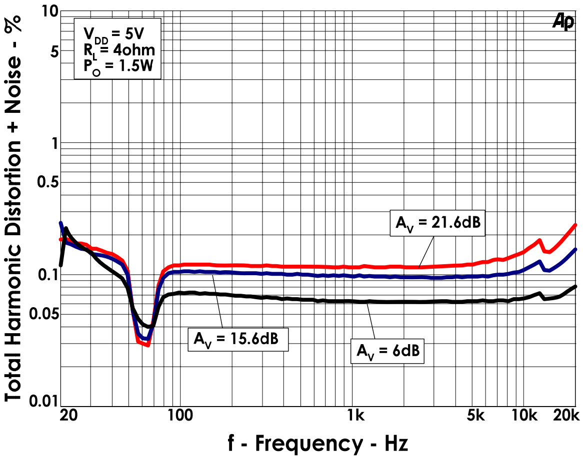
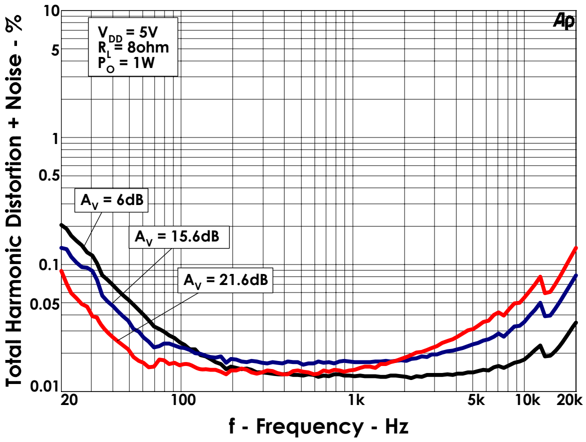
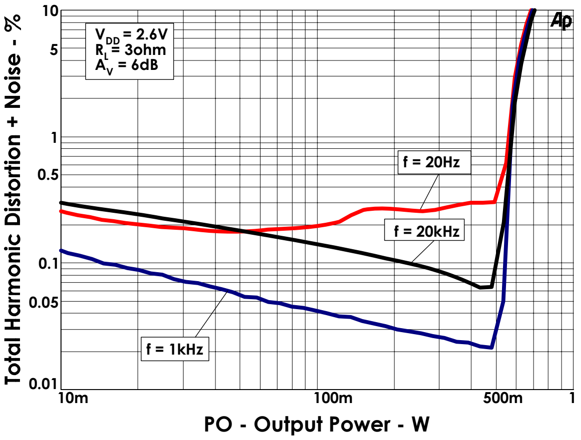
vs
FREQUENCY



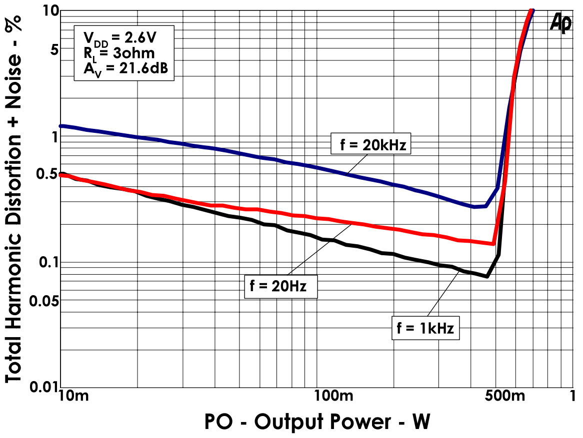
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY



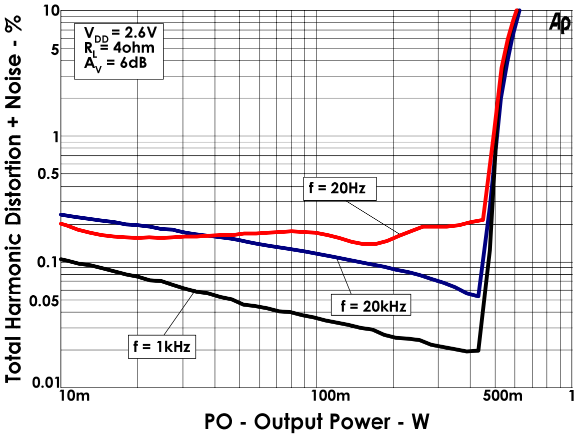
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



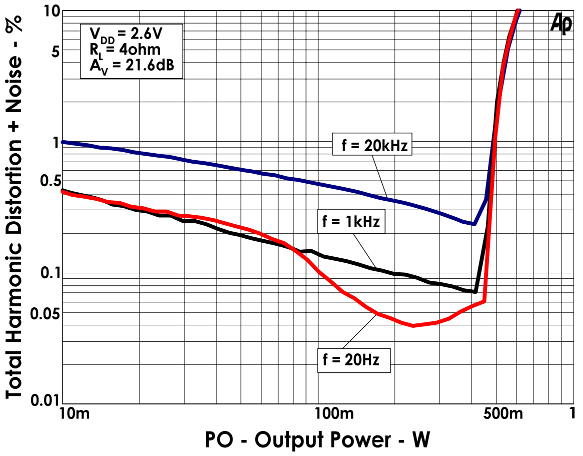
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



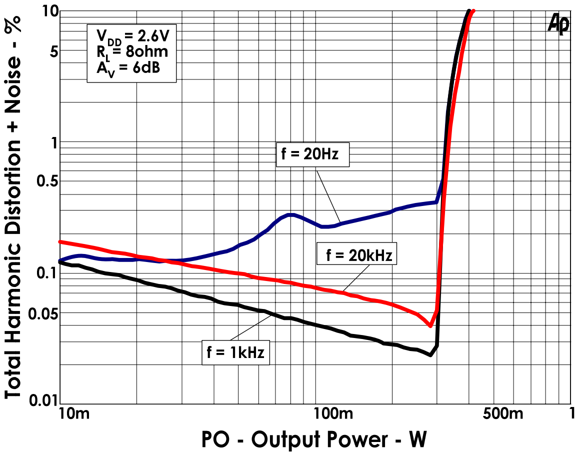
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



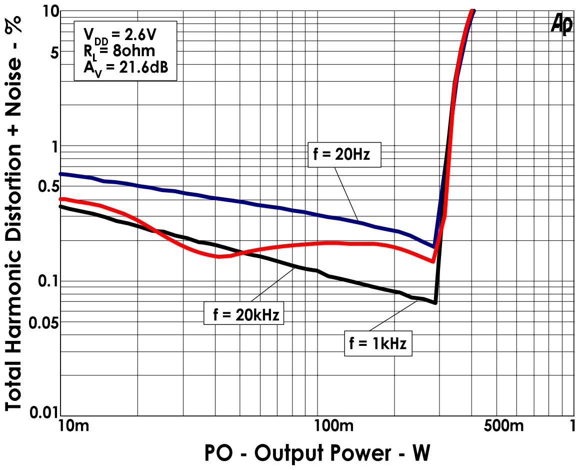
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



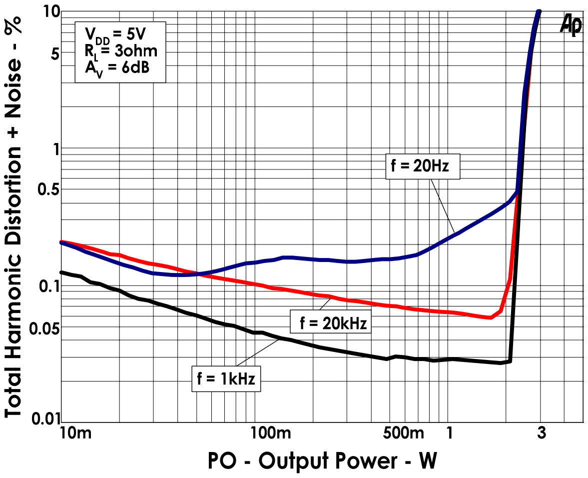
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



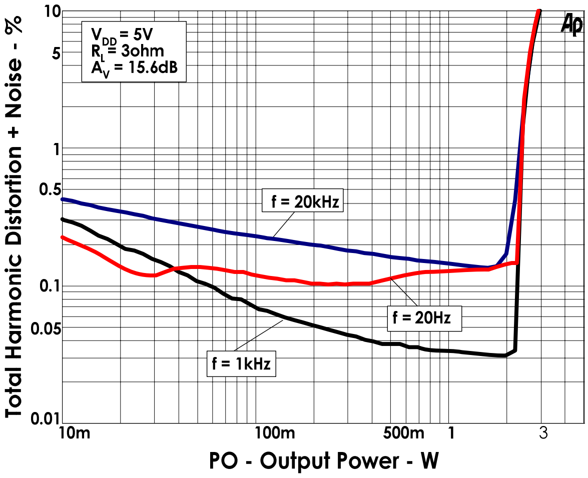
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



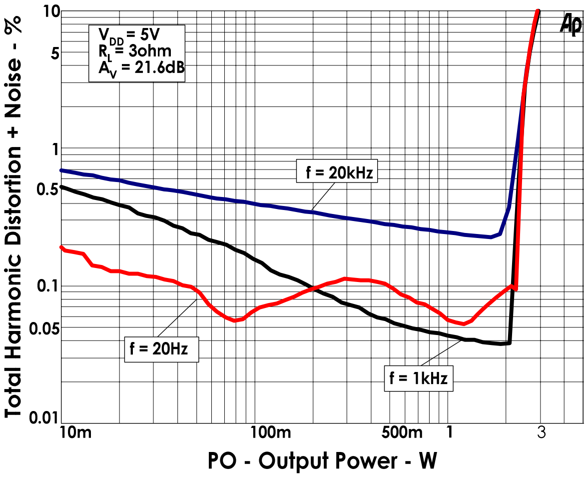
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



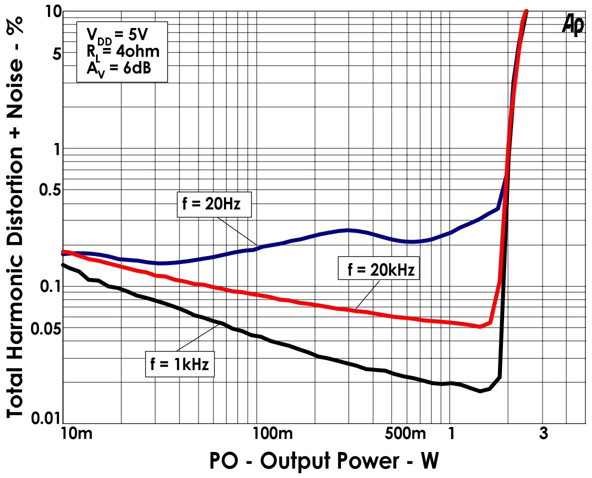
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



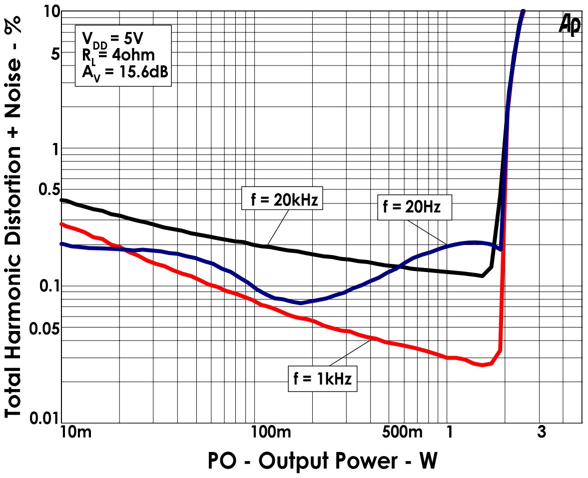
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



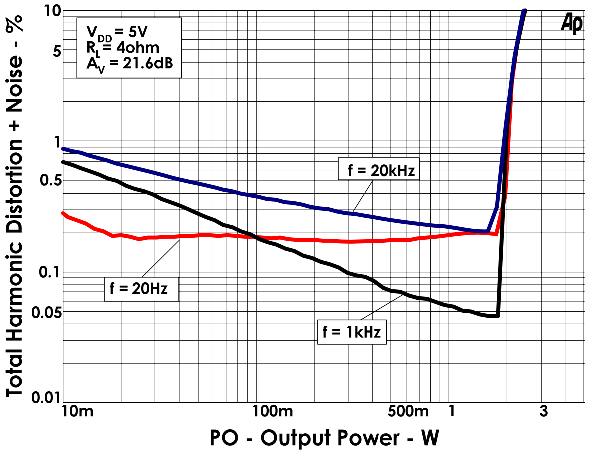
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



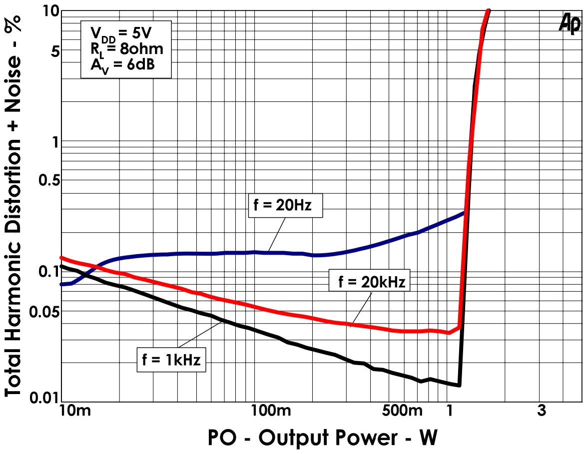
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



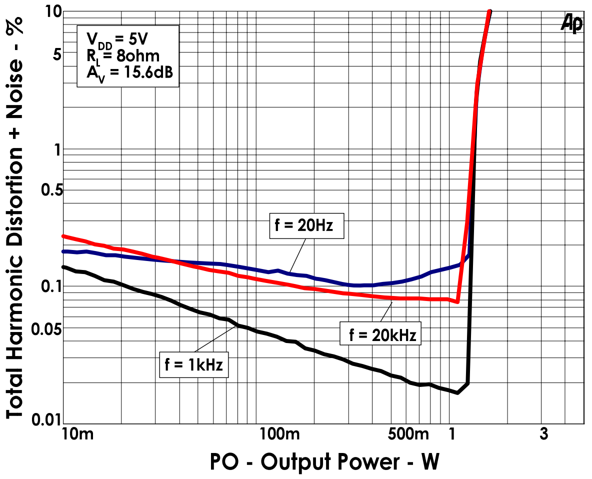
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



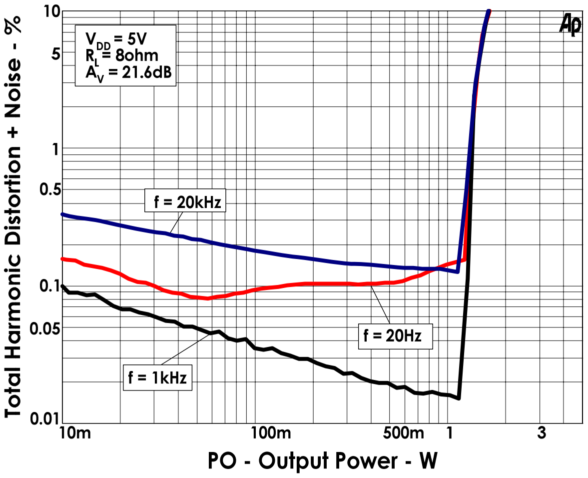
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



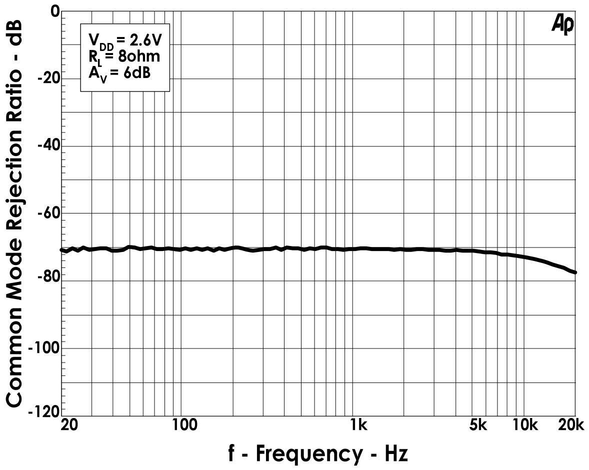
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



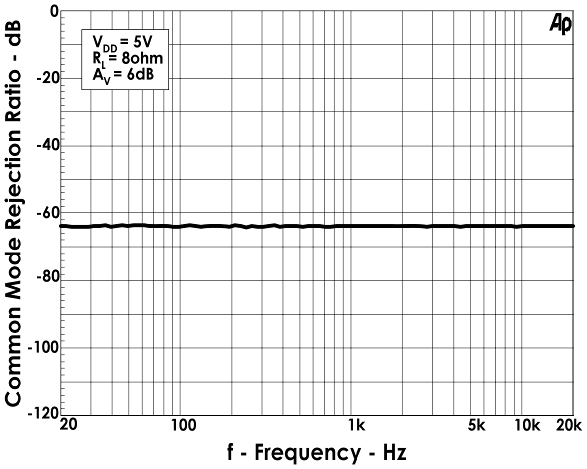
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



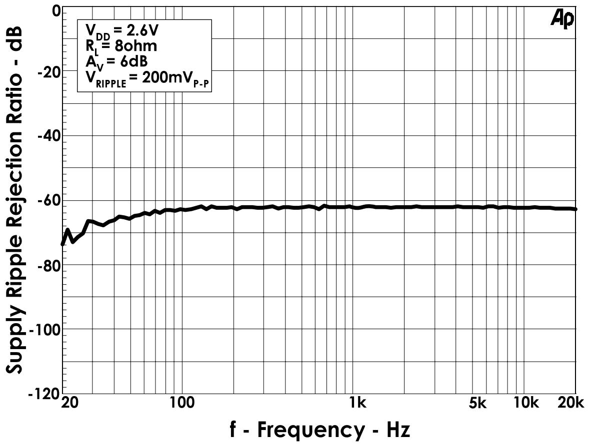
COMMON MODE REJECTION RATIO
vs
FREQUENCY



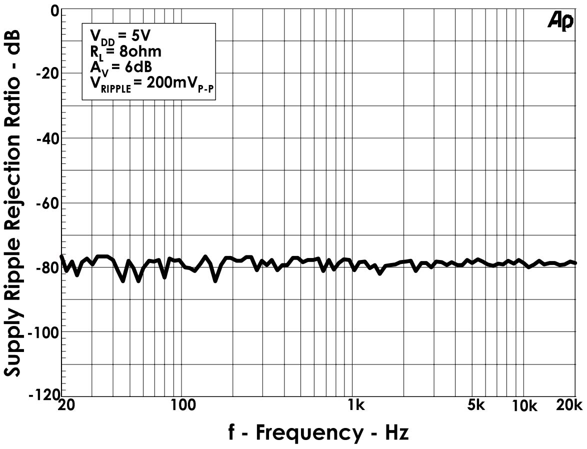
COMMON MODE REJECTION RATIO
vs
FREQUENCY



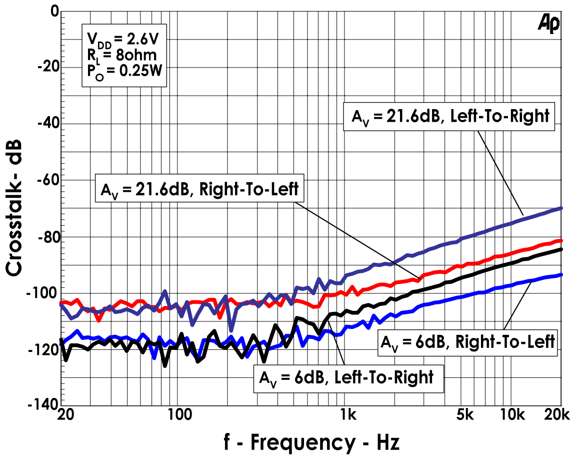
SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY



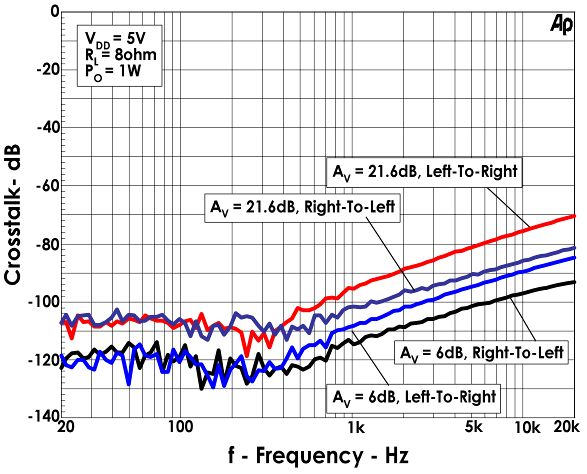
SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

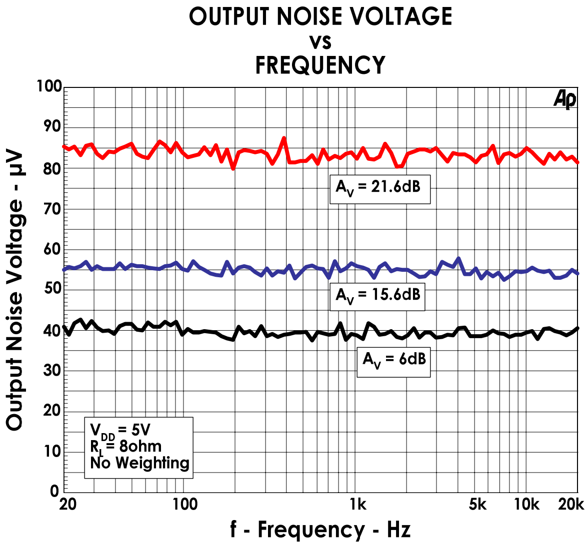


CROSSTALK
vs
FREQUENCY



CROSSTALK
vs
FREQUENCY




OUTPUT NOISE VOLTAGE
vs
FREQUENCY
Output Noise Voltage - µV
100
90
80
70
60
50
40
30
20
10
0
20
100
1k
5k
10k
20k
f - Frequency - Hz
Ap
A$_V$ = 21.6dB
A$_V$ = 15.6dB
A$_V$ = 6dB
V$_{DD}$ = 5V
R$_L$ = 8ohm
No Weighting

APPLICATION INFORMATION

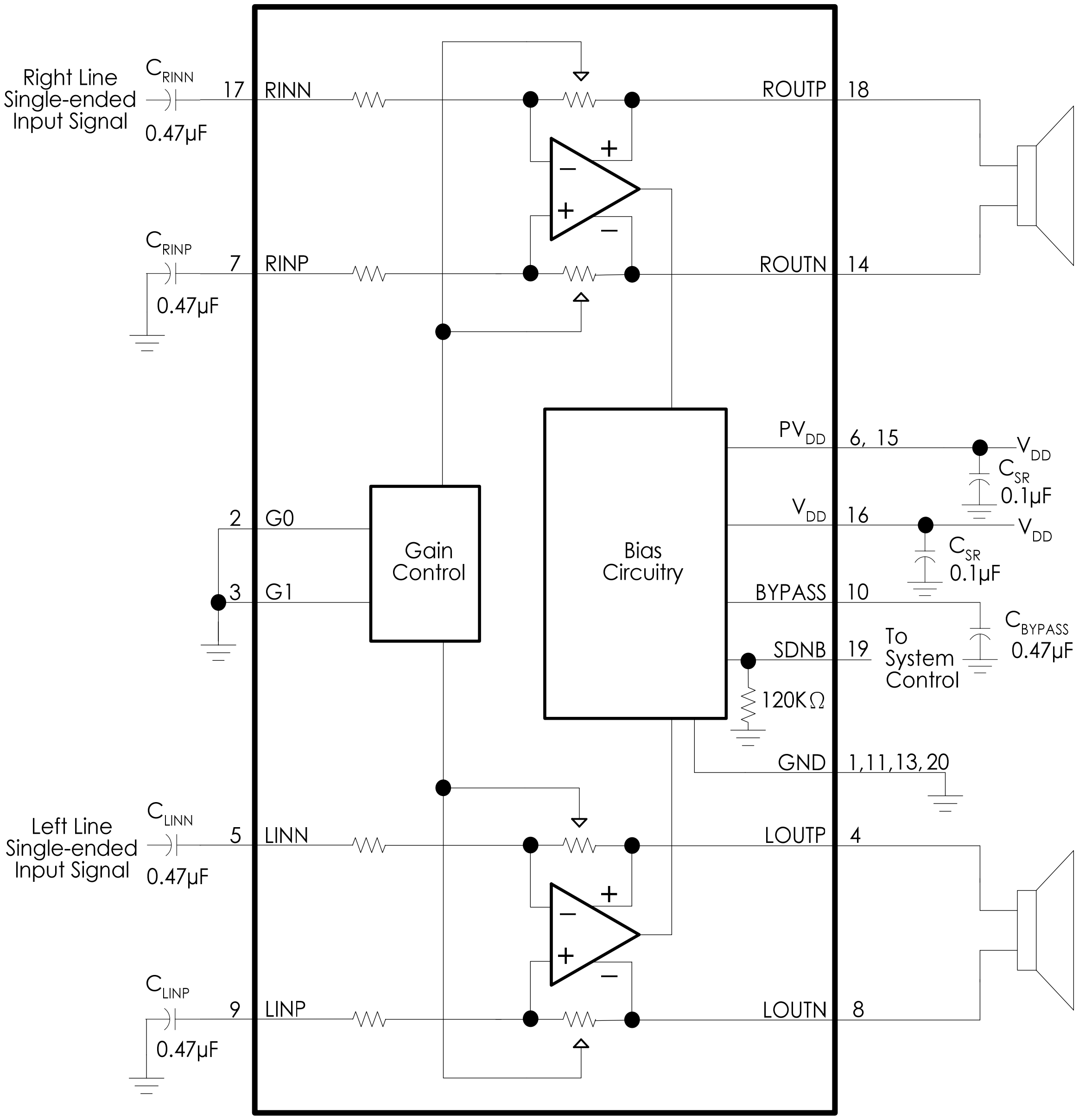


Figure 1. Typical EMA2217 Application Circuit Using Single-Ended Inputs

APPLICATION INFORMATION

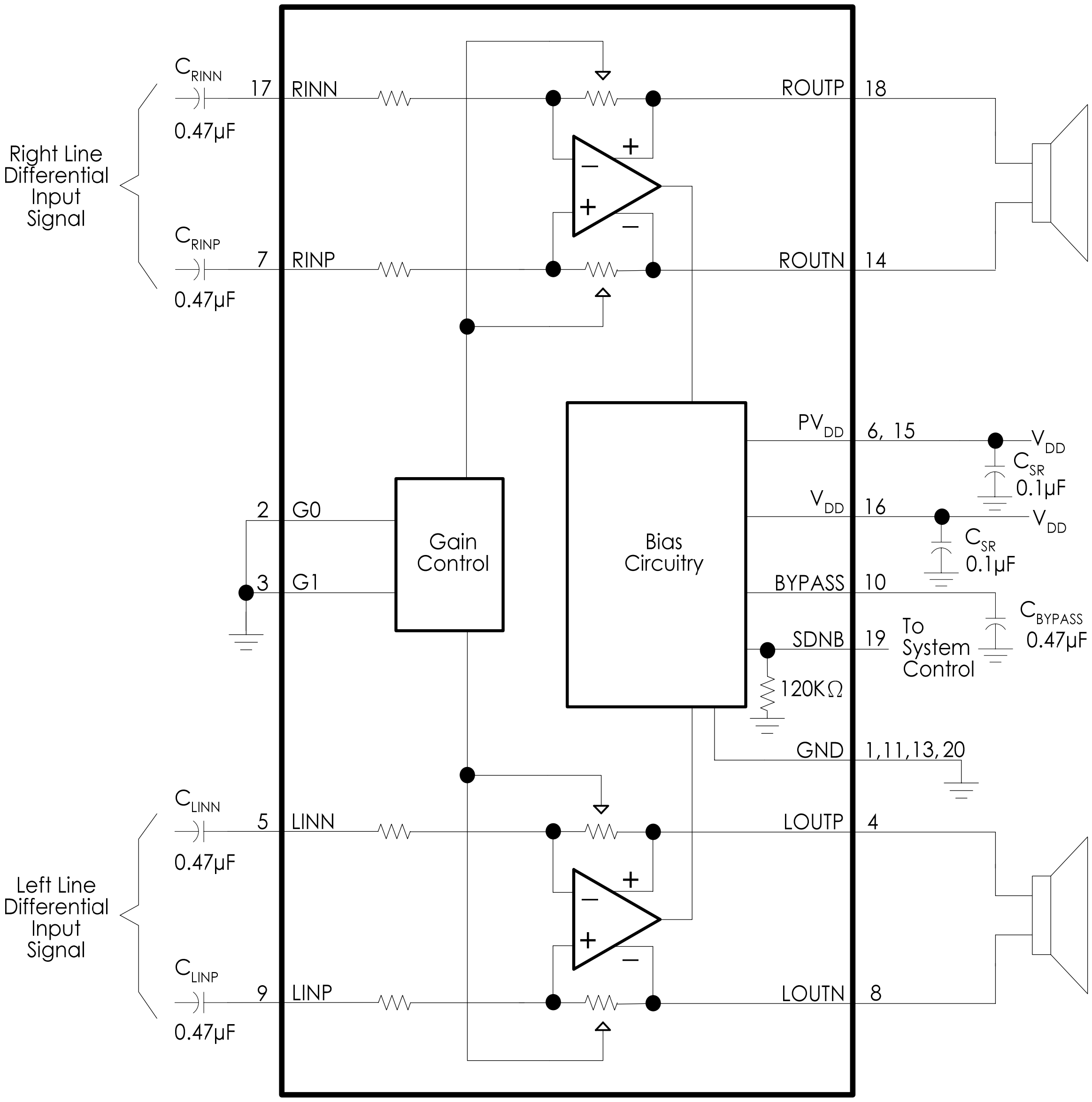


Figure 2. Typical EMA2217 Application Circuit Using Differential Inputs

NOTE A: A 0.1 μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

APPLICATION INFORMATION

shutdown modes

The EMA2217 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SDNB input terminal should be held high during normal operation when the amplifier is in use. Pulling SDNB low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} < 1$ µA. SDNB should never be left unconnected because amplifier operation would be unpredictable.

gain setting via G0 and G1 inputs

The gain of the EMA2217 is set by two input terminals, G0 and G1.

Table 1. Gain Settings

G0	G1	GAIN (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

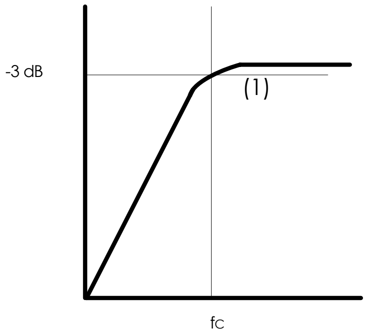
The gains listed in Table 1 are realized by changing the taps on the feedback resistors inside the amplifier. Input impedance, ZI (25 kΩ), is independent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 20% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 20 kΩ, which is the absolute minimum input impedance of the EMA2217.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 1.

$$f_{C(highpass)} = \frac{1}{2\pi Z_I C_I}$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 20 kΩ, which is the absolute minimum input impedance of the EMA2217,and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 2.

$$C_I = \frac{1}{2\pi Z_I f_C} \quad (2)$$

In this example, C_I is 0.2µF, so one would likely choose a value in the range of 0.22µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, CS

The EMA2217 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device VDD lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

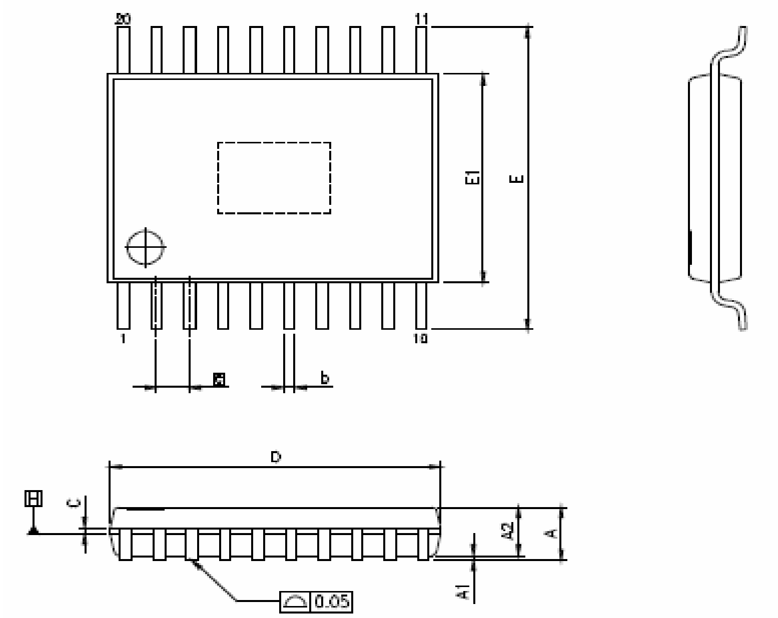
The mid-rail bypass capacitor C_{BYP}, the most critical capacitor serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the mid-rail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

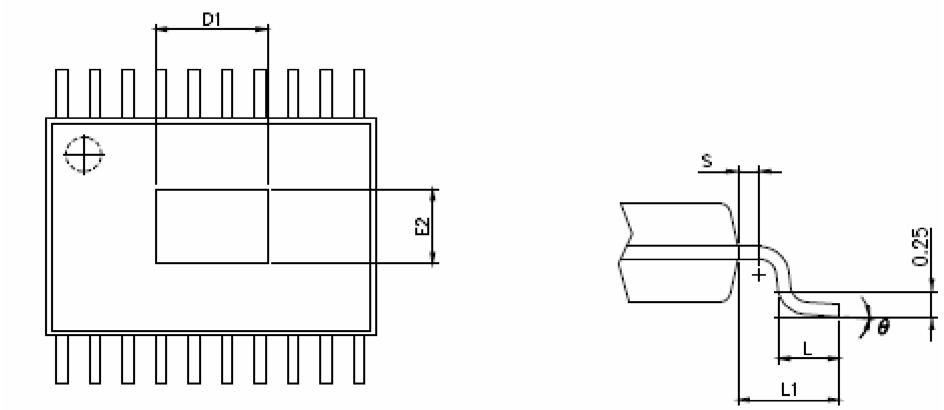
Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

TSSOP-20 Exposed Pad OUTLINE DIMENSION





THERMALLY ENHANCED VARIATIONS ONLY

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

	SYMBOLS	MIN.	NOM.	MAX.
	A	—	—	1.20
△4	A1	0.05	—	0.15
△4	A2	0.80	0.90	1.05
	b	0.19	—	0.30
△4	C	0.09	—	0.20
	D	6.40	6.50	6.60
	E1	4.30	4.40	4.50
	E	6.40 BSC		
	e	0.65 BSC		
	L1	1.00 REF		
△4	L	0.50	0.60	0.75
	S	0.20	—	—
	θ	0°	—	8°

△3 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2	D1
118X16E	2.70 REF	3.77 REF

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