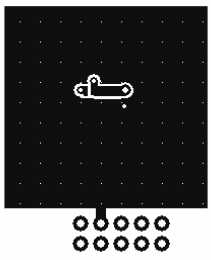
Electrical Characteristics T_J = 25 °C unless otherwise noted

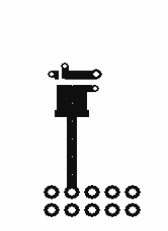
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17.5 A		4.2	5.3	mΩ
		V_{GS} = 4.5 V, I_D = 15.0 A		5.1	6.8	
		V_{GS} = 10 V, I_D = 17.5 A, T_J = 125 °C		5.7	7.2	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 17.5 A		90		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1MHz		1810	2410	pF
C_{oss}	Output Capacitance			620	820	pF
C_{rss}	Reverse Transfer Capacitance			75	110	pF
R_g	Gate Resistance			0.7	2.5	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 17.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	19	ns
t_r	Rise Time			41	0	ns
$t_{d(off)}$	Turn-Off Delay Time				26	41	ns
t_f	Fall Time			31	0	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 17.5 A		28	39	nC
	Total Gate Charge	V_{GS} = 0 V to 4.5 V, V_{DD} = 15 V, I_D = 17.5 A		14	19	nC
Q_{gs}	Gate to Source Charge			4.4		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 17.5 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 17.5 A, di/dt = 100 A/μs	3	0	49	ns
Q_{rr}	Reverse Recovery Charge			13	23	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

3. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurence only. No continuous rating is implied.

4. E_{AS} of 54 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 19 A, V_{DD} = 27 V, V_{GS} = 10 V.

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Typical Characteristics T_J = 25°C unless otherwise noted

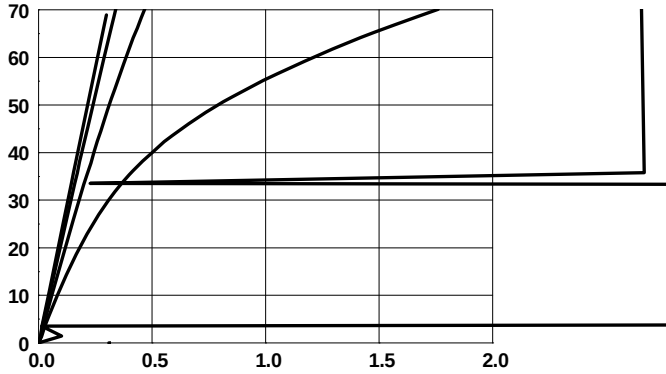


Figure 1.

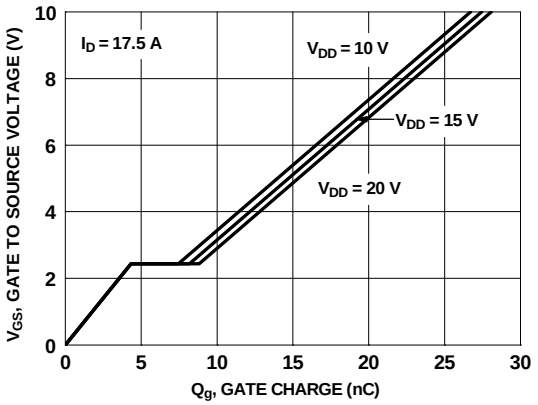


Figure 7. Gate Charge Characteristics

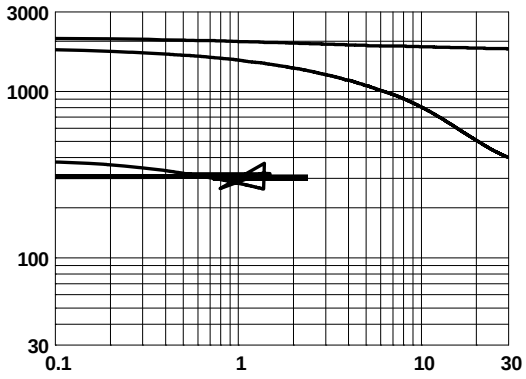


Figure 8.

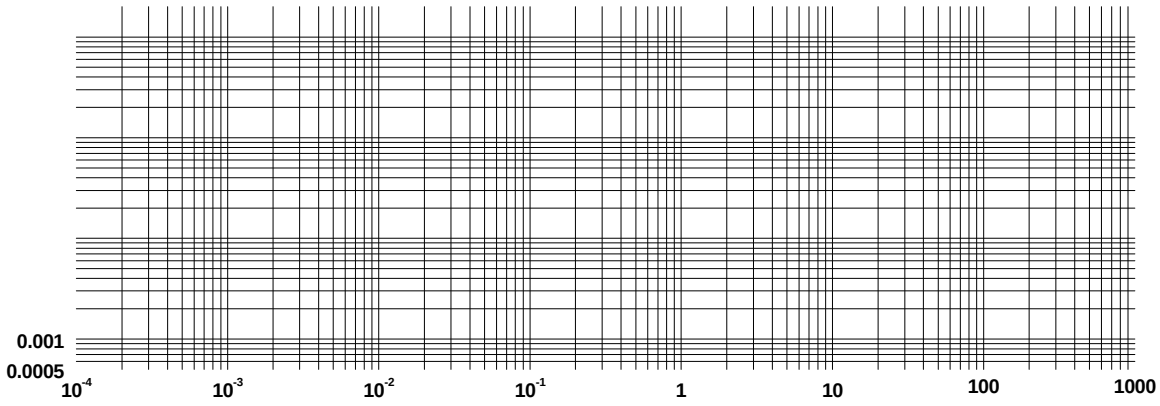
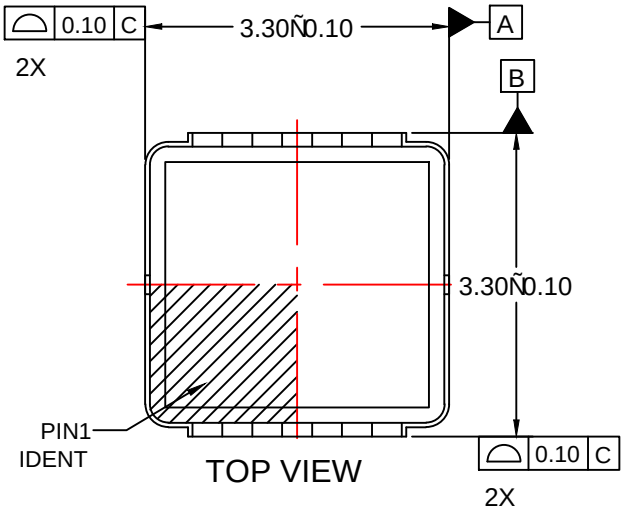
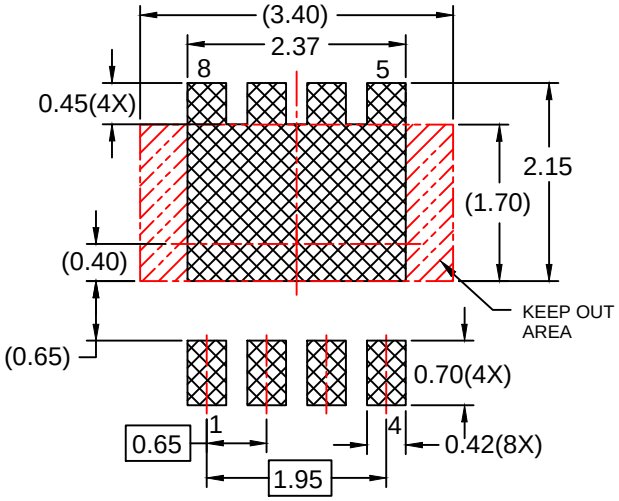
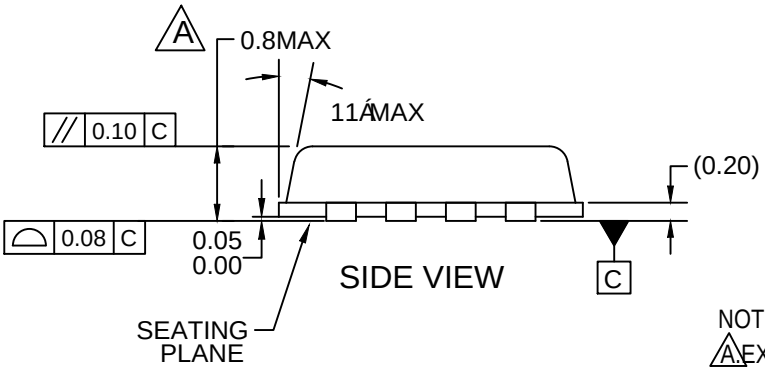


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

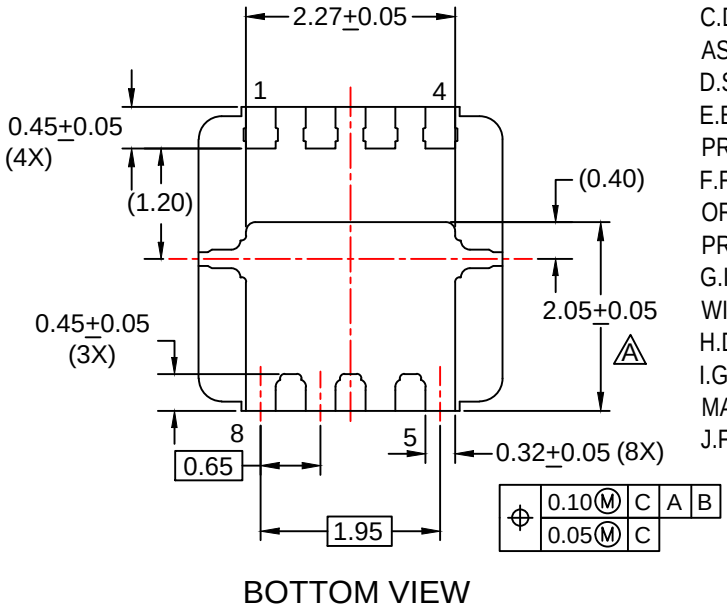
Dimensional Outline and Pad Layout







RECOMMENDED LAND PATTERN



NOTES:

A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA..

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M,1994.

D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY

E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATEBURRS.

F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.

G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.

H. DRAWING FILENAME: MKT-MLP08Trev3.

I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.

J. FAIRCHILD SEMICONDUCTOR.

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