SG588

Low EMI Clock Generator for Digital Camera

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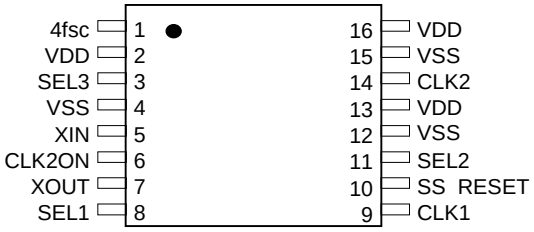
Product Features

The IMISG588 is a clock generator that integrates clock requirements for Digital Camera. It integrates a Spectrum Spread technology, a modulation technique designed specifically for reducing EMI at the fundamental frequency and its harmonics. The IMISG588 generates three output clocks: a buffered reference output (4fsc) of the crystal and 2 other clocks (CLK1,CLK2) generated by the internal Phase Lock Loops. CLK1 clock is modulated output for EMI attenuation. The IMISG588 is packaged in a 16pin TSSOP package for minimum occupation of board space.

- Support clock requirements for Digital Camera
- Application.
- Integrates Spectrum Spread technology for
- EMI attenuation.
- 30 mA buffer switching current
- 16 pin TSSOP package.

Pin Configuration



Pin Description

XIN, XOUT - Forms an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal, 14.318MHz for NTSC. XIN may also serve as input for an externally generated reference signal.

4fsc – Buffered reference output clock of the crystal.

CLK1 and CLK2 – CLK1 and CLK2, are derived from the reference crystal oscillator by using Phase-Locked Loop (PLL). CLK1 integrates a proprietary frequency modulation technique called Spread Spectrum Clock Generation (SSCG) to reduce the Electro Magnetic Interference (EMI) found in high speed digital systems. The amount of modulation (Spread %) of CLK1 is +/-0.5% or +/-0.1% Center-Spread. Modulation frequency of spread is 31.3995KHz. See table 1 for frequencies and function.

SEL1 and SEL2 – These pins are used to select the clock frequencies, spread on/off and spread bandwidth to be modulated +/-0.5% or +/-0.1%. See table 1. These pins have internal pull-up resistors.

CLK2ON – This pin is used to enable/disable CLK2 output. When Low, CLK2 to be disabled, low state. When High (default), CLK2 to be enabled. This pin has an internal pull-up resistor.

SS_RESET– This pin is used to reset location of SSCG profile. When signal goes high to low, the location of SSCG profile is reset to the reference frequency. This pin has an internal pull-up resistor.

VDD – Circuit positive power supply.

VSS – Circuit ground.

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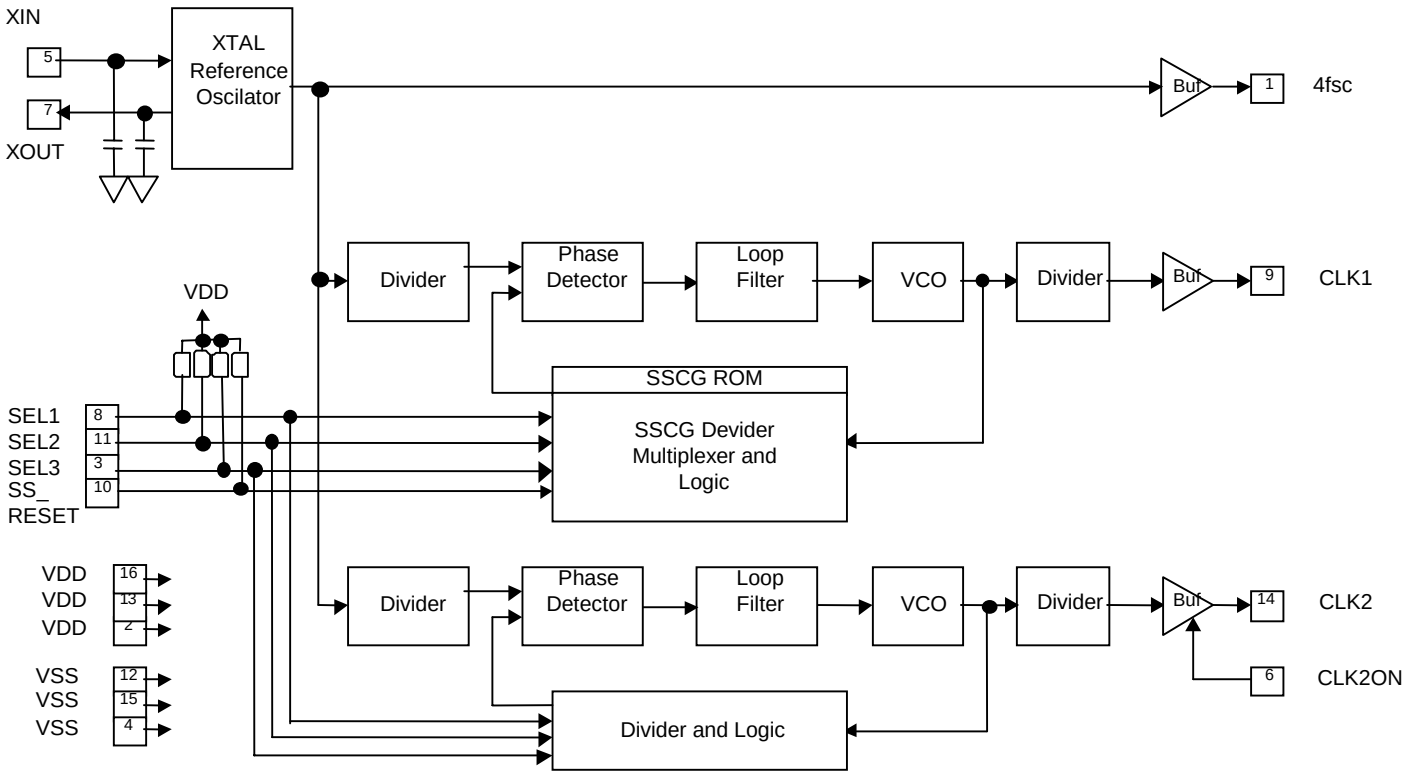
Block Diagram



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Frequency Selection and SSCG Mode Table

Frequencies [MHz]

SEL1	SEL2	SEL3	CLK2ON	4fsc	CLK1	CLK2
H	H	H	H	X'tal buffer	71.877264+/-0.1%	48.008015
H	H	L	H	X'tal buffer	71.877264	48.008015
H	L	H	H	X'tal buffer	71.877264+/-0.5%	48.008015
H	L	L	H	X'tal buffer	96.016031+/-0.1%	48.008015
L	H	H	H	X'tal buffer	114.545440+/-0.1%	96.016031
L	H	L	H	X'tal buffer	114.545440	96.016031
L	L	H	H	X'tal buffer	114.545440+/-0.5%	96.016031
L	L	L	H	X'tal buffer	96.016031	48.008015
H	H	H	L	X'tal buffer	71.877264+/-0.1%	DISABLE(LOW)
H	H	L	L	X'tal buffer	71.877264	DISABLE(LOW)
H	L	H	L	X'tal buffer	71.877264+/-0.5%	DISABLE(LOW)
H	L	L	L	X'tal buffer	96.016031+/-0.1%	DISABLE(LOW)
L	H	H	L	X'tal buffer	114.545440+/-0.1%	DISABLE(LOW)
L	H	L	L	X'tal buffer	114.545440	DISABLE(LOW)
L	L	H	L	X'tal buffer	114.545440+/-0.5%	DISABLE(LOW)
L	L	L	L	X'tal buffer	96.016031	DISABLE(LOW)

Table-1

Frequency ratio

XIN=14.318180MHz

(1) 71.877264MHz: XIN * 251/25/2
(2) 96.016031MHz: XIN * 228/17/2
(3) 114.545440MHz: XIN * 112/7/2
(4) 48.008015MHz: XIN * 57*2/17/2
(5) 96.016031MHz: XIN * 57*2/17

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock around the center of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, modulating the clock is center spread from its resting frequency.

Center Spread

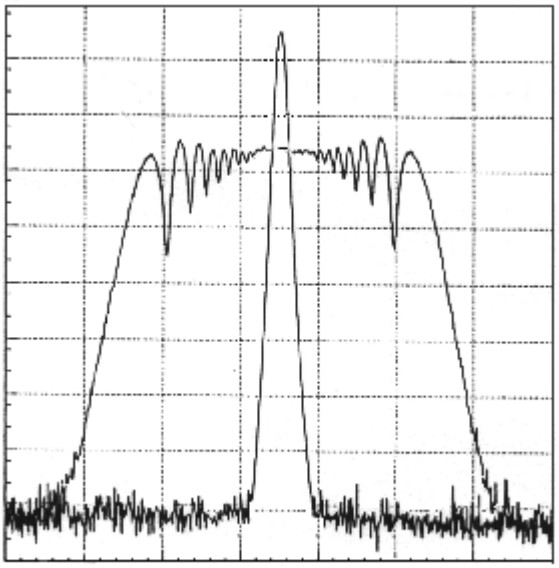

Figure-1

Low EMI Clock Generator for Digital Camera

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-30ºC to + 125ºC
Operating Temperature:	0ºC to + 70ºC
Maximum Power Supply:	5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	V	
Input High Voltage	VIH	2.0	-	-	V	
Input Low Current	IIL	-	-	100	µA	
Input High Current	IIH	-	-	100	µA	
Output Low Voltage	VOL	-	-	0.4	V	IOL=4mA
Output High Voltage	VOH	2.4	-	-	V	IOH=-4mA
Xtal Input / Output Capacitors	CL1,2	-	22	-	PF	X'tal's CL=11.5pf
Supply Current	IDD	-	54	65	mA	
Short Circuit Current	ISC	-	-	30	mA	
Supply Voltage Range	VDDR	3.0	3.3	3.6	V	
VDD = 3.3V, T_A = 0 to 70°C and C_L = 15pF						

Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise Time	tr	-	1.2	1.6	ns	0.2*VDD to 0.8*VDD
Output Fall Time	tf	-	1.1	1.6	ns	0.2*VDD to 0.8*VDD
Output Duty Cycle	Tduty	45	50	55	%	Vth=1.5V
Absolute Jitter (CLK_1)	Tj1	-	145	190	ps	Vth=1.5V
Absolute Jitter (CLK_2)	Tj2	-	95	125	ps	Vth – 1.5V
Power-up Frequency Stabilization	tpw-on		-	50	ms	From 0.9*VDD to frequency lock
Conditions: VDD = 3.3V +/-10%, T_A = 0 to 70°C and C_L = 15pF						

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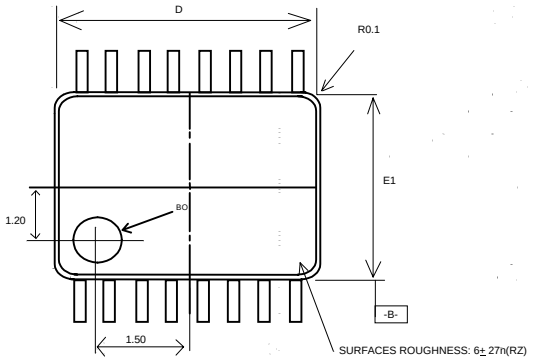
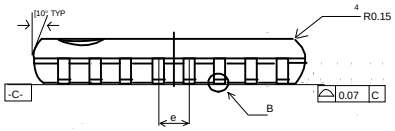
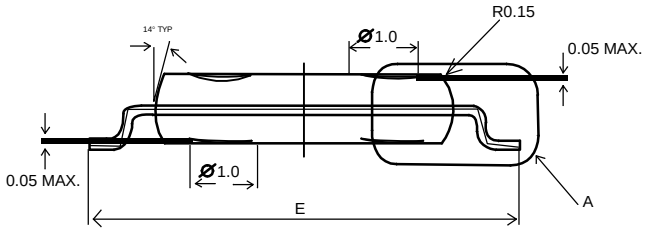
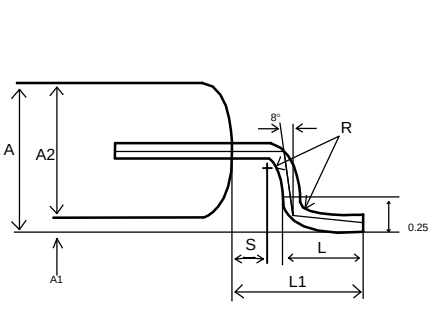
Package Drawing and Dimensions

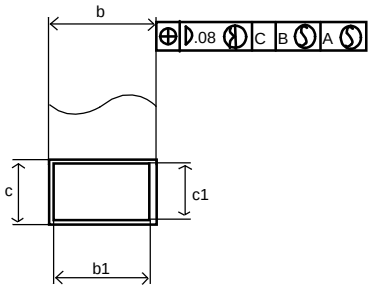








DETAIL A



DETAIL B

16 Pin TSSOP Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.0059	0.05	-	0.15
A2	0.032	0.039	0.041	0.8	1.0	1.05
L	0.018	0.024	0.030	0.45	0.60	0.75
b	0.007	-	0.012	0.19	-	0.30
θ	0°	-	8°	0°	-	8°
e	0.026 BSC			0.65 BSC		
D	0.193	0.197	0.201	4.90	5.0	5.10
E	0.248	0.252	0.256	6.3	6.4	6.5
E1	0.169	0.173	0.177	4.30	4.40	4.50

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Ordering information

Part Number	Package Type	Production Flow
IMISG588BTB	16 PIN TSSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI, Date Code
SG588BTB
Lot#

IMISG588BTB

- Flow
  B = Commercial, 0ºC to +70ºC
- Package
  T = TSSOP
- Revision
- IMI Device Number

NOTES: