

DATA SHEET

TDA7056AT

**3 W mono BTL audio amplifier with
DC volume control**

Product specification

1998 Feb 23



3 W mono BTL audio amplifier with DC volume control

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FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056AT is a mono Bridge-Tied Load (BTL) output amplifier with DC volume control. It is designed for use in TVs and monitors, but is also suitable for battery-fed portable recorders and radios. The device is contained in a 20-lead small outline package.

A Missing Current Limiter (MCL) is built in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (300 mA typ.). This level of 100 mA allows for Single-Ended (SE) headphone applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_o	output power	$V_P = 12\text{ V}; R_L = 16\ \Omega$	3	3.5	–	W
$G_{V(\max)}$	maximum total voltage gain	$V_P = 12\text{ V}; R_L = 16\ \Omega$	34.5	35.5	36.5	dB
ΔG_V	voltage gain control range		75	80	–	dB
$I_{q(\text{tot})}$	total quiescent current	$V_P = 12\text{ V}; R_L = \infty$	–	8	16	mA
THD	total harmonic distortion	$P_o = 0.5\text{ W}$	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7056AT	SO20	plastic small outline package with 20 leads; body width 7.5 mm	SOT163-1

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BLOCK DIAGRAM

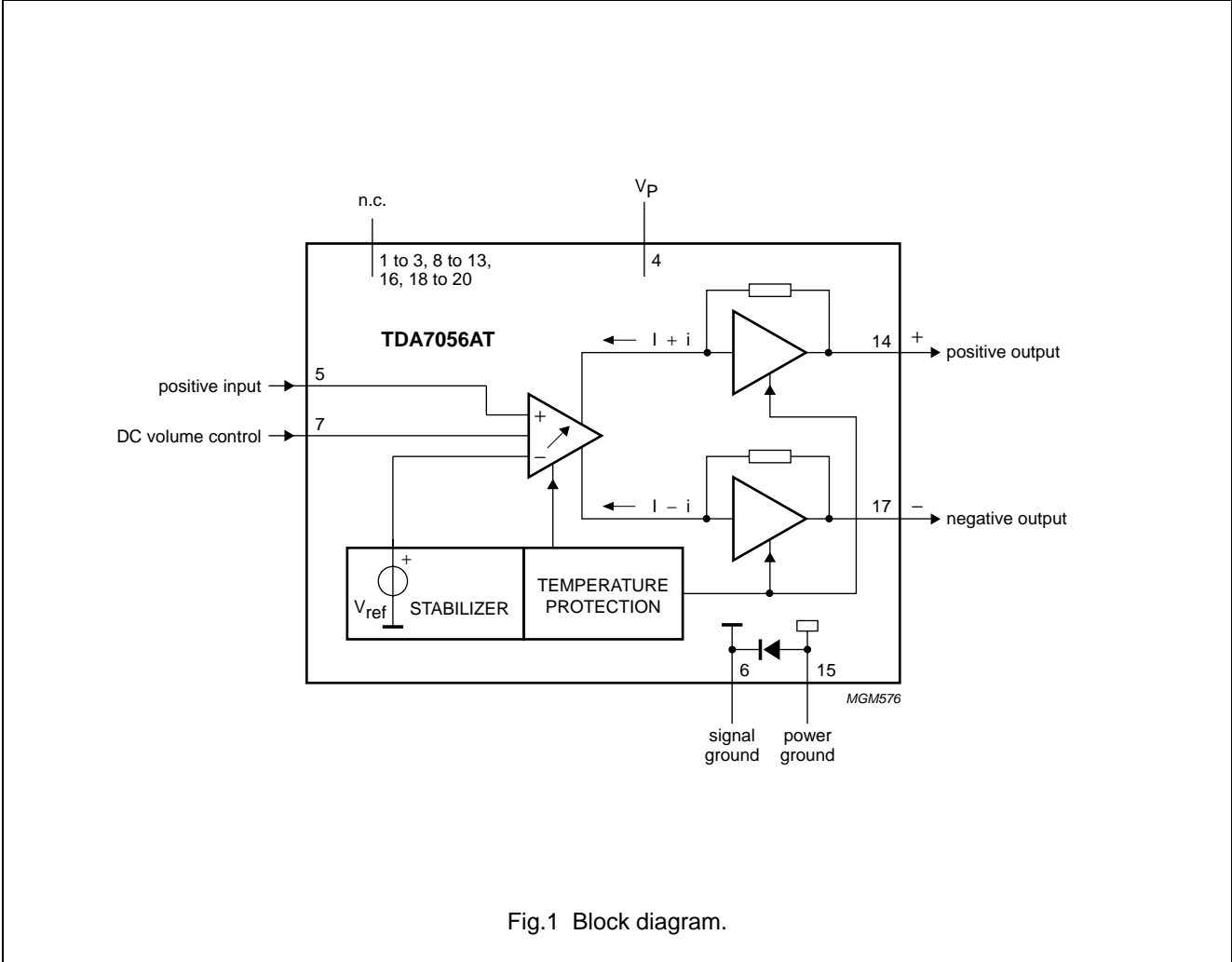


Fig.1 Block diagram.

3 W mono BTL audio amplifier with DC volume control

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PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
n.c.	3	not connected
V _P	4	positive supply voltage
V _I	5	positive input
GND1	6	signal ground
VC	7	DC volume control
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
OUT+	14	positive output
GND2	15	power ground
n.c.	16	not connected
OUT-	17	negative output
n.c.	18	not connected
n.c.	19	not connected
n.c.	20	not connected

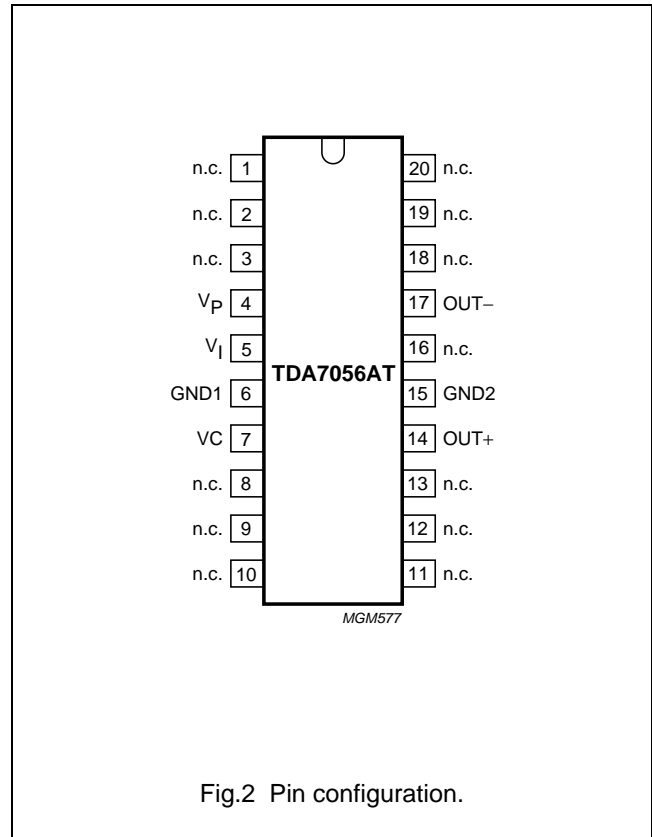


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

The TDA7056AT is a mono BTL output amplifier with DC volume control. It is designed for use in TVs and monitors but is also suitable for battery-fed portable recorders and radios.

In conventional DC volume circuits the control or input stage is AC-coupled to the output stage via external capacitors to keep the offset voltage low. In the TDA7056AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required. With this configuration, a low offset voltage is still maintained and the minimum supply voltage remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which also results in cost reductions. For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from +35.5 to -44 dB.

If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power. Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

Power dissipation

Assume $V_P = 12\text{ V}$; $R_L = 16\ \Omega$.

The maximum sine wave dissipation is 1.8 W.

The $R_{th\ vj-a}$ of the package is 60 K/W.

Therefore $T_{amb(max)} = 150 - 60 \times 1.8 = 42\ \text{°C}$.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
$V_{5,7}$	input voltage pins 5 and 7		–	5	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60\ \text{°C}$	–	1.5	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
t_{sc}	short-circuit time		–	1	h

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

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CHARACTERISTICS

$V_P = 12\text{ V}$; $V_{DC} = 1.4\text{ V}$; $f = 1\text{ kHz}$; $R_L = 16\ \Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$; unless otherwise specified (see Fig.14).

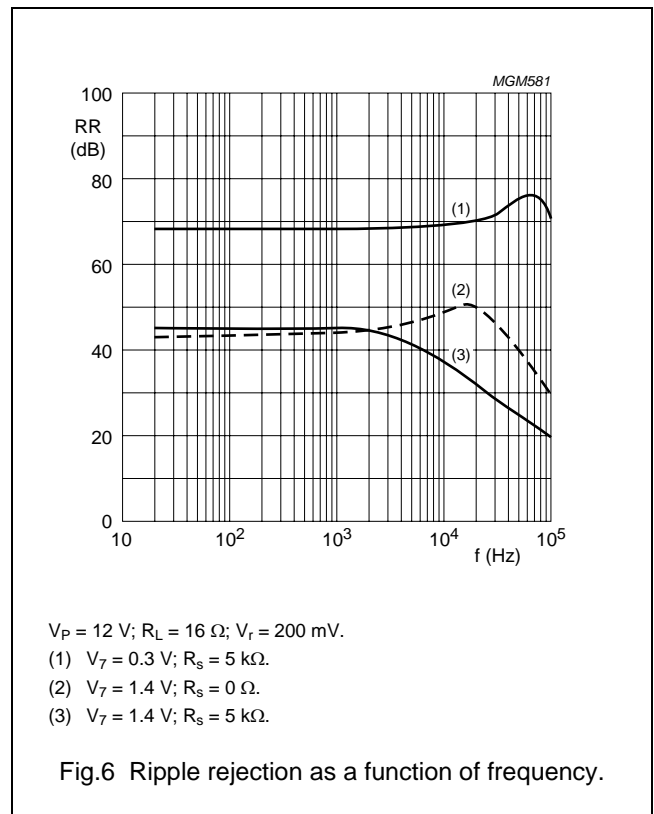
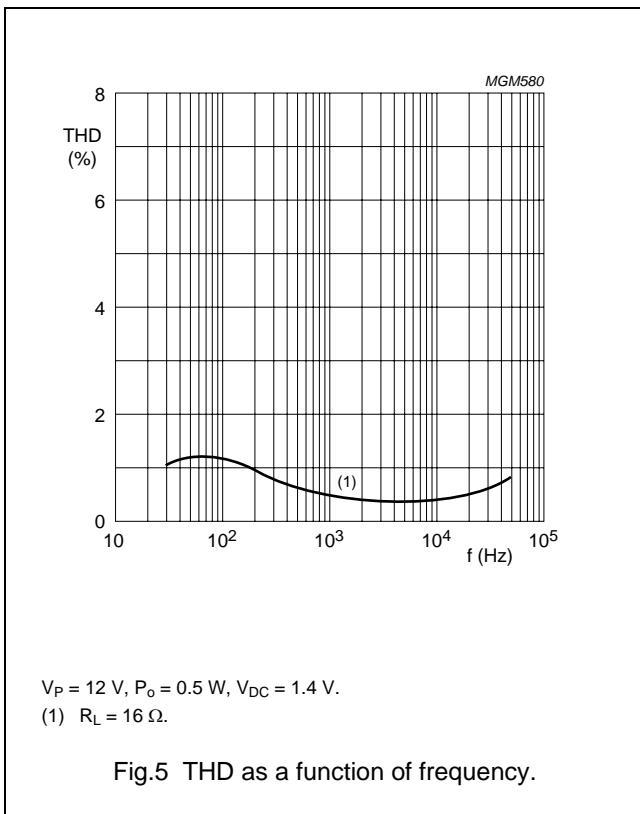
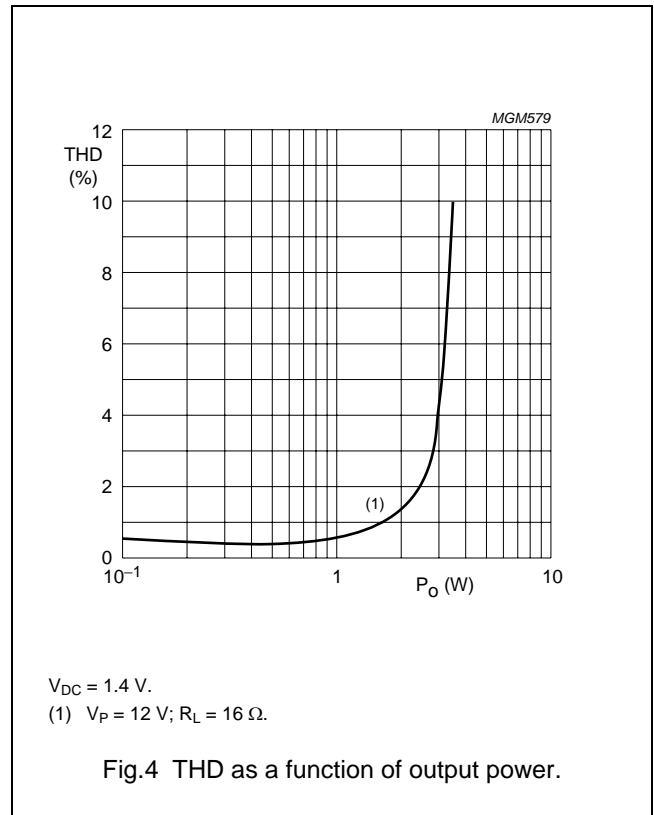
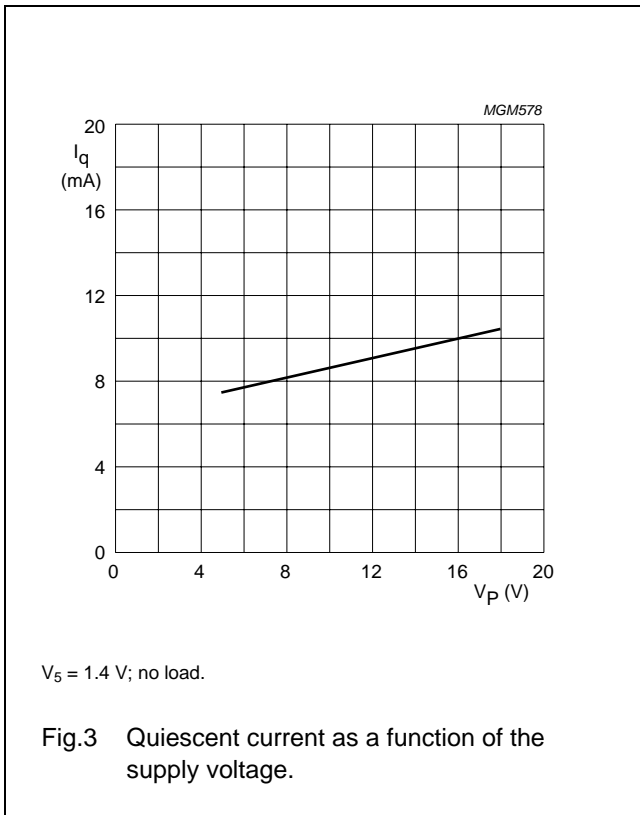
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	–	18	V
$I_{q(\text{tot})}$	total quiescent current	$R_L = \infty$; note 1	–	8	16	mA
Maximum gain ($V_7 = 1.4\text{ V}$)						
P_o	output power	THD = 10%; $R_L = 16\ \Omega$	3	3.5	–	W
THD	total harmonic distortion	$P_o = 0.5\text{ W}$	–	0.3	1	%
$G_{V(\text{max})}$	maximum total voltage gain		34.5	35.5	36.5	dB
$V_{i(\text{rms})}$	input signal handling (RMS value)	$V_{VC} = 0.8\text{ V}$; THD < 1%	0.5	0.65	–	V
$V_{n(o)(\text{rms})}$	noise output voltage (RMS value)	$f = 500\text{ kHz}$; note 2	–	210	–	μV
B	bandwidth	at –1 dB	–	0.02 to 300	–	kHz
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$ \Delta V_{OS} $	DC output offset voltage	$ V_{17} - v_{14} $	–	0	150	mV
Z_i	input impedance (pin 3)		15	20	25	$\text{k}\Omega$
Minimum gain ($V_7 = 0.5\text{ V}$)						
G_V	voltage gain		–	–44	–	dB
$V_{o(n)(\text{rms})}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
$V_{o(\text{mute})}$	output voltage in mute position	$V_{VC} \leq 0.3\text{ V}$; $V_I = 600\text{ mV}$; note 4	–	35	45	μV
DC volume control						
ΔG_V	voltage gain control range		75	80	–	dB
I_{VC}	control current	$V_{VC} = 0\text{ V}$	60	70	80	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L .
2. The noise output voltage ($V_{n(o)(\text{rms})}$) at $f = 500\text{ kHz}$, is measured with $R_s = 0\ \Omega$ and $B = 5\text{ kHz}$.
3. The ripple rejection is measured with $R_s = 0\ \Omega$ and $f = 100\text{ Hz}$ to 10 kHz . The ripple voltage ($V_{\text{ripple}} = 200\text{ mV RMS}$) is applied to the positive supply rail.
4. The noise output voltage ($V_{n(o)(\text{rms})}$) is measured with $R_s = 5\text{ k}\Omega$ unweighted.

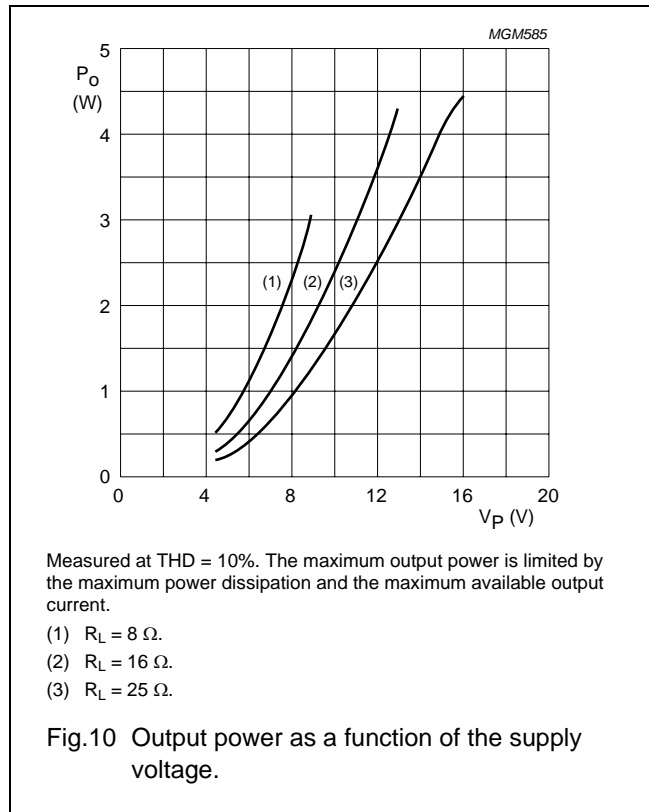
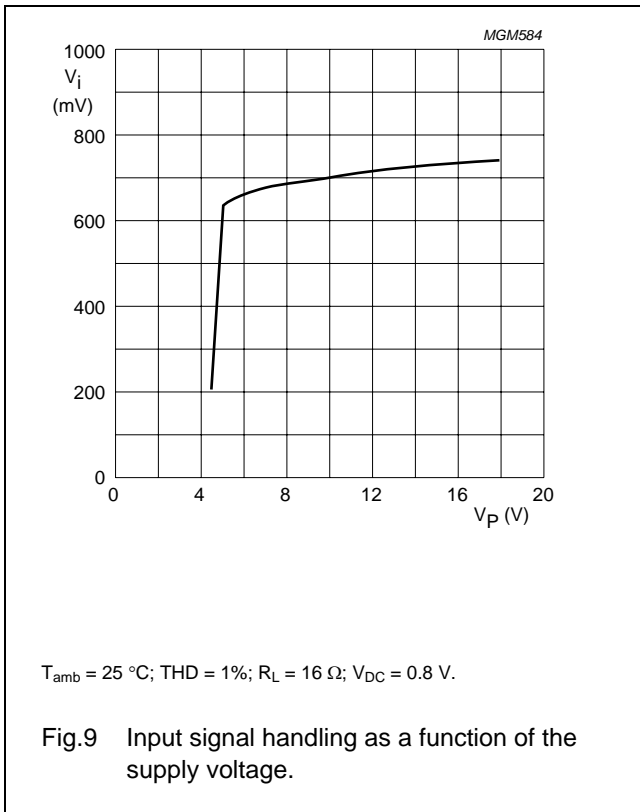
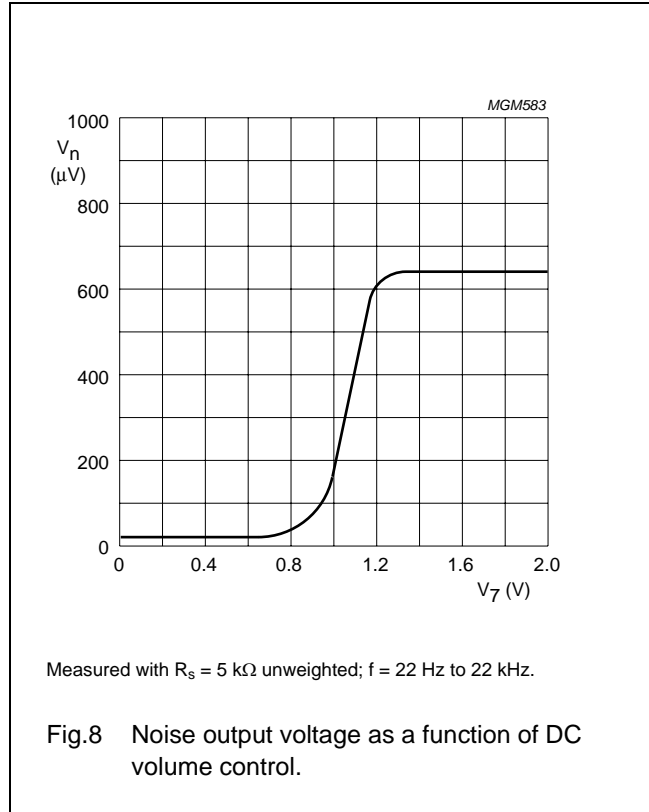
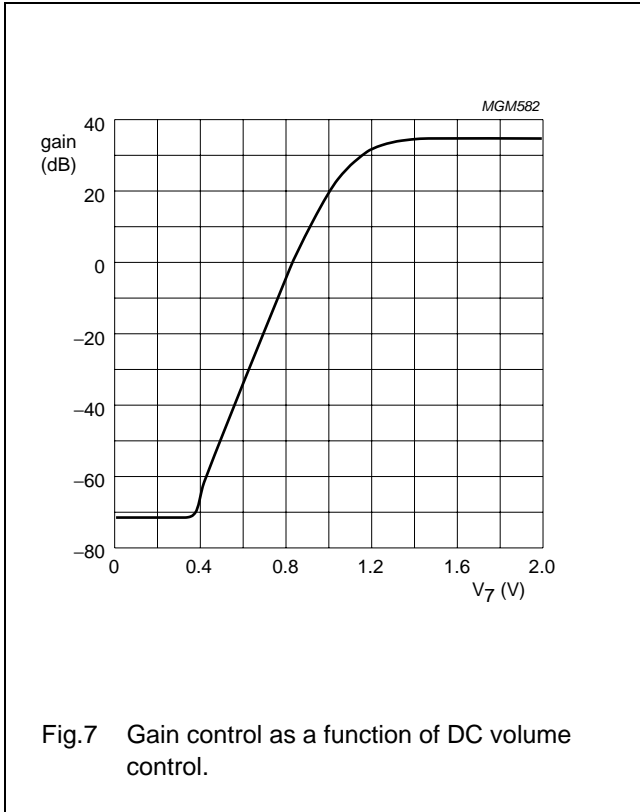
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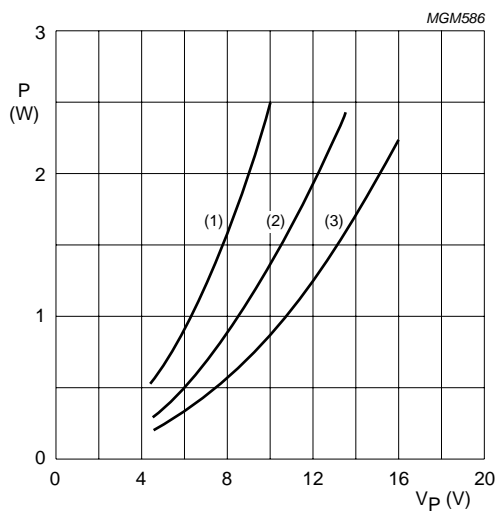
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- (1) $R_L = 8 \Omega$.
- (2) $R_L = 16 \Omega$.
- (3) $R_L = 25 \Omega$.

Fig.11 Total worst case power dissipation as a function of supply voltage.

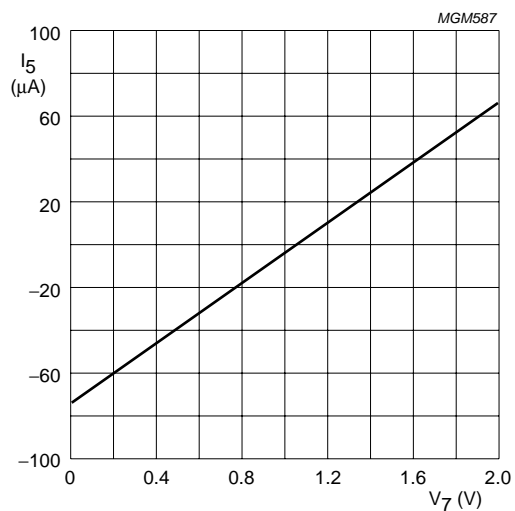
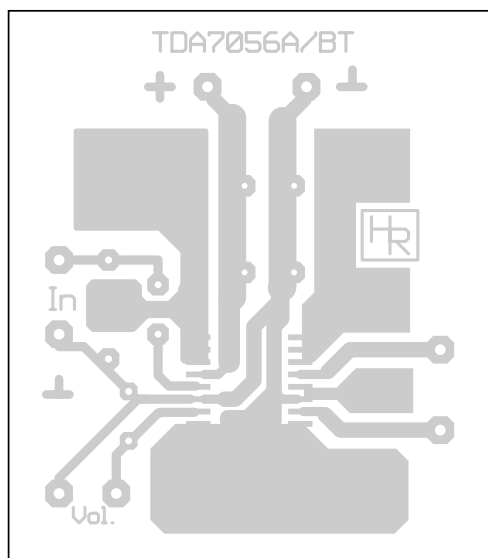


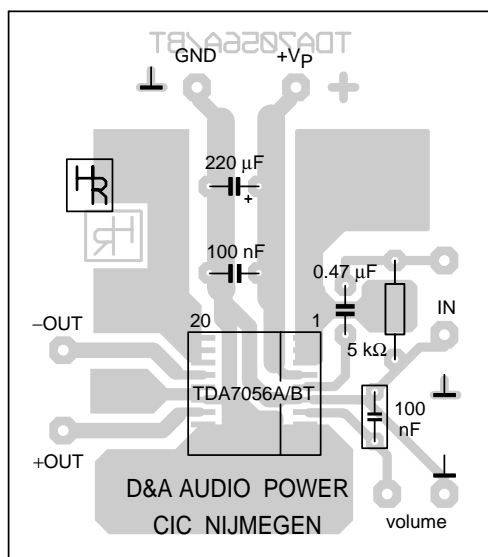
Fig.12 Control current as a function of DC volume control.

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a. Top view of bottom copper.



b. Top view of component side.

Fig.13 Printed-circuit board layout.

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TEST AND APPLICATION INFORMATION

Test conditions

$T_{amb} = 25\text{ °C}$ if not specified; $V_P = 12\text{ V}$; $V_{DC} = 1.4\text{ V}$;
 $f = 1\text{ kHz}$; $R_L = 16\text{ }\Omega$; audio bandpass: 22 Hz to 22 kHz.

In Figures 5 and 6 a low-pass filter of 80 kHz was applied. It should be noted that capacitive loads (100 pF and 5 nF) connected between the output pins to a common ground can cause oscillations. The BTL application circuit diagram is shown in Fig.14. To avoid instabilities and too high distortion, the input and power ground traces must be separated as far as possible and connected together as close as possible to the IC. The quiescent current has been measured without load impedance.

Voltage gain

The maximum closed-loop voltage gain has been internally fixed at 35.5 dB. The input sensitivity at maximum gain for $P_o = 3\text{ W}$ ($R_L = 16\text{ }\Omega$) is 115 mV. The gain bandwidth is 20 Hz to 300 kHz within 1 dB.

Output power

The output power as a function of supply voltage has been measured at THD = 10%. The maximum output power is limited by the maximum allowed power dissipation at $T_{amb} = 25\text{ °C}$ approximately 2 W, and the maximum available output current is 1.25 A repetitive peak current.

Switch-on/switch-off

The switch-on behaviour depends on the following:

- The rise time of the power supply (if $t_r > 40\text{ ms}$ for $V_P = 0$ to 12 V then the switch-on behaviour will be good)
- The input capacitor and source impedance (a higher source impedance and/or lower input capacitor value will have a positive influence on the switch-on/switch-off behaviour)
- The DC volume control pin (a capacitor of $>0.1\text{ }\mu\text{F}$ avoids disturbances).

Thermal behaviour:

The measured thermal resistance of the IC package is highly dependent on the configuration and size of the application board. Data may not be comparable between different semiconductor manufacturers because the application boards and test methods are not (yet) standardized. The thermal performance of packages for a specific application may also be different than presented here, because the configuration of the application boards (copper area) may be different. NXP Semiconductors uses FR-4 type application boards with 1 oz copper traces with solder coating. The measurements have been carried out with vertical placed boards.

Using a practical PCB layout with wider copper tracks and some copper area to the IC pins and just under the IC, the thermal resistance from junction to ambient can be reduced. In the demonstration application PCB the $R_{th(j-a)} = 56\text{ K/W}$ for the SO20 plastic package. For a maximum ambient temperature of $T_{amb} = 50\text{ °C}$ the following calculation can be made for the maximum power

$$\text{dissipation: } \frac{(150\text{ K/W} - 50\text{ K/W})}{56\text{ K/W}} = 1.79\text{ W}$$

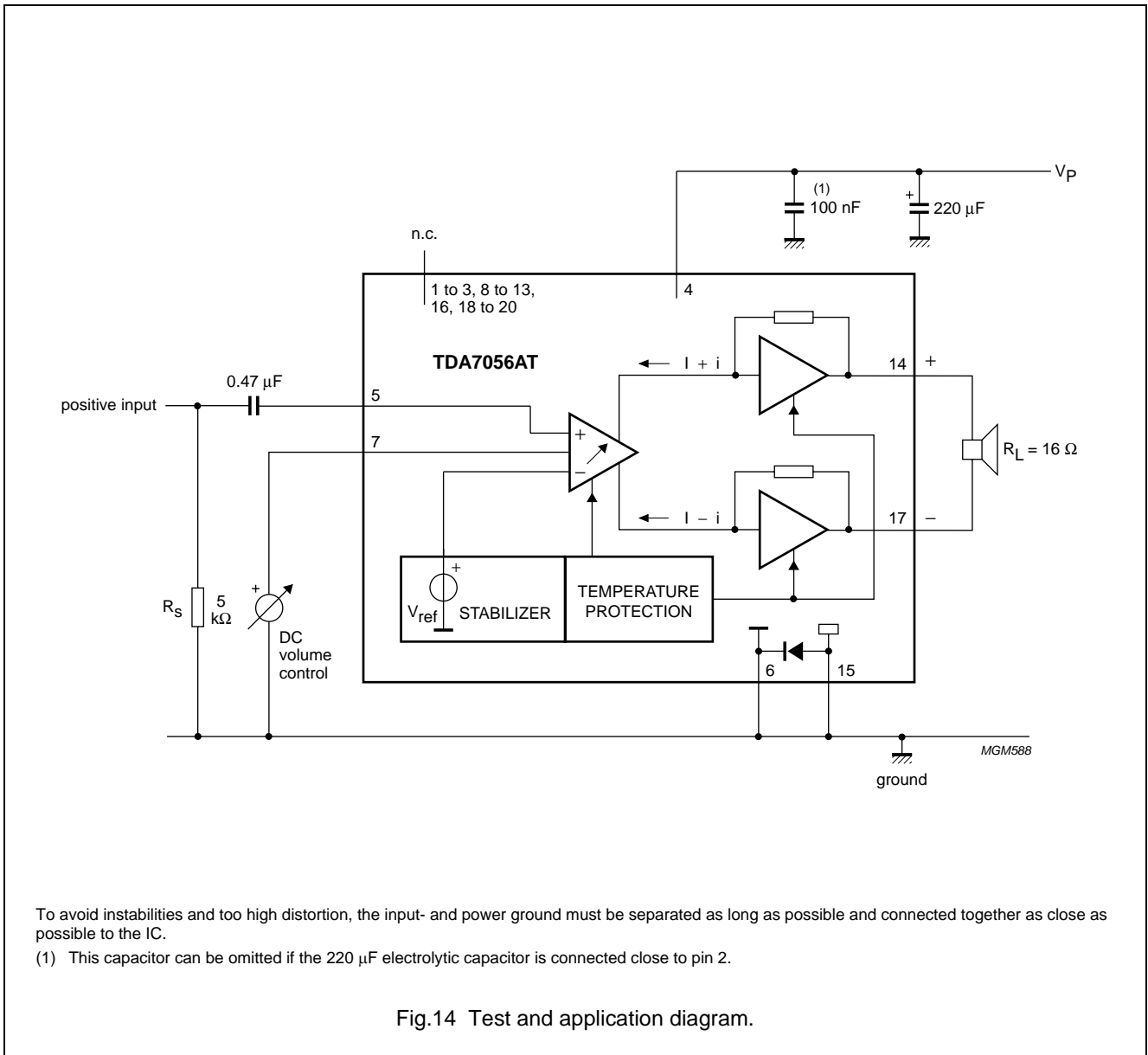
For the application at $V_P = 12\text{ V}$ and $R_L = 16\text{ }\Omega$ the worst case sine wave dissipation is 1.85 W. Because in practice the 'music-power' causes about the half of the sine wave dissipation, this application ($V_P = 12\text{ V}$; $R_L = 16\text{ }\Omega$) has been allowed.

Short-circuit protection:

The output pins (pins 14 and 17) can be short-circuited to ground respectively to $+V_P$. The Missing Current Limiter (MCL) protection circuit will shut-off the amplifier. Removing the short-circuit will reset the amplifier automatically. Short-circuit across the load (pins 14 and 17) will activate the thermal protection circuit; this will result in reducing the short-circuit current.

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For single-end application the output peak current may not exceed 100 mA; at higher output currents the short circuit protection (MLC) will be activated.

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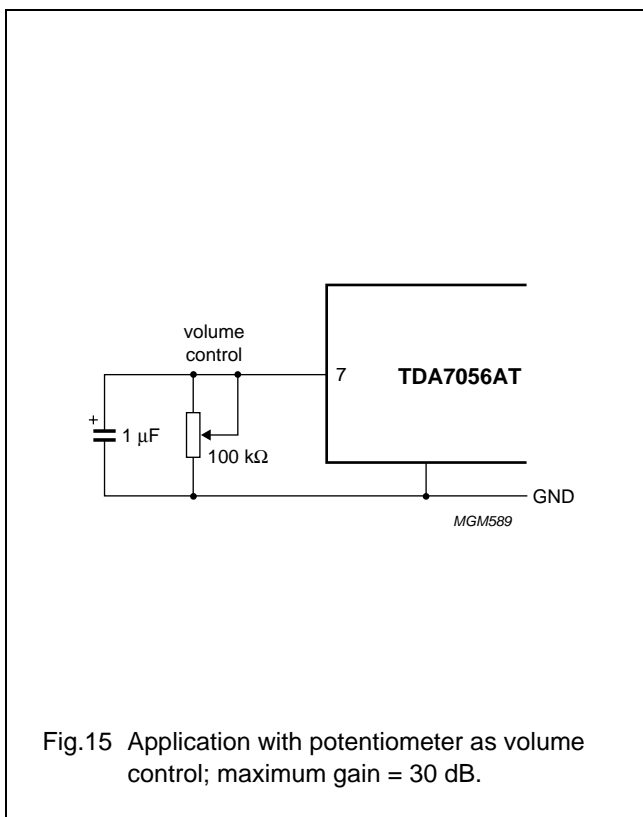


Fig.15 Application with potentiometer as volume control; maximum gain = 30 dB.

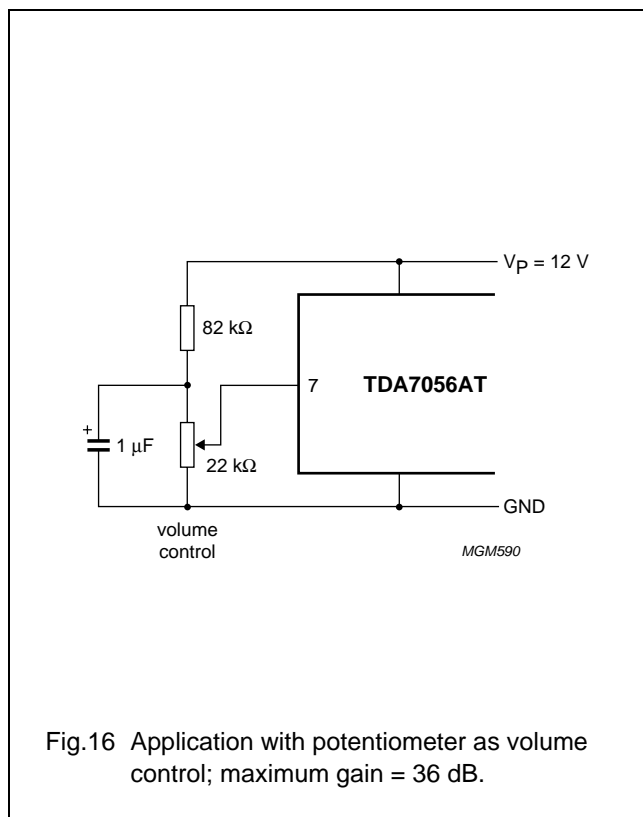


Fig.16 Application with potentiometer as volume control; maximum gain = 36 dB.

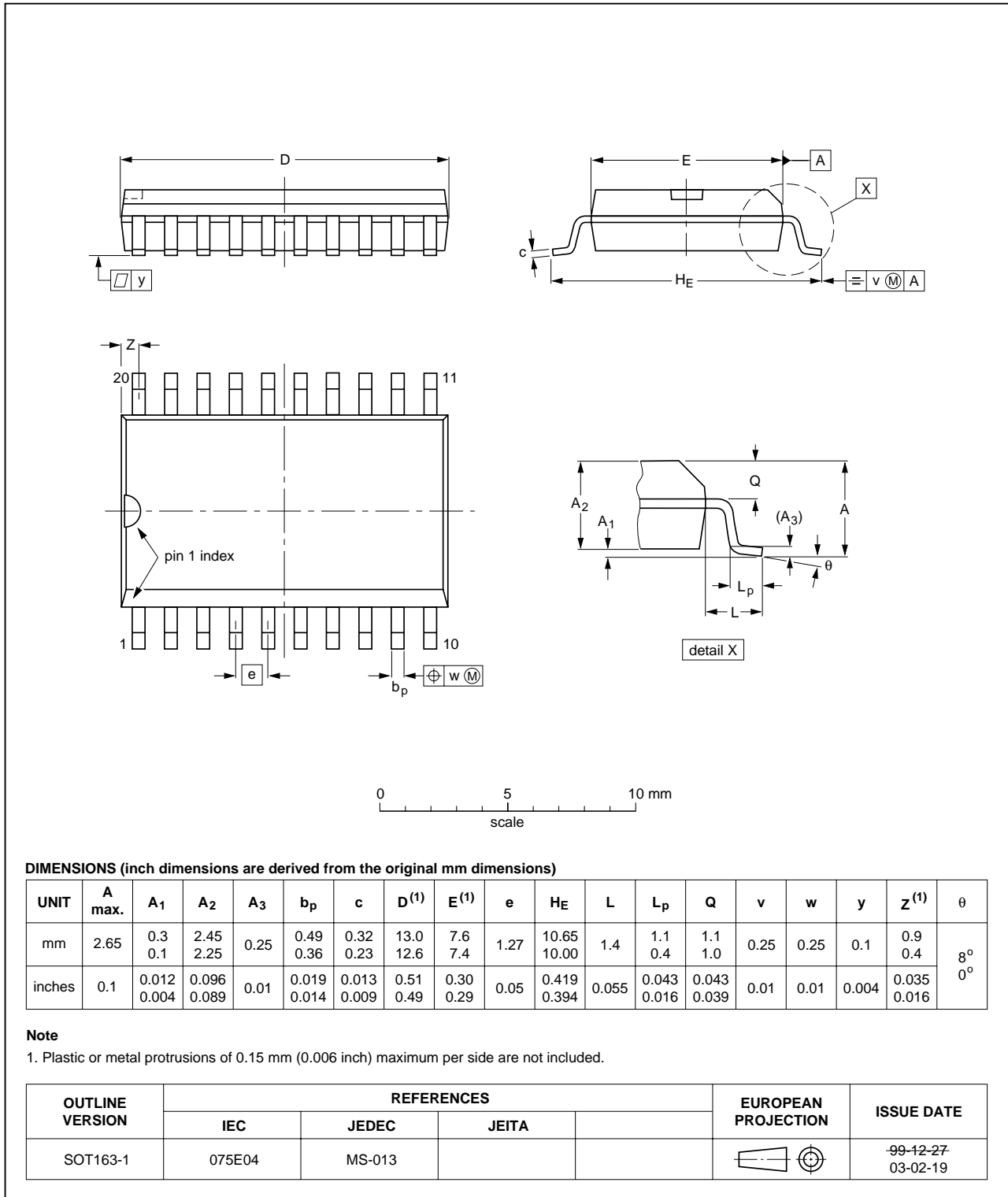
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PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

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