

TLE8888-1QK

Engine Management System IC for 4 Cylinder Cars

Engine Management System IC TLE8888-1QK
TLE8888QK
TLE8888-2QK

Data Sheet

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Table of Contents

1	Overview	5
1.1	Abbreviations	7
2	Block Diagram	8
3	Pin Configuration	9
3.1	Pin Assignment	9
3.2	Pin Definitions and Functions	9
4	General Product Characteristics	13
5	Operation Behavior	17
5.1	Operation States	18
5.2	Reset and Operation Modes	22
5.3	Electrical Characteristics Operation Behavior	29
6	Monitoring Watchdog Module (Signature Watchdog)	31
6.1	Window Watchdog	33
6.2	Functional Watchdog	35
6.2.1	Question and Response Definition	37
6.3	Total Error Counter Module	38
6.4	Watchdog Reset Counter	39
6.5	Power Down Counter	39
6.6	Secure Shut Off Timer	39
6.7	Operation State Definition and Reset Generation	40
6.8	Synchronisation of Window Watchdog Sequence and Heartbeat	42
6.9	Electrical Characteristics Monitoring Watchdog Module	43
7	Wake Up Detection and Main Relay Driver	44
7.1	Wake Up Detection by Pin <i>KEY</i> and Key Off Delay	45
7.2	Wake Up Detection by Pin <i>WK</i>	46
7.3	Main Relay Driver	49
7.4	Engine Off Timer	49
7.5	Electrical Characteristics Key Detection, Wake Up Detection and Main Relay Driver	53
8	Power Supply	56
8.1	Pre-Regulator	56
8.2	5V Main Supply	57
8.3	Sensor Supply	57
8.4	IO Supply	57
8.5	Standby Supply	57
8.6	Charge Pump	57
8.7	Voltage Monitoring	57
8.8	Electrical Characteristics Power Supply	57
9	Power Stages	61
9.1	Power Stage Control	62
9.2	Power Stages Enable	63
9.3	Power Stages Configuration	63
9.4	Special Function "Delayed Switch Off" for <i>OUT17</i> and <i>OUT21</i>	64
9.5	Electrical Characteristics Direct Drive Inputs	66
9.6	Low Side Switches <i>OUT1</i> to <i>OUT7</i> and <i>OUT14</i> to <i>OUT20</i>	68
9.6.1	Protection of <i>OUT1</i> to <i>OUT7</i> and <i>OUT14</i> to <i>OUT20</i>	68
9.6.2	Diagnosis of <i>OUT1</i> to <i>OUT7</i> and <i>OUT14</i> to <i>OUT20</i>	68

Table of Contents

9.6.3	Electrical Characteristics Low Side Switches <i>OUT1</i> to <i>OUT7</i> and <i>OUT14</i> to <i>OUT20</i>	69
9.7	Half Bridges <i>OUT21</i> to <i>OUT24</i>	73
9.7.1	Protection of Half Bridges <i>OUT21</i> to <i>OUT24</i>	74
9.7.2	Diagnosis of Half Bridges <i>OUT21</i> to <i>OUT24</i>	75
9.7.3	Electrical Characteristics Half Bridges	78
9.8	Push Pull Stages <i>OUT8</i> to <i>OUT13</i> and <i>DFB8</i> to <i>DFB13</i>	80
9.8.1	Protection of <i>OUT8</i> to <i>OUT13</i>	80
9.8.2	Diagnosis of <i>OUT8</i> to <i>OUT13</i>	80
9.8.3	Electrical Characteristics Push Pull Stages <i>OUT8</i> to <i>OUT13</i>	81
9.9	Push Pull Stages <i>IGN1</i> to <i>IGN4</i>	82
9.9.1	Protection of <i>IGN1</i> to <i>IGN4</i>	82
9.9.2	Diagnosis of <i>IGN1</i> to <i>IGN4</i>	82
9.9.3	Electrical Characteristics Push Pull Stages <i>IGN1</i> to <i>IGN4</i>	83
10	VR and Hall Sensor Interface	85
10.1	Signal Detection	85
10.2	Detection Modes	87
10.3	Diagnosis for VR Sensor Signal Detection Modes	87
10.4	Electrical Characteristics VR Sensor Interface	92
11	Local Interconnect Network (LIN)	94
11.1	Operation Modes	95
11.2	Failure Modes in LIN/K-Line Operation	95
11.2.1	Performance in Non Operation Supply Voltage Range	95
11.2.2	Loss of Supply Voltage and GND Connection	95
11.2.3	Bus Wiring Short to Battery or GND	96
11.2.4	TX Time Out	96
11.2.5	Over Temperature Protection	96
11.3	Electrical Characteristics LIN	97
12	High Speed Controller Area Network (CAN) Transceiver	101
12.1	Functional Description	101
12.2	Operation Modes	101
12.2.1	Normal Operation Mode	102
12.2.2	Receive Only Mode	102
12.2.3	Power Down Mode	102
12.2.4	Remote Wake Up	102
12.3	Diagnostic Functions	104
12.3.1	CAN Bus Failure Detection	104
12.3.2	Local Failure Detection	104
12.4	Electrical Characteristics CAN Transceiver	105
13	Micro Second Channel MSC	107
13.1	Downstream Communication	107
13.1.1	Downstream Supervisory Functions	109
13.1.2	Command Frame	110
13.1.3	Data Frame	110
13.2	Upstream Communication	112
13.3	Timing Characteristics	114
13.4	Electrical Characteristics	115
14	Register and Commands	118
14.1	Register Table	122
14.2	Command Register	124

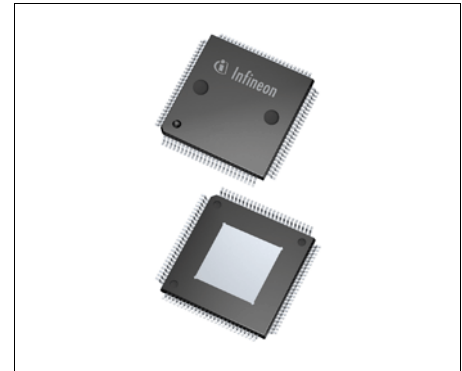
Table of Contents

14.3	Diagnosis Register	138
14.4	Status Register	149
14.5	Configuration Register	156
14.6	Control Register	186
15	SPI	191
15.1	SPI Protocol	191
15.2	SPI Frame Definition	193
15.3	Electrical Characteristics SPI	194
16	EMC Requirements	195
16.1	ISO Pulse Tests	195
17	Application Information	196
17.1	Supply Systems	197
17.2	VR Sensor Interface	198
18	Package Outlines	200
19	Revision History	201

Engine Management System IC

1 Overview
Features

- Voltage pre-regulator
- Integrated 5V regulator
- 2 integrated 5V trackers
- Standby regulator
- Separate internal supply
- Voltage monitoring
- High speed CAN interface with wake up by bus
- LIN interface with high speed mode for K-Line operation
- Variable reluctance sensor interface
- Micro Second Channel interface (MSC) with low voltage differential signal (LVDS) inputs pads for low EME
- SPI and direct control inputs for high flexibility
- Main relay driver
- Ignition Key detection with key off delay output
- Wake up input
- Engine off timer
- 4 low side power stages especially to drive injectors ($R_{on}=550m\Omega$) with enable input
- 3 low side power stages ($R_{on}=350m\Omega$)
- 6 push pull stages for driving on-board MOSFET with drain feedback
- 7 low side power stages especially to drive relays ($R_{on}=1.5\Omega$), one with delayed switch off functionality
- 4 half bridge stages for high flexibility, one with delayed switch off functionality
- 4 push pull stages for driving on- and off- board IGBT with back supply suppression and high voltage capability
- Open-load, short-to-GND and short-to-BAT diagnostic
- Over temperature and short-to-BAT protection
- Monitoring watchdog module
- Green Product (RoHS compliant)
- AEC Qualified


LQFP-100
Description

The device is a U-Chip suitable for automotive engine management systems. It contains the basic functionality to supply the micro controller and the ECU, establish the communication on- and off- board and drive EMS typical actuators. Furthermore it controls the main relay driver.

Type	Package	Marking
TLE8888-1QK	LQFP-100	TLE8888-1QK
TLE8888QK	LQFP-100	TLE8888QK
TLE8888-2QK	LQFP-100	TLE8888-2QK

Device Variants TLE8888QK and TLE8888-2QK

The device variants TLE8888QK and TLE8888-2QK differ from the main version TLE8888-1QK in the watchdog functionality.

The TLE8888QK has a fixed set of parameter for the watchdog (see datasheet addendum "TLE8888QK - Addendum").

For the TLE8888-2QK the watchdog function is disabled (see datasheet addendum "TLE8888-2QK - Addendum").

Only the main version TLE8888-1QK is described in this datasheet.

For order conditions please contact the nearest Infineon Technologies office.

1.1 Abbreviations

Table 1 Abbreviations

Symbol	Explanation
MSC	Micro second channel
SPI	Serial peripheral interface
LVDS	Low voltage differential signal
EME	Electromagnetic emission
EMI	Electromagnetic interference
LIN	Local interconnect network
HS CAN	High speed controller area network

2 Block Diagram

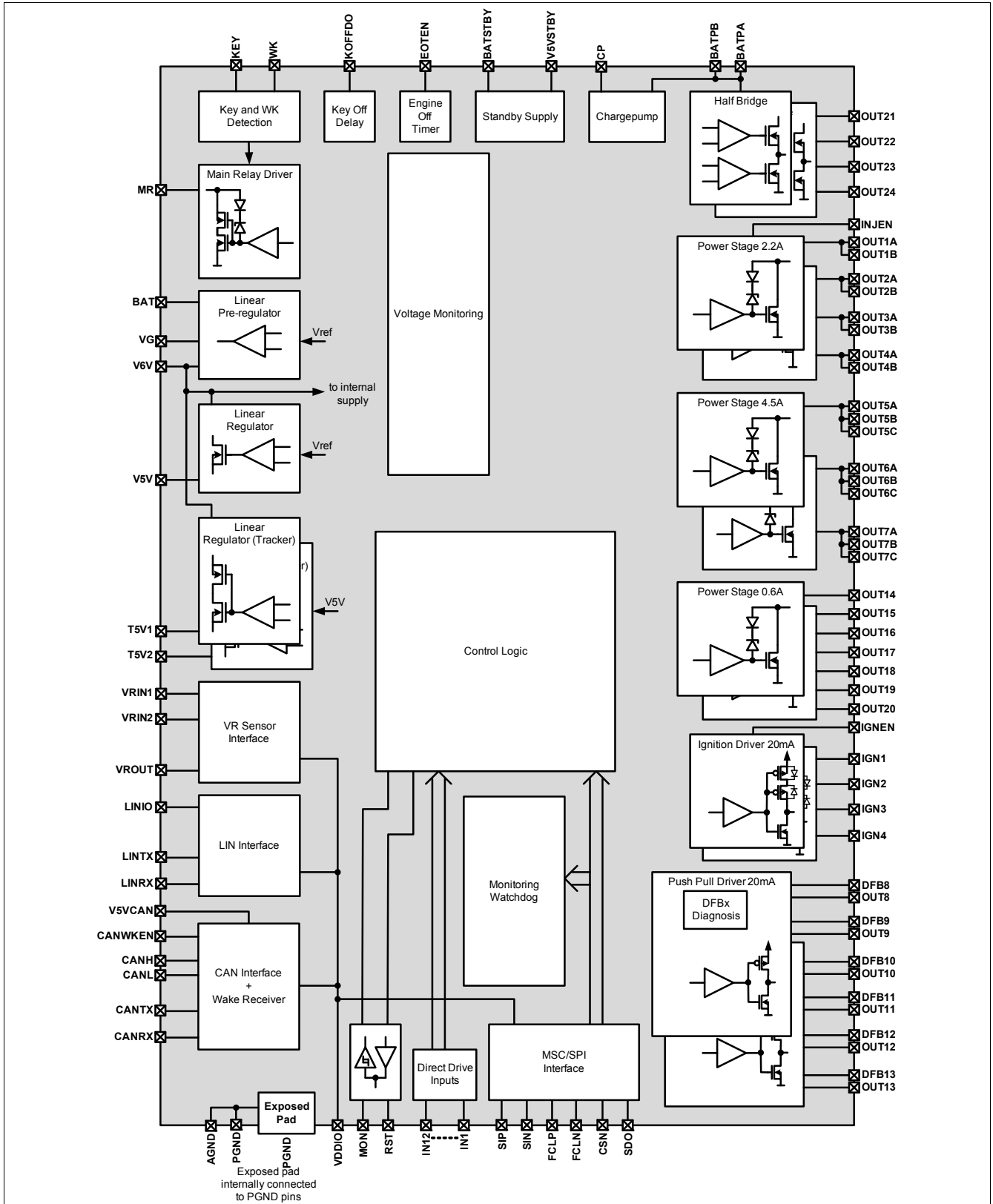


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

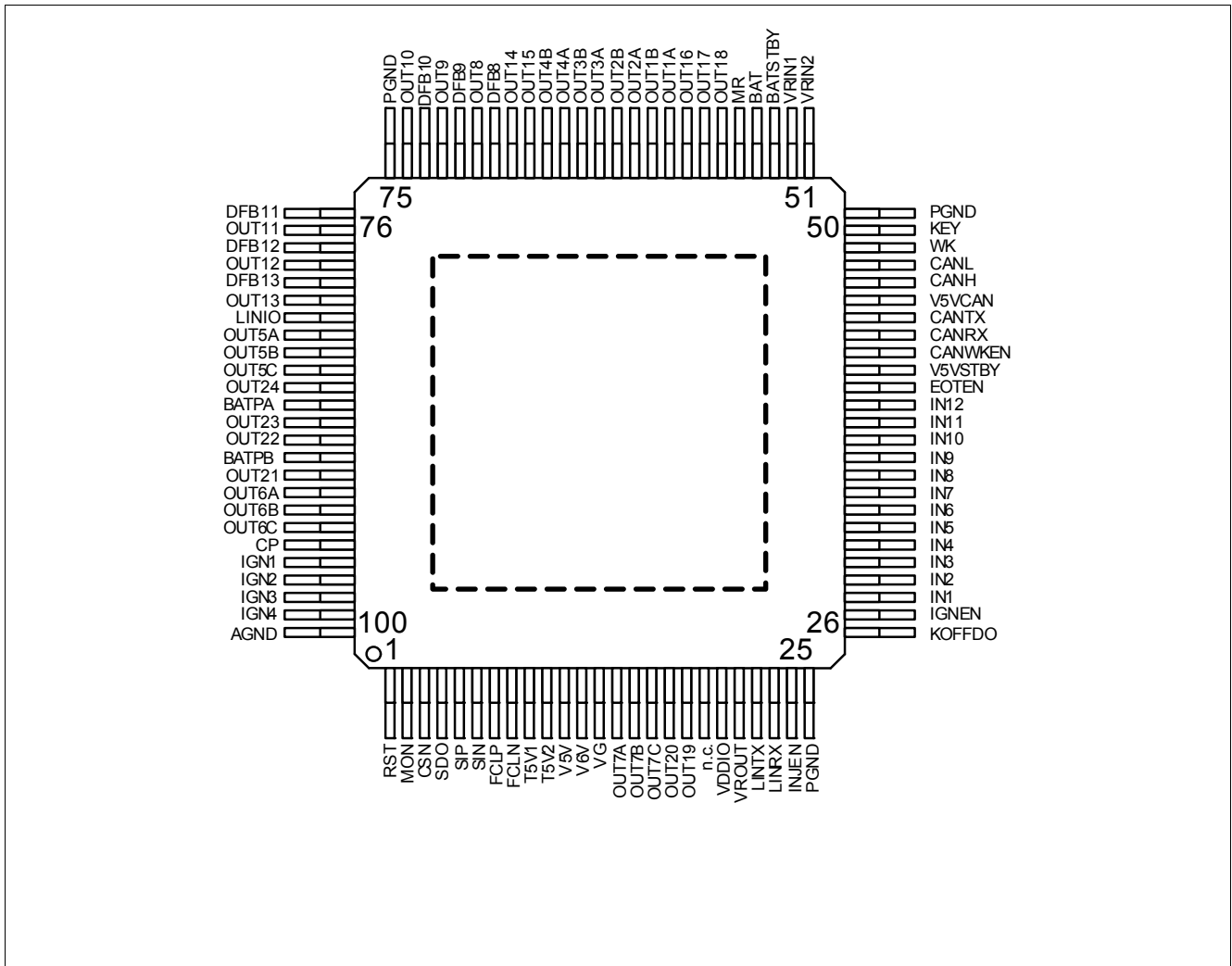


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function	Function
1	<i>RST</i>	IN/OUT	Reset ; Bidirectional pin for reset functions
2	<i>MON</i>	IN/OUT	Monitor ; Bidirectional pin for monitoring functions
3	<i>CSN</i>	IN	MSC/SPI slave chip select ; Single ended chip select for MSC and SPI
4	<i>SDO</i>	OUT	MSC/SPI serial data output ; Output for MSC and SPI
5	<i>SIP</i>	IN	MSC/SPI Data input ; positive data input of LVDS in MSC mode or single ended data input in SPI mode

Pin Configuration

Pin	Symbol	Function	Function
6	<i>SIN</i>	IN	MSC data input or select input; negative data input of LVDS in MSC mode or select input for SPI mode
7	<i>FCLP</i>	IN	MSC/SPI Clock input; positive clock input of LVDS in MSC mode or single ended clock input in SPI mode
8	<i>FCLN</i>	IN	Select input or MSC clock input; negative clock input of LVDS in MSC mode or select input for single ended mode (SPI or MSC)
9	<i>T5V1</i>	OUT	5V tracker; Supply voltage for off- board sensors
10	<i>T5V2</i>	OUT	5V tracker; Supply voltage for off- board sensors
11	<i>V5V</i>	OUT	5V supply; Supply voltage for main functions of the ECU
12	<i>V6V</i>	IN	Source of external pre-regulator
13	<i>VG</i>	OUT	Gate of external pre-regulator
14	<i>OUT7A</i>	OUT	Low side power stage; Must be connected to <i>OUT7B</i> and <i>OUT7C</i> without any parasitic
15	<i>OUT7B</i>	OUT	Low side power stage; Must be connected to <i>OUT7A</i> and <i>OUT7C</i> without any parasitic
16	<i>OUT7C</i>	OUT	Low side power stage; Must be connected to <i>OUT7A</i> and <i>OUT7B</i> without any parasitic
17	<i>OUT20</i>	OUT	Low side small signal stage;
18	<i>OUT19</i>	OUT	Low side small signal stage;
19	n.c.		leave open or connect to GND
20	<i>VDDIO</i>	Supply	Supply input for logic level inputs and outputs
21	<i>VR0UT</i>	OUT	Output of variable reluctance sensor interface; Digital output to micro controller
22	<i>LINTX</i>	IN	Transmit digital input for LIN interface;
23	<i>LINRX</i>	OUT	Receive digital output for LIN interface;
24	<i>INJEN</i>	IN	Injector enable input;
25	<i>PGND</i>	GND	Power ground; internally connected to cooling tab
26	<i>KOFFDO</i>	OUT	Key off delay output;
27	<i>IGNEN</i>	IN	Ignition enable input;
28	<i>IN1</i>	IN	Parallel input; Input pin for direct control of power stage OUT1,
29	<i>IN2</i>	IN	Parallel input; Input pin for direct control of power stage OUT2
30	<i>IN3</i>	IN	Parallel input; Input pin for direct control of power stage OUT3
31	<i>IN4</i>	IN	Parallel input; Input pin for direct control of power stage OUT4
32	<i>IN5</i>	IN	Parallel input; Input pin for direct control of push pull state IGN1
33	<i>IN6</i>	IN	Parallel input; Input pin for direct control of push pull state IGN2
34	<i>IN7</i>	IN	Parallel input; Input pin for direct control of push pull state IGN3
35	<i>IN8</i>	IN	Parallel input; Input pin for direct control of push pull state IGN4
36	<i>IN9</i>	IN	Parallel input; Input pin for direct control of power stages, could be multiplexed to various stages
37	<i>IN10</i>	IN	Parallel input; Input pin for direct control of power stages, could be multiplexed to various stages
38	<i>IN11</i>	IN	Parallel input; Input pin for direct control of power stages, could be multiplexed to various stages

Pin Configuration

Pin	Symbol	Function	Function
39	<i>INI2</i>	IN	Parallel input; Input pin for direct control of power stages, could be multiplexed to various stages
40	<i>EOTEN</i>	IN	Engine off timer enable input;
41	<i>V5VSTBY</i>	OUT	5V standby supply; Supply voltage in sleep mode
42	<i>CANWKEN</i>	IN	Enable input for remote CAN wake up;
43	<i>CANRX</i>	OUT	Receive digital output for CAN;
44	<i>CANTX</i>	IN	Transmit digital input for CAN;
45	<i>V5VCAN</i>	Supply	5V supply input for CAN;
46	<i>CANH</i>	IN/OUT	CAN bus high;
47	<i>CANL</i>	IN/OUT	CAN bus low;
48	<i>WK</i>	IN	Wake up input; Input signal and supply for MR
49	<i>KEY</i>	IN	Key input; Input signal and supply for MR
50	<i>PGND</i>	GND	Power ground; internally connected to cooling tab
51	<i>VRIN2</i>	IN	Differential input of variable reluctance sensor; Analog input from sensor
52	<i>VRIN1</i>	IN	Differential input of variable reluctance sensor; Analog input from sensor
53	<i>BATSTBY</i>	Supply	Battery input for standby supply; Battery supply voltage standby supply regulator
54	<i>BAT</i>	Supply	Battery; Supply voltage for main functions of the device.
55	<i>MR</i>	OUT	Low side power stage for main relay;
56	<i>OUT18</i>	OUT	Low side power stage;
57	<i>OUT17</i>	OUT	Low side power stage;
58	<i>OUT16</i>	OUT	Low side power stage;
59	<i>OUT1A</i>	OUT	Low side power stage; Must be connected to <i>OUT1B</i> without any parasitic
60	<i>OUT1B</i>	OUT	Low side power stage; Must be connected to <i>OUT1A</i> without any parasitic
61	<i>OUT2A</i>	OUT	Low side power stage; Must be connected to <i>OUT2B</i> without any parasitic
62	<i>OUT2B</i>	OUT	Low side power stage; Must be connected to <i>OUT2A</i> without any parasitic
63	<i>OUT3A</i>	OUT	Low side power stage; Must be connected to <i>OUT3B</i> without any parasitic
64	<i>OUT3B</i>	OUT	Low side power stage; Must be connected to <i>OUT3A</i> without any parasitic
65	<i>OUT4A</i>	OUT	Low side power stage; Must be connected to <i>OUT4B</i> without any parasitic
66	<i>OUT4B</i>	OUT	Low side power stage; Must be connected to <i>OUT4A</i> without any parasitic
67	<i>OUT15</i>	OUT	Low side power stage;
68	<i>OUT14</i>	OUT	Low side power stage;
69	<i>DFB8</i>	IN	Drain Feedback; Related to OUT8
70	<i>OUT8</i>	OUT	Push pull stage; To control on- board MOSFET
71	<i>DFB9</i>	IN	Drain Feedback; Related to OUT9
72	<i>OUT9</i>	OUT	Push pull stage; To control on- board MOSFET
73	<i>DFB10</i>	IN	Drain Feedback; Related to OUT10
74	<i>OUT10</i>	OUT	Push pull stage; To control on- board MOSFET
75	<i>PGND</i>	GND	Power ground; internally connected to cooling tab
76	<i>DFB11</i>	IN	Drain Feedback; Related to OUT11
77	<i>OUT11</i>	OUT	Push pull stage; To control on- board MOSFET

Pin Configuration

Pin	Symbol	Function	Function
78	<i>DFB12</i>	IN	Drain Feedback; Related to <i>OUT12</i>
79	<i>OUT12</i>	OUT	Push pull stage; To control on- board MOSFET
80	<i>DFB13</i>	IN	Drain Feedback; Related to <i>OUT13</i>
81	<i>OUT13</i>	OUT	Push pull stage; To control on- board MOSFET
82	<i>LINIO</i>	IN/OUT	BUS for LIN interface;
83	<i>OUT5A</i>	OUT	Low side power stage; Must be connected to <i>OUT5B</i> and <i>OUT5C</i> without any parasitic
84	<i>OUT5B</i>	OUT	Low side power stage; Must be connected to <i>OUT5A</i> and <i>OUT5C</i> without any parasitic
85	<i>OUT5C</i>	OUT	Low side power stage; Must be connected to <i>OUT5A</i> and <i>OUT5B</i> without any parasitic
86	<i>OUT24</i>	OUT	Half bridge stage;
87	<i>BATPA</i>	Supply	Battery; Supply voltage for half bridges and the charge pump; must be connected to <i>BATPB</i> without any parasitic
88	<i>OUT23</i>	OUT	Half bridge stage;
89	<i>OUT22</i>	OUT	Half bridge stage;
90	<i>BATPB</i>	Supply	Battery; Supply voltage for half bridges and the charge pump; must be connected to <i>BATPA</i> without any parasitic
91	<i>OUT21</i>	OUT	Half bridge stage;
92	<i>OUT6A</i>	OUT	Low side power stage; Must be connected to <i>OUT6B</i> and <i>OUT6C</i> without any parasitic
93	<i>OUT6B</i>	OUT	Low side power stage; Must be connected to <i>OUT6A</i> and <i>OUT6C</i> without any parasitic
94	<i>OUT6C</i>	OUT	Low side power stage; Must be connected to <i>OUT6A</i> and <i>OUT6B</i> without any parasitic
95	<i>CP</i>	OUT	Charge pump; add external capacitance to stabilise charge pump voltage
96	<i>IGN1</i>	OUT	Push pull stage; To control on- or off- board IGBT
97	<i>IGN2</i>	OUT	Push pull stage; To control on- or off- board IGBT
98	<i>IGN3</i>	OUT	Push pull stage; To control on- or off- board IGBT
99	<i>IGN4</i>	OUT	Push pull stage; To control on- or off- board IGBT
100	<i>AGND</i>	GND	Signal ground; internally connected to <i>PGND</i> and cooling tab
Cooling tab ¹⁾	<i>PGND</i>	GND	Power ground; internally connected PGND pins

1) Cooling tab is also called exposed pad

4 General Product Characteristics

General definition:

V_S is the short cut for all battery supplies of the TLE8888-1QK (*BAT, BATPA, BATPB, BATSTBY*) unless otherwise specified

GND is the short cut for all grounds of the TLE8888-1QK (*AGND, PGND*) unless otherwise specified.

Table 2 Absolute Maximum Ratings¹⁾

$T_j = -40$ to 150°C , all voltages with respect to *GND*, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
BATPA, BATPB, OUT8...13, DFB8...13	$V_{BATPA,MR}$, $V_{BATPB,MR}$, $V_{OUT8...13,MR}$, $V_{DFB8...13,MR}$	-0.3	–	40	V	–	P_4.1
CP	$V_{CP,MR}$	-0.3	–	45	V	$-0.3V < V_{CP} - V_{BATPA} < 5V$	P_4.2
OUT1...7, OUT14...20	$V_{OUT1..7,MR}$, $V_{OUT14..20,MR}$	-0.3	–	50	V	OUTn is switched off, clamping is allowed according Chapter 9.6	P_4.3
V6V	$V_{V6V,MR}$	-0.3	–	10	V	–	P_4.4
VG	$V_{VG,MR}$	-0.3	–	12	V	$V_{VG} - V_{V6V} < 5V$	P_4.5
V5V, V5VSTBY, VDDIO, V5VCAN	$V_{V5V,MR}$, $V_{V5VSTBY,MR}$, $V_{VDIO,MR}$, $V_{V5VCAN,MR}$	-0.3	–	5.5	V	–	P_4.6
T5V1, T5V2, IGN1...4	$V_{T5V1,MR}$, $V_{T5V2,MR}$, $V_{IGN1...4,MR}$	-1	–	40	V	–	P_4.7
BAT, BATSTBY, KEY, WK, MR	$V_{BAT,MR}$, $V_{KEY,MR}$, $V_{WK,MR}$, $V_{BATSTBY,MR}$, $V_{MR,MR}$	-16	–	40	V	–	P_4.8
IN1...12, SIP, SIN, FCLP, FCLN, CSN, LINTX, CANTX, IGNEN, INJEN, CANWKEN, EOTEN	$V_{IN1...12,MR}$, $V_{FCLP,MR}$, $V_{FCLN,MR}$, $V_{SIP,MR}$, $V_{SIN,MR}$, $V_{CSN,MR}$, $V_{LINTX,MR}$, $V_{CANTX,MR}$, $V_{IGNEN,MR}$, $V_{INJEN,MR}$, $V_{EOTEN,MR}$, $V_{CANWKEN,MR}$	-0.3	–	5.5	V	–	P_4.9

General Product Characteristics

Table 2 Absolute Maximum Ratings¹⁾ (cont'd)

$T_j = -40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SDO, RST, VROUT, LINRX, CANRX	$V_{\text{SDO,MR}}$	-0.3	–	V_{DDIO}	V	both conditions must be observed	P_4.31
	$V_{\text{RST,MR}}$			+0.3			
	$V_{\text{VROUT,MR}}$	-0.3	–	5.5	V		
	$V_{\text{LINRX,MR}}$						
	$V_{\text{CANRX,MR}}$						
MON, KOFFDO	$V_{\text{MON,MR}}$	-0.3	–	$V_{5V}+0.3$	V	both conditions must be observed	P_4.10
	$V_{\text{KOFFDO,MR}}$			3			
		-0.3	–	5.5	V		
VRIN1	$V_{\text{VRIN1,MR}}$	-0.3	–	40	V	VRIN2 open	P_4.11
VRIN2	$V_{\text{VRIN2,MR}}$	-0.3	–	40	V	VRIN1 open	P_4.12
LINIO, CANH, CANL	$V_{\text{LINIO,MR}}$	-40	–	40	V	–	P_4.13
	$V_{\text{CANH,MR}}$						
	$V_{\text{CANL,MR}}$						
OUT21...24	$V_{\text{OUT21...24,MR}}$	-0.3	–	BATPx+0.3	V	–	P_4.14

Currents

DFB8...13	$I_{\text{DFB8...13,MR}}$	-5	–	5	mA	²⁾	P_4.15
Common Mode Input Current of VRIN1 and VRIN2	$I_{\text{VRIN,CM,MR}}$	-5	–	5	mA	$I_{\text{VRIN,CM,MR}} = I_{\text{VRIN1}} + I_{\text{VRIN2}}$ ²⁾	P_4.16
Common Mode Input Current of VRIN1 and VRIN2, non permanent	$I_{\text{VRIN,CM,MR}}$	-15	–	15	mA	$I_{\text{VRIN,CM,MR}} = I_{\text{VRIN1}} + I_{\text{VRIN2}}$ ²⁾ , maximum duty cycle 60% and maximum on time of 1ms, 100h	P_4.34
Differential Current of VRIN1 and VRIN2	$\Delta I_{\text{VRIN,MR}}$	-50	–	50	mA	$\Delta I_{\text{VRIN,MR}} = (I_{\text{VRIN1}} - I_{\text{VRIN2}})^2$ ²⁾	P_4.17
PGND	$I_{\text{PGND,MR}}$	-25	–	25	A	–	P_4.18
IGN1...4	$I_{\text{IGN1...4,MR}}$	-50	–	–	mA	²⁾	P_4.19

Temperatures

Junction Temperature	T_j	-40	–	150	$^\circ\text{C}$	³⁾	P_4.20
Storage Temperature	T_{stg}	-55	–	150	$^\circ\text{C}$	–	P_4.21

ESD Susceptibility

ESD Susceptibility	V_{ESDHBM}	-2	–	2	kV	HBM ⁴⁾	P_4.22
ESD Susceptibility BAT, BATPA, BATPB, T5V1, T5V2, BATSTBY, KEY, WK, MR, OUT1...7, OUT14...24, DFB8...13, IGN1...4, CANH, CANL, LINIO, VRIN1, VRIN2 to PGND	$V_{\text{ESD,HBM}}$	-4	–	4	kV	HBM ⁴⁾	P_4.23

General Product Characteristics

Table 2 Absolute Maximum Ratings¹⁾ (cont'd)

$T_j = -40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ESD Susceptibility	V_{ESDCDM}	-500	–	500	V	CDM ⁵⁾	P_4.24
ESD Susceptibility Pin 1, 25, 26, 50, 51, 75, 76, and 100 (corner pins)	$V_{\text{ESD1, 25, 26, 50, 51, 75, 76, 100}}$	-750	–	750	V	CDM ⁵⁾	P_4.25

- 1) not subject to production test
- 2) Current has to be limited when maximum voltages are exceeded
- 3) according to qualification
- 4) ESD susceptibility, HBM according to EIA/JESD 22-A114F (1.5k Ω , 100pF)
- 5) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Table 3 Functional Range

$T_j = -40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage - Reduced Operation	$V_{\text{BAT,ro}}$	4.5	–	6	V	reduced operation range, main relay and delayed off power stages are on if enabled, remaining functions not working	P_4.26
Supply Voltage - Low Drop Range	$V_{\text{BAT,ld}}$	6	–	9	V	low drop operation range, supply regulators working with supply out of the charge pump, standby supply regulator out of operation range	P_4.27
Supply Voltage - Normal Operation range	$V_{\text{BAT,nop}}$	9	–	28	V	normal operation range ¹⁾	P_4.28

General Product Characteristics

Table 3 Functional Range (cont'd)

$T_j = -40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage - Over Voltage Range	$V_{\text{BAT,ov}}$	28	–	40	V	over voltage, power stages are switched off	P_4.29
Supply Voltage transients ²⁾	d_{VBAT}/d_t	-1	–	1	V/ μs	–	P_4.30

1) over temperature due to bad R_{thJA} of the ECU or overload can happen

2) not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case ¹⁾	R_{thJC}	–	2.4	–	K/W	–	P_4.32
Junction to Ambient	R_{thJA}	–	–	–	K/W	²⁾	P_4.33

1) Not subject to production test, specified by design.

2) EIA/JESD 52_2, FR4, $80 \times 80 \times 1.5$ mm; $35 \times \text{Cu}$, $5 \times \text{Sn}$; 300 mm^2

5 Operation Behavior

The TLE8888-1QK has implemented the whole supply of an ECU. Therefore a complex control logic is implemented to provide several operation states.

In this chapter

- the ramp up and down behavior and
- the status of the TLE8888-1QK during special conditions like 5V undervoltage

is described. For the description of the monitoring watchdog module see [Chapter 6](#).

In [Figure 3](#) the block diagram with all blocks affecting the status of the device and the ECU are shown. Following blocks are influenced during the different operation states and reset functions:

- **Serial Interface MSC/SPI:** with the serial interface the setup of the device is done
- **Key input detection:** start signal from key switch (KL15)
- **Wake up input detection:** additional start signal e.g. from external CAN with wake up by bus function
- **Engine off timer:** wake up signal in comparator mode
- **Power supply:** ECU 5V supply and 5V sensor supplies, 5V standby supply
- **Voltage monitoring:** supervision of all supplies (BAT, V5V, T5V1, T5V2)
- **Main relay driver:** controls external main relay to switch battery voltage to an ECU supply pin (see also application setups in [Chapter 17](#))
- **Power stages and half-bridges control block**
- **LIN/K-Line:** transmission mode depends on operation state of the ECU
- **CAN:** transmission mode depends on operation state of the ECU, remote wake up function
- **Reset outputs MON and RST**
- **Monitoring watchdog module:** signature watchdog for safety applications
- **Operation Mode Control**

The operation mode control block consists of:

- ramp up and down sequence control logic
- the reset control logic and
- status output logic.

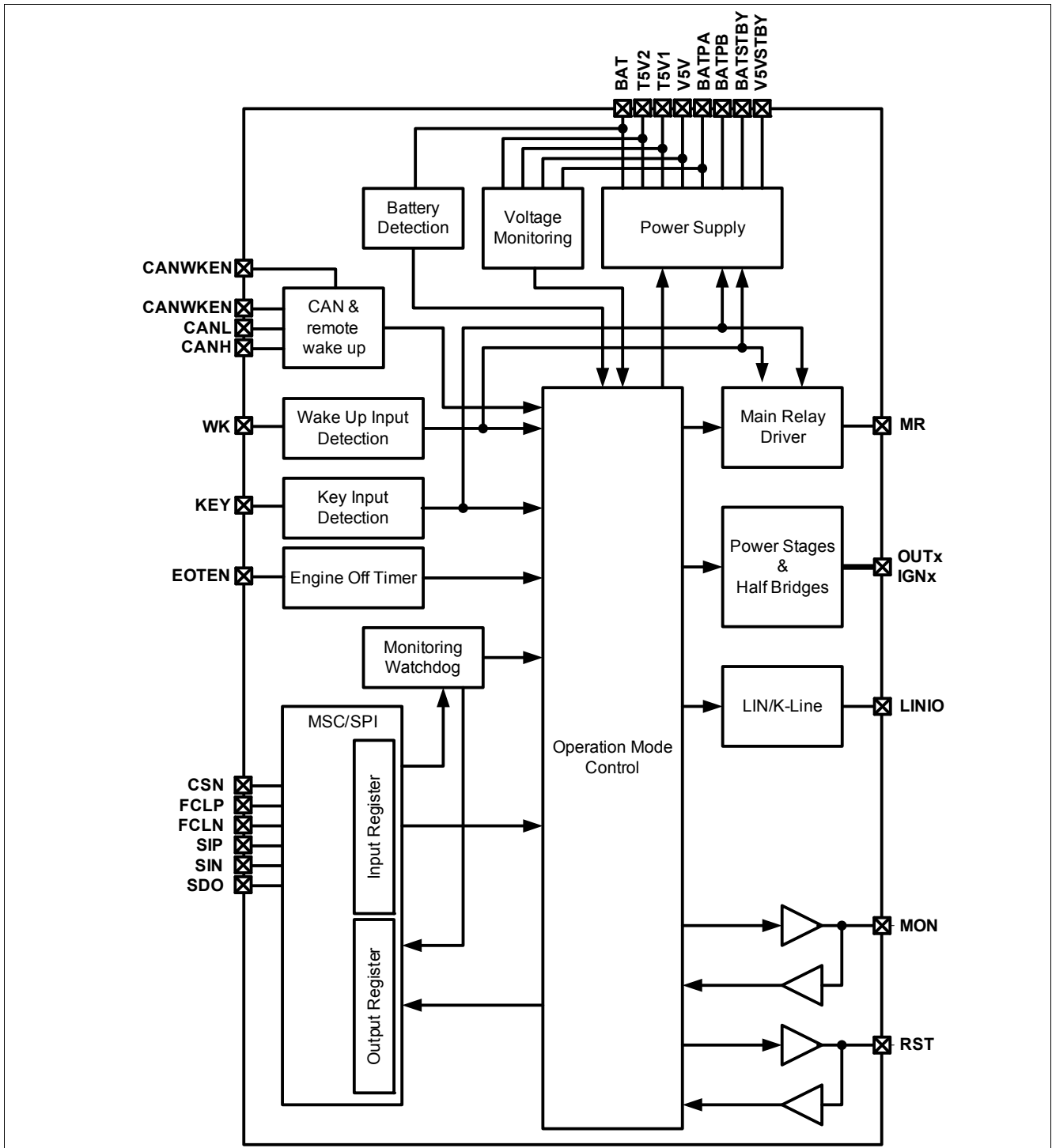


Figure 3 Block diagram operation mode control

5.1 Operation States

In **Figure 4** the state diagram of the whole ramp up and down sequence is shown. There are seven operation states:

- **ECU sleep state:** *KEY* and *WK* input are “low”, no wake up signals from engine off timer or CAN are active, main relay is off, the whole ECU inclusive TLE8888-1QK is not supplied, 5V standby supply is working if pin *BATSTBY* is supplied, engine off timer and CAN wake up circuits are active if enabled and supplied.

- **Supply ramp up state:** *KEY* input or *wake*¹⁾ are “high” and the supply of the TLE8888-1QK starts working, the voltage of V6V, V5V, T5V1 and T5V2 are ramping up but the voltage levels are below the under voltage threshold. For wake up by *wake*¹⁾ the ramp up of the main supply has to be finished before the ramp up timer overflow. The main relay is switched on depending on the voltage level at the pin *BAT* (see [Chapter 7.2](#))
- **Normal operation state:** *KEY* input or *wake* are “high” and main relay is switched on depending on the voltage level at the pin *BAT* or the status of bit **MR** in the status register **OpStat0** (see [Chapter 7.2](#)), the whole ECU is supplied and the status of the different functions and registers is according [Table 6](#) and [Table 7](#).
- **Afterrun state:** *KEY* is “low” but afterrun enable bit is set and therefore the whole ECU is supplied, the status of the different functions and registers is according [Table 6](#) and [Table 7](#) and the micro controller can execute afterrun routines
- **Afterrun reset state:** the reset procedure before direct reentry in normal operation is executed if bit **AR** =1 in the configuration register **OpConfig0**
- **General power down state:** the supplies of the ECU (*V5V*, *T5V1*, *T5V2*) are disabled and the power down timer is counting, main relay remains in the switching status and the TLE8888-1QK is supplied to ensure the power down (V5V drops down to 0V) of the ECU, *V5VSTBY* is working if *BATSTBY* is supplied, all functions to external are disabled.
- **Wake clear state:** this state avoids permanent wake up in failure cases. The wake clear command is executed (function according setting bit **WKCLR** in the command register **Cmd0**). All wake signals which are active after the supply ramp up and the general power down state are reset.

1) description see [Figure 4](#), [Chapter 7.2](#), [Chapter 7.4](#) and [Chapter 12.2.4](#)

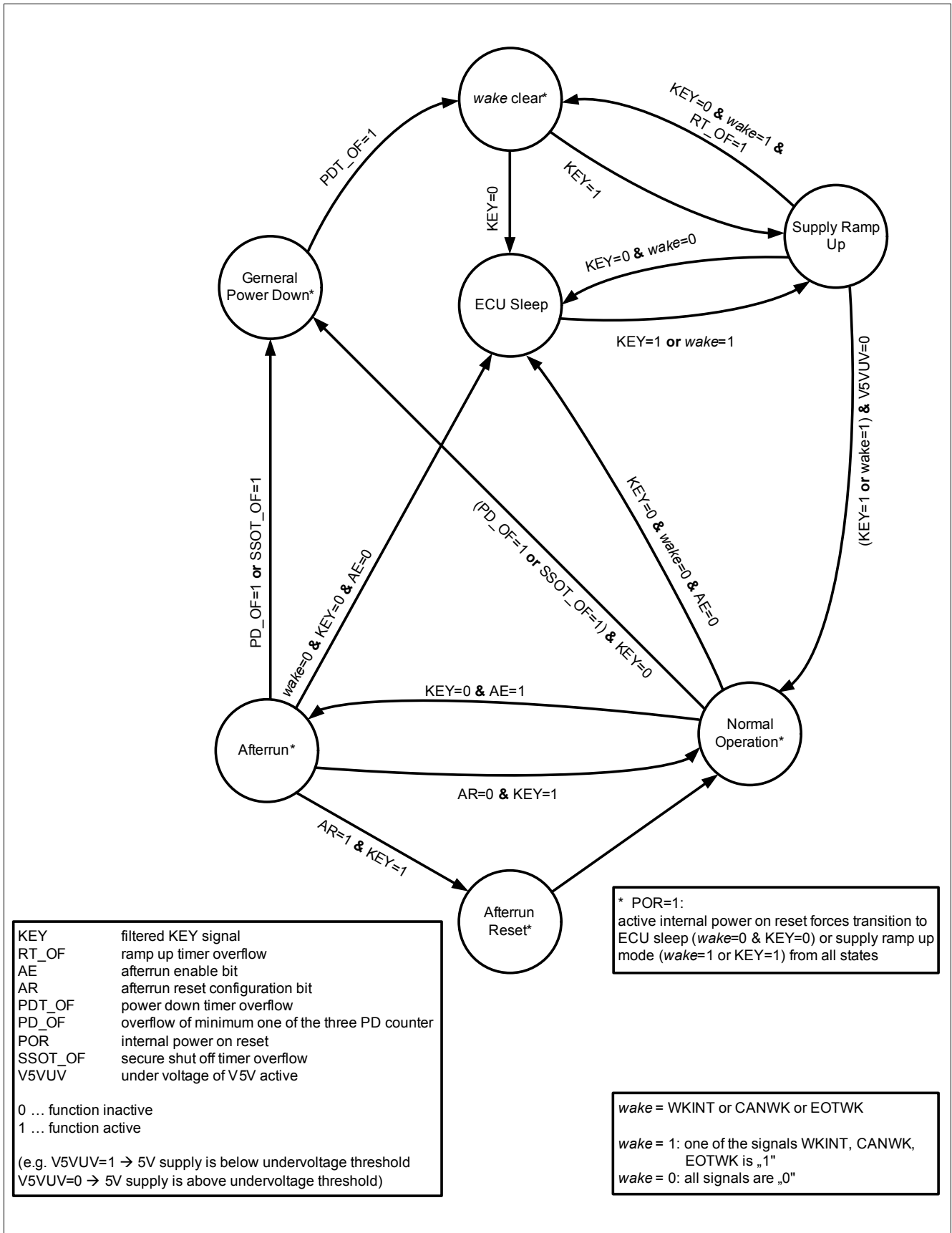


Figure 4 Operation state diagram

Description of the transitions:

Table 5 Operation State Transitions

Transition	Condition	Description
from all states to ECU sleep state	internal supply voltage < internal por threshold and $KEY=0$ and $wake^1)=0^2)$	internal power on reset is active and reset the whole digital logic, ECU sleep state is entered due to no wake up signal at KEY or $wake$
from all states to supply ramp up state	internal supply voltage < internal por threshold and $KEY=1$ or $wake=1^2)$	internal power on reset is active and reset the whole digital logic, supply ramp up state is entered due to a wake up signal at KEY or $wake$
ECU sleep state to supply ramp up state	$KEY > V_{KEY,th}$ or $wake=1$	With a "high" voltage at KEY or $wake$ the wake up of the TLE8888-1QK starts
Supply ramp up state to ECU sleep state	$KEY < V_{KEY,th}$ and $wake=0^2)$	The external supply ramp up is not finished but the wake up signals are low
Supply ramp up state to wake clear state	$KEY < V_{KEY,th}$ and $wake=1^2)$ and $RT_OF=1$	The KEY signal is low and the wake up signals are active. The ramp up timer has an overflow which indicates a ramp up problem of the external supply (e.g. short to GND). To avoid permanent high current consumption the internal wake signals must be reset to enter the ECU sleep state.
Supply ramp up state to normal operation state	$(KEY > V_{KEY,th}$ or $wake=1)$ and $V5V > V_{uv,V5V}^2)$	normal operation state is entered if the main supply voltage $V5V$ is above the under voltage threshold, KEY is high or one of the wake up conditions are active
Normal operation state to afterrun state	$KEY < V_{KEY,th}$ and $AE=1^2)$	KEY is "low" and afterrun function is enabled: no changes in the setup of the TLE8888-1QK
Normal operation state to ECU sleep state	$AE=0$ and $KEY < V_{KEY,th}$ and $wake=0^2)$	normal shut off
Normal operation state to general power down state	$(PD_OF=1$ or $SSOT_OF=1)$ and $KEY < V_{KEY,th}^2)$	KEY is low and watchdog error shut off with overflow of the power down counter or secure shut off due to expired secure shut off timer
Afterrun state to ECU sleep state	$AE=0$ and $KEY < V_{KEY,th}$ and $wake=0^2)$	normal shut off in afterrun mode with the reset of the afterrun enable bit AE by the micro controller
Afterrun state to general power down state	$PD_OF=1$ or $SSOT_OF=1$	watchdog error shut off with overflow of the power down counter or secure shut off due to expired secure shut off timer
Afterrun state to normal operation state	$KEY > V_{KEY,th}$ and $AR=0^2)$	reentry of normal operation with KEY on during afterrun operation, no reset is performed ($AR=0$)
Afterrun state to afterrun reset state	$KEY > V_{KEY,th}$ and $AR=1^2)$	reentry of normal operation with KEY on during afterrun operation with reset ($AR=1$)
Afterrun reset state to normal operation state		transition to normal operation with the next active internal clock edge after entry to the afterrun reset state
General power down state to wake clear state	$PDT_OF=1$	with the power down timer overflow the reset of the internal wake signals must be performed

Table 5 Operation State Transitions (cont'd)

Transition	Condition	Description
Wake clear state to ECU sleep state	$KEY < V_{KEY,th}$	after reset of the internal wake signals and <i>KEY</i> is low the ECU sleep state is entered, no unwanted wake up due to a failure condition will occur
Wake clear state to supply ramp up state	$KEY > V_{KEY,th}$	after reset of the internal wake signals and <i>KEY</i> is high the supply ramp up state is entered, no unwanted wake up due to a failure condition at the CAN bus and pin <i>WK</i> will occur

1) *wake* = WKINT or CANWK or EOTWK (see [Chapter 7.2](#), [Chapter 7.4](#) and [Chapter 12.2.4](#))

2) including defined filter times

The two states:

- normal operation
- afterrun

are reflected in the bit **OM** of the status register **OpStat0**.

The power down time is defined with the bits **PDT** of the configuration register **OpConfig0**.

In [Figure 5](#) a sequence with wake up by *KEY* and go to sleep with afterrun mode is shown.

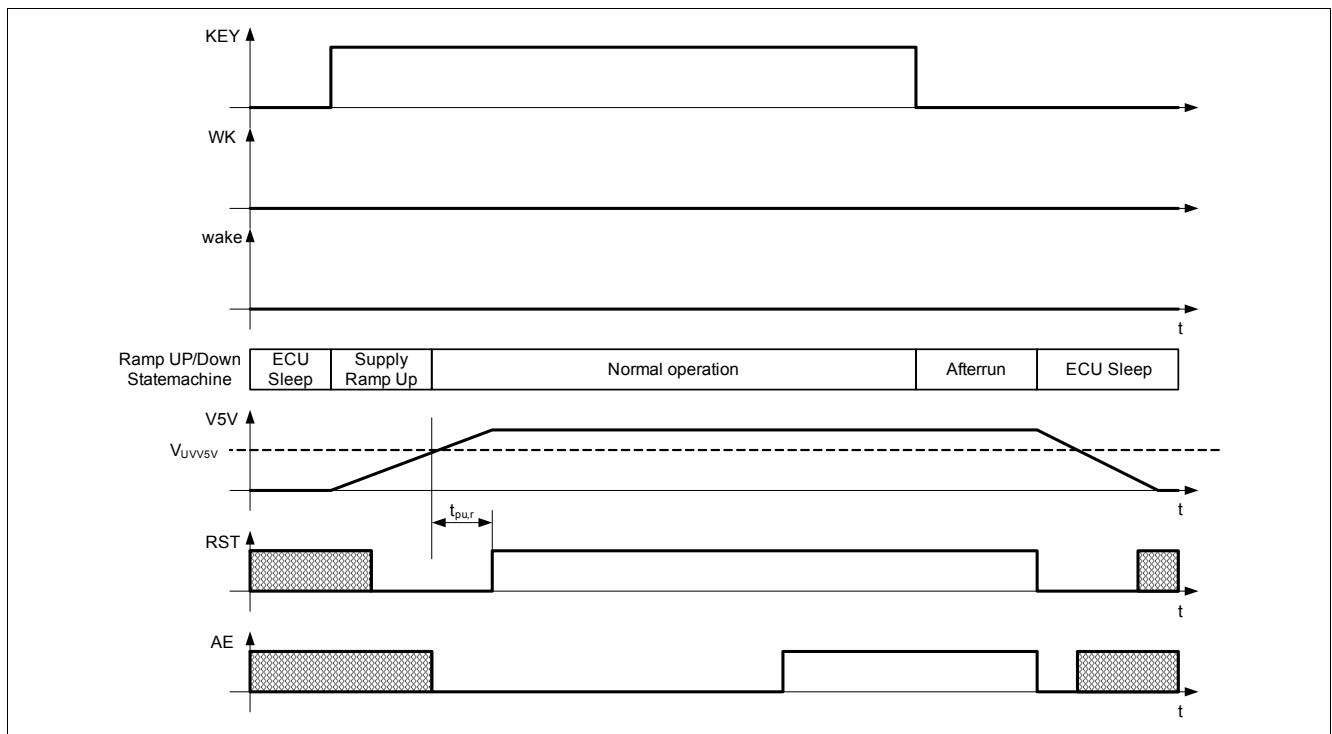


Figure 5 Ramp up and down sequence diagram with wake up by *KEY* and afterrun mode

5.2 Reset and Operation Modes

The TLE8888-1QK provides several supervision functions which lead to some dedicated reset states and special operation modes of the device and the ECU.

There are two bidirectional reset pins MON and RST implemented. For the behavior during reset of the reset pins MON and RST and the other status of the TLE8888-1QK see [Table 6](#) and [Table 7](#).

Following reset functions and special states are implemented:

- **Internal power on reset:** the internal power on reset detection circuit monitors the voltage level of the internal supply. For an internal supply voltage below the internal power on reset threshold the whole digital logic of the TLE8888-1QK is reset which results in the ECU sleep state or supply ramp up state depending on the state of *KEY* and *wake*. If the voltage level for operation is high enough the 6V pre regulator is working. The 5V supplies are disabled till the internal supply level is over the power on threshold level.
- **ECU power on reset:** this is the reset at ramp up of the power supplies and the beginning of the operation. The pins *RST* and *MON* are pulled to GND to reset the micro controller and all devices connected to the pin *MON*. The device is reset to the initial reset status. The reset is released with a voltage at pin *V5V* higher than the **V5V Under Voltage Detection Hysteresis** after $t_{pu,r}$.
- **Reset during under voltage of the 5V supply V5V:** this reset occurs during under voltage of the 5V ECU supply. The pins *RST* and *MON* are pulled to GND to reset the micro controller and all devices connected to the pin *MON*. The delayed switch off function is active regarding the configuration setup. The status of the main relay is according to the status of the wake up pins *KEY* and *WK* and the voltage level of the supply pin *BAT*.
- **State during under voltage of the 5V supplies T5V1 and T5V2:** with the under voltage detection of the tracker supplies diagnosis bits are set but there is no effect to the behavior of the device.
- **Reset during over voltage of the 5V supply V5V:** with the over voltage detection of the 5V ECU supply all functions of the device which have an effect externally or can lead to over current or over temperature are disabled (e.g. power stages, LIN/CAN/MSB/SPI communication). The pins *RST* and *MON* are low.
- **State during over voltage of the 5V supplies T5V1 and T5V2:** with the detection of over voltage of the tracker supplies diagnosis bits are set but there is no effect to the behavior of the device.
- **Power stages switch off during over voltage of the battery supply BAT:** For voltages at the supply pin *BAT* higher than the over voltage threshold the power stages are disabled to avoid too high clamping energy during switch off. Damage of the switches is prevented.
- **Watchdog reset:** If the reset counter is incremented and the reset is enabled (bit **WDREN** = 1) the micro controller is reset with a "low" at the pin *RST*. The power stages are disabled and the LIN/CAN communication is set to receive only mode.
- **Software reset from micro controller:** with the software reset command (command register **CmdSR**) the software reset is activated. The device is reset to the reset status defined in **Table 6** and **Table 7**. The activation of the software reset triggers an increase of the power down counter by 1.
- **Reset with an external forced "low" at RST:** With a detected "low" at the *RST* pin the TLE8888-1QK is reset to the reset status defined in **Table 6** and **Table 7**.
- **Power stages switch off with an external forced "low" at MON:** With a detected "low" at the *MON* pin the power stages are disabled (**O1E** to **O24E**, **IGN1E** to **IGN4E** are set to "0"). After *MON*=0 event the power stages must be enabled again.
- **State with time out of the MSC communication:** With the time out of the MSC communication the power stages are disabled (**O1E** to **O24E**, **IGN1E** to **IGN4E** are set to "0"). After the next valid received data frame the power stages must be enabled again.
- **Afterrun reset:** This reset is executed if the bit **AR** of register **OpConfig0** is 1 and the transition from afterrun state to normal operation is triggered (definition see **Table 7**).

Table 6 Overview Behavior at Reset and Operation Conditions (part 1)

Effect to functions:	Conditions						
	Internal power on reset	ECU power on reset	Under voltage V5V	Undervoltage T5V1, T5V2	Over voltage V5V ¹⁾	Over voltage T5V1, T5V2	Over voltage BAT
notes	forces state change	only after transition from Supply Ramp Up to Normal Operation state for $t_{pu,r}$	timing see Chapter 8.7 and Table 8	timing see Chapter 8.7	timing see Chapter 8.7 and Table 8	timing see Chapter 8.7	timing see Chapter 8.7
<i>V5VSTBY, V6V</i>	en.	en.	en.	en.	en.	en.	en.
<i>V5V, T5V1, T5V2</i>	dis.	en.	en.	en.	en.	en.	en.
MSC/SPI communication	dis.	dis.	dis.	en.	dis.	en.	en.
Main relay	en. ²⁾	en. ²⁾	en. ²⁾	en. ²⁾	en. ²⁾	en. ²⁾	en. ²⁾
Low Side switches / Half bridges / Push Pull Driver	off/dis./off	off/dis./off	off/dis./off	no change	off/dis./off	no change	off/dis./off
<i>OUT17</i> and <i>OUT21</i> with delayed switch off function	dis.	dis.	delayed switch off activated	en.	delayed switch off activated	en.	dis.
LIN/CAN communication	dis.	rec. only, after release setup acc. bits CAN , LIN , CANWE , LINWE ³⁾	rec. only, after release setup acc. bits CAN , LIN , CANWE , LINWE ³⁾	acc. bits CAN , LIN , CANWE , LINWE	dis., after release setup acc. bits CAN , LIN , CANWE , LINWE	acc. bits CAN , LIN , CANWE , LINWE	acc. bits CAN , LIN , CANWE , LINWE
MON (output function)	"low" ⁴⁾	"low"	"low"	no effect ⁵⁾	"low"	no effect ⁵⁾	no effect ⁵⁾
RST (output function)	"low" ⁴⁾	"low"	"low"	no effect ⁵⁾	"low"	no effect ⁵⁾	no effect ⁵⁾
Watchdog Sequence, Heartbeat Timer ⁶⁾	reset	reset	reset	no effect	reset	no effect	no effect
WWD Error Counter, FWD pass counter, Total error counter	reset	reset	reset	no effect	reset	no effect	no effect
PD Counter	reset	reset	reset	no effect	reset	no effect	no effect
Reset Counter; SSOT	reset	reset	reset	no effect	reset	no effect	no effect
AR ; CANWE ; LINWE ; FWDQUEST	reset	reset	reset	no effect	reset	no effect	no effect
AE ; WWDConfig0 ; WDCConfig0 ; watchdog diagnosis bits	reset	reset	reset	no effect	reset	no effect	no effect

Table 6 Overview Behavior at Reset and Operation Conditions (part 1) (cont'd)

Effect to functions:	Conditions						
	Internal power on reset	ECU power on reset	Under voltage V5V	Undervoltage T5V1, T5V2	Over voltage V5V ¹⁾	Over voltage T5V1, T5V2	Over voltage BAT
Logic and MSC/SPI register bits ⁷⁾⁸⁾	reset	reset	reset, diagnosis bit is set	diagnosis bits are set	no effect	diagnosis bits are set	diagnosis bit is set
EOTWK, CANWK, WKINT	no effect	no effect	reset	no effect	no effect	no effect	no effect

- 1) for voltages greater than the maximum ratings of pin $V5V$ behavior is not guaranteed
- 2) according the definition in [Chapter 7](#)
- 3) after release of RST (transition from low to high) there is a time delay of $t_{del,r}$ before configuration is enabled
- 4) active pull down if supply voltage is high enough
- 5) pull up of open drain output is active
- 6) start of watchdog sequence after release of reset
- 7) valid for all register bits which are not described in [Table 6](#) or [Table 7](#)
- 8) During active delayed switch off mode some register bits related to the power stages are not reset, see [Chapter 9.4](#)

Table 7 Overview Behavior at Reset and Operation Conditions (part 2)

Effect to functions:	Conditions							
	Watchdog reset	Safe State	SW reset from micro controller	MON switch off (input function)	RST reset (input function)	MSC time out	afterrun reset	
							no reset AR=0	reset AR=1
note	status during reset pulse $t_{op,r}$		status during reset pulse $t_{int,r}$	masked by MON output function	masked by RST output function	status till next valid MSC communication		
<i>V5VSTBY, V6V</i>	en.	en.	en.	en.	en.	en.	en.	en.
<i>V5V, T5V1, T5V2</i>	en.	en.	en.	en.	en.	en.	en.	en.
MSC/SPI communication	dis.	en.	en.	en.	dis.	en.	en.	dis.
Main relay	en. ¹⁾	en.	en. ¹⁾	en. ¹⁾	en. ¹⁾	en. ¹⁾	en. ¹⁾	en. ¹⁾
Low Side switches / Half bridges / Push Pull Driver	off/dis./off	off/dis./off	off/dis./off ³⁾	off/dis./off	off/dis./off	off/dis./off	no change	off/dis./off
<i>OUT17</i> and <i>OUT21</i> with delayed switch off function	no trigger if termination of delayed switch off function	no trigger if termination of delayed switch off function	dis. ³⁾	delayed switch off activated	delayed switch off activated	delayed switch off activated	en.	dis.
LIN/CAN communication	acc. bits CAN, LIN, CANWE, LINWE	acc. bits CAN, LIN, CANWE, LINWE	acc. bits CAN, LIN, CANWE, LINWE	acc. bits CAN, LIN, CANWE, LINWE	rec. only, after release setup acc. bits CAN, LIN, CANWE, LINWE ²⁾	acc. bits CAN, LIN, CANWE, LINWE	acc. bits CAN, LIN, CANWE, LINWE	rec. only, after release setup acc. bits CAN, LIN, CANWE, LINWE ²⁾
MON	“low”	“low”	“low” ³⁾	forced from outside	“low”	no effect ⁴⁾	no effect ⁴⁾	“low”
RST	“low”	no effect ⁴⁾	no effect ⁴⁾	no effect ⁴⁾	forced from outside	no effect ⁴⁾	no effect ⁴⁾	“low”

Table 7 Overview Behavior at Reset and Operation Conditions (part 2) (cont'd)

Effect to functions:	Conditions							
	Watchdog reset	Safe State	SW reset from micro controller	MON switch off (input function)	RST reset (input function)	MSC time out	afterrun reset	
							no reset AR=0	reset AR=1
Watchdog Sequence, Heartbeat Timer ⁵⁾	reset	no effect	reset	no effect	reset	no effect	no effect	reset
WWD Error Counter, FWD pass counter, Total error counter	reset	no effect	reset	no effect	reset	no effect	no effect	reset
PD Counter	no effect	no effect	increment +1	no effect	no effect	no effect	no effect	no effect
Reset Counter; SSOT	no effect	no effect	no effect	no effect	no effect	no effect	no effect ⁶⁾	no effect ⁶⁾
AR; CANWE; LINWE; FWDQUEST	no effect	no effect	no effect	no effect	no effect	no effect	no effect	no effect
AE; WWDConfig0; WDConfig0 ; watchdog diagnosis bit	reset	no effect	reset	no effect	reset	no effect	no effect	reset
Logic and MSC/SPI register bits ⁷⁾⁸⁾	no effect	no effect	reset	no effect	reset	diagnosis bit is set	no effect	reset
EOTWK, CANWK, WKINT	no effect	no effect	no effect	no effect	no effect	no effect	no effect	no effect

1) according the definition in [Chapter 7](#)

2) after release of RST (transition from low to high) there is a time delay of $t_{del,r}$ before configuration is enabled

3) status for time $t_{op,r}$

4) pull up of open drain output is active

5) start of watchdog sequence after release of reset

6) SSOT reset due to $KEY=1$

7) valid for all register bits which are not described in [Table 6](#) or [Table 7](#)

8) During active delayed switch off mode some register bits related to the power stages are not reset, see [Chapter 9.4](#)

Table 8 Reset Time Definition

Reset Function		Reset Time at RST Output	Related Status Bits in Register OpStat1
internal power on reset			all registers are reset
ECU power on reset		$t_{pu,r}$	
Under voltage V5V		$t_{pu,r}$	V5VUVR
Over voltage V5V		$t_{pu,r}$	V5VOVR
Watchdog reset		$t_{op,r}$	WDRES
RST reset forced from outside		forced from outside	RSTR
Software reset from micro controller		no effect	all registers are reset ¹⁾
Afterrun reset	AR="0"	no effect	
	AR="1"	$t_{op,r}$	ARES

1) internal reset with $t_{int,r}$ active

After a reset with pin *RST* the configuration of the CAN and LIN bus is delayed by the time $t_{del,r}$ to avoid that undefined micro controller pins are affecting the buses. During this delay time the configuration bits can be changed by a write access to the register.

5.3 Electrical Characteristics Operation Behavior

Table 9 Electrical Characteristics: Operation Behavior
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Internal power on reset threshold	$V_{por,int,th}$	–	–	2.8	V	of internal supply voltage	P_5.3.1
Supply voltage range for internal supply	$V_{BATP,int}$	4.5	–	–	V	only valid if the charge pump has ramped up before voltage drop, both condition must be fulfilled to ensure no internal power on reset	P_5.3.2
	$V_{V6V,int}$	3.5	–	–	V		

Power Down Timer

Power down time 1	$t_{pd,1}$	–	100	–	ms	–	P_5.3.3
Power down time 2	$t_{pd,2}$	–	200	–	ms	–	P_5.3.4
Power down time 3	$t_{pd,3}$	–	300	–	ms	–	P_5.3.5
Power down time 4	$t_{pd,4}$	–	400	–	ms	–	P_5.3.6
Power down time accuracy	$t_{pd,a}$	-10	–	+10	%	–	P_5.3.7

Ramp Up timer

Ramp up time	t_{ru}	185	–	650	ms	–	P_5.3.8
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MON In- Output

Input low level	V_{il}	–	–	$0.29 \cdot V_{5V}$	V	–	P_5.3.10
Input high level	V_{ih}	$0.7 \cdot V_{5V}$	–	–	V	–	P_5.3.11
Input hysteresis	V_{ihys}	0.1	–	1	V	–	P_5.3.12
Pull up current	I_{imax}	-100	–	–	μA	$V_{in}=0V$, pull up to V_{5V}	P_5.3.13
Input de-glitch time for low and high level detection	$t_{i,d}$	0.5	–	3.5	μs	–	P_5.3.14
Output low level operation	V_{ol}	–	–	0.7	V	$I_{out}=2mA$; $V_{V5V}=2.5V$	P_5.3.15
Output current capability	I_{omax}	15 ¹⁾	–	–	mA	$V_{MON}=5V$	P_5.3.16

RST In- Output

Input low level	V_{il}	–	–	$0.29 \cdot V_{DDIO}$	V	–	P_5.3.17
Input high level	V_{ih}	$0.7 \cdot V_{DDIO}$	–	–	V	–	P_5.3.18
Input hysteresis	V_{ihys}	0.1	–	1	V	–	P_5.3.19

Table 9 Electrical Characteristics: Operation Behavior (cont'd)

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull up current	I_{imax}	-100	–	–	μA	$V_{in}=0V$, pull up to $VDDIO$	P_5.3.20
Input de-glitch time for low and high level detection	$t_{i,d}$	0.5	–	3.5	μs	–	P_5.3.21
Output low level operation	V_{ol}	–	–	0.7	V	$I_{out}=2mA$; $V_{V5V}=2.5V$	P_5.3.22
Output current capability	I_{omax}	15 ¹⁾	–	–	mA	$V_{RST}=5V$	P_5.3.23
Reset Times							
Power up reset time	$t_{pu,r}$	12	16	20	ms	–	P_5.3.24
Operation reset time	$t_{op,r}$	1	2	4	ms	–	P_5.3.25
Internal reset time	$t_{int,r}$	–	–	1	μs	–	P_5.3.26
Delay time after reset	$t_{del,r}$	6	10	14	μs	–	P_5.3.27

1) Application must ensure that current into this pin does not exceed this value.

6 Monitoring Watchdog Module (Signature Watchdog)

The watchdog function is intended for a temporal and logical monitoring of the micro controller's program sequence. In **Figure 6** the block diagram of the monitoring module is drawn. The module has an interface to the MSC/SPI block. The monitoring of the micro controller is done by the separate check of the timing with the window watchdog and the logical operation check by the functional watchdog. Therefore the micro controller must send a window watchdog service command for the window watchdog and four response bytes for the functional check. The results of the checks affect the corresponding counter (window watchdog error counter or functional watchdog pass counter). Additionally a total error counter module is implemented which detects the occurrence of watchdog errors (the timing check or the functional is not passed) and changes the status of the total error counter accordingly.

For the independent functional watchdog and the total error counter a heartbeat is implemented to define the increment timing of both functions.

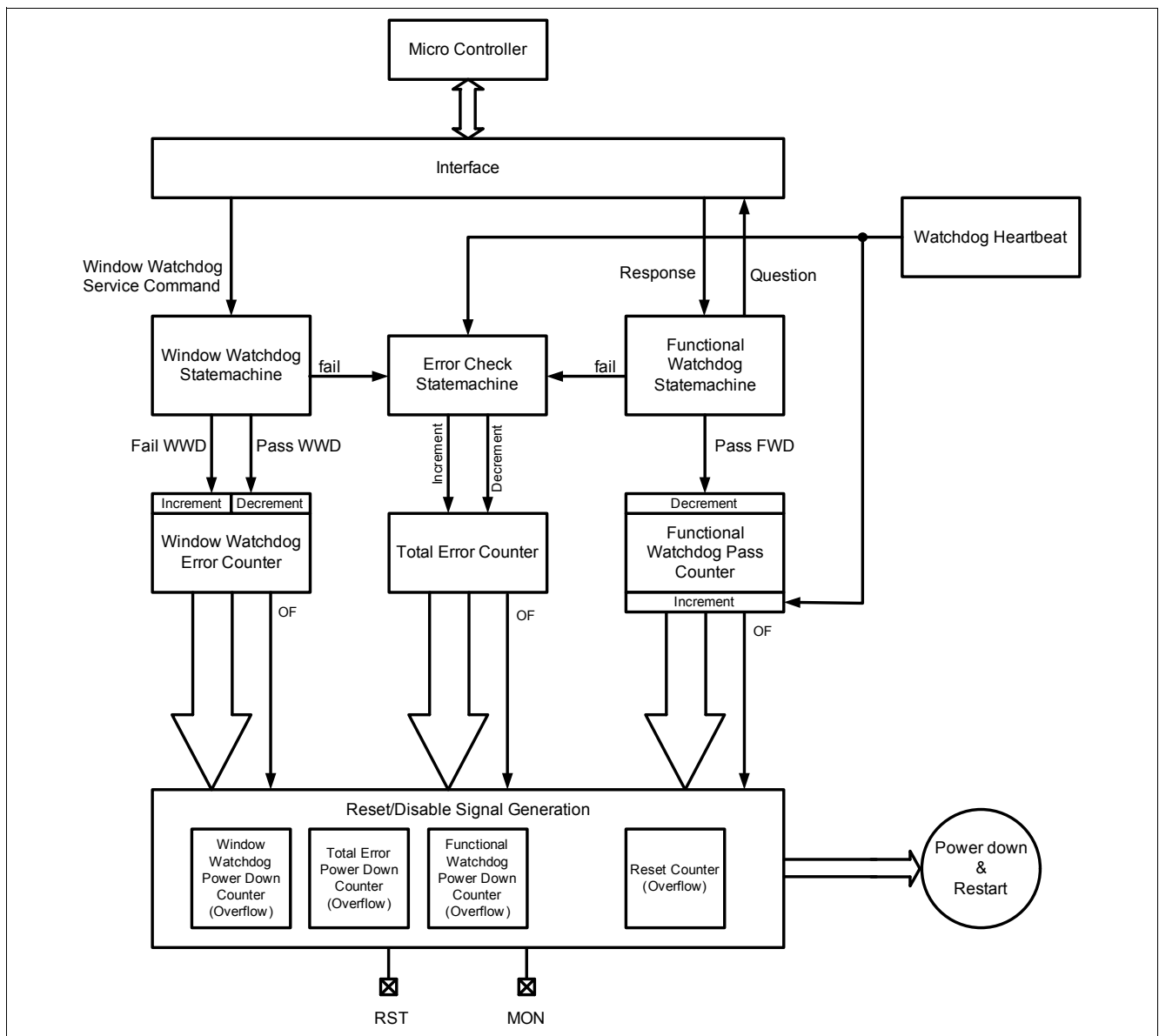


Figure 6 Block diagram of the Monitoring Watchdog Function

Monitoring Watchdog Module (Signature Watchdog)

The status of the counters (window watchdog error counter, functional watchdog pass counter and total error counter) and the corresponding overflow signals are inputs to the watchdog reset, power down counter and the secure shut off timer. This information is used to affect the operation status of the TLE8888-1QK and the status of the pins *MON* and *RST*.

The software of the micro controller has to make sure that the program sequence and any safety critical parts of the micro controller are self tested by performing related routines according to the received questions.

Table 10

Bit Name	Register	Type	Description
General			
WDRES	OpStat1	status	reset caused by watchdog (general status bit)
RESC	WdStat0	status	reset counter value
SSOTS	WdStat0	status	Secure shut off timer start status
WDHBTPRE	WDHBT0	status	heartbeat timer pre divider value
WDHBT	WDHBT1	status	heartbeat timer value
WDHBTP	WDConfig0	configuration	definition of heartbeat period for functional watchdog and total error counter
CANWE	WDConfig1	configuration	CAN operation mode during safe state
LINWE	WDConfig1	configuration	LIN operation mode during safe state
WDREN	WDConfig1	configuration	watchdog reset enable
FWDQG	WDConfig1	configuration	Functional watchdog question generation pattern setup
	MSCReadWd0	command	Multi read command for WdStat0 , TECStat , FWDStat0 , FWDStat1 , WdDiag , WWDStat , WDConfig0 and WWDCConfig0
	MSCReadWd1	command	Multi read command for WDHBT0 , WDHBT1 , WdStat0 and WdStat1
	WDHBTPSync Cmd	command	heartbeat period synchronization command
WDHBTS	Cmd0	command	watchdog heartbeat timer sample command
Window Watchdog			
WWDEC	WWDStat	status	value of error counter for window watchdog
WWDSER	WdStat0	status	Window watchdog service command received status
WWDPDC	WdStat0	status	power down counter value of window watchdog
WWDECI	WWDCConfig1	configuration	definition of the increment value of error counter for window watchdog
WWDECD	WWDCConfig1	configuration	definition of the decrement value of error counter for window watchdog
WWDCWT	WWDCConfig0	configuration	closed window time
WWDOWT	WWDCConfig0	configuration	open window time
	WWDSerServiceCmd	command	window watchdog service command
WWDSCE	WdDiag	diagnosis	window watchdog service command too early
WWDTO	WdDiag	diagnosis	window watchdog time out
WWDRES	WdDiag	diagnosis	reset caused by window watchdog

Monitoring Watchdog Module (Signature Watchdog)

Table 10 (cont'd)

Bit Name	Register	Type	Description
Functional Watchdog			
FWDQUEST	FWDStat1	status	question definition
FWDRESPC	FWDStat1	status	response counter
FWDPC	FWDStat0	status	pass counter value of functional watchdog
FWDPCD	WdStat1	status	power down counter value of functional watchdog
FWDPCI	FWDCConfig	configuration	definition of the increment value of pass counter for functional watchdog
FWDPCD	FWDCConfig	configuration	definition of the decrement value of pass counter for functional watchdog
FWDKQ	WDConfig1	configuration	Keep question function set up
	FWDRspCmd	command	response write command
	FWDRspSync Cmd	command	response write command with heartbeat synchronization at received response byte 0
FWDREA	WdDiag	diagnosis	response error of actual question
FWDREL	WdDiag	diagnosis	response error of last answer
FWDRES	WdDiag	diagnosis	reset caused by functional watchdog
Total Error Counter			
TEC	TECStat	status	total error counter value
TECPDC	WdStat1	status	power down counter value of total error counter part
TECI	TECConfig	configuration	definition of the increment value of total error counter
TECD	TECConfig	configuration	definition of the decrement value of total error counter
TECRES	WdDiag	diagnosis	reset caused by total error counter

6.1 Window Watchdog

For the timing check the micro controller has to send periodically the window watchdog service command **WWDServiceCmd**. The window watchdog is triggered correctly if the command is received inside the open window of the window watchdog sequence. The check result is used to change the value of the window watchdog error counter. If the check is passed the counter will be decremented and for errors it will be incremented. Additionally a write access to configuration register **WWDConfig0** causes also an incrementation of the window watchdog error counter. The incrementation of the window watchdog error counter (error is occurred) is an input for the total error counter (**Chapter 6.3**). In **Figure 7** the state machine of the window watchdog is shown. The values for incrementation or decrementation can be set in the configuration register **WWDConfig1**. The window watchdog error counter is a 6 bit counter. The influence of the counter values to the operation behavior is shown in **Table 12** and **Table 13**.

The window watchdog sequence for the timing check consists of a closed window followed by an open window (see **Figure 8**). A watchdog sequence starts with:

- the release of a reset of the monitoring module (see **Table 6** and **Table 7** in **Chapter 5.2**)
- a window watchdog service command
- a write to the window time configuration register **WWDConfig0**
- a timer overflow of the watchdog timer

In **Figure 8** the two parts of one watchdog sequence are shown. After the power on reset it is running in an endless loop with the defined time for the open and closed window. It is only stopped at active reset signals or outside

Monitoring Watchdog Module (Signature Watchdog)

normal operating conditions [Table 6](#) and [Table 7](#) in [Chapter 5.2](#).

The timing of the window watchdog sequence can be set with a write command to the configuration register [WWDConfig0](#) or directly with the data bits of the [WWDServiceCmd](#). With a write access to the configuration register [WWDConfig0](#) the watchdog window sequence is started and the window watchdog error counter is incremented.

The check is passed if the command is received inside the open window. A command send too early or a missing command leads to an error. In the diagnosis register [WdDiag](#) the bit [WWDSCCE](#) signalizes a window watchdog service command received too early and the bit [WWDTO](#) signalizes a time out (no window watchdog service command received before end of open window) of the last sequence. The diagnosis information is not cleared with the read out.

The bit [WWDSCR](#) in the status register [WdStat0](#) signalizes a received window watchdog service command at the last watchdog sequence. The reset of this bit is done with a readout of the bit or with the window watchdog time-out.

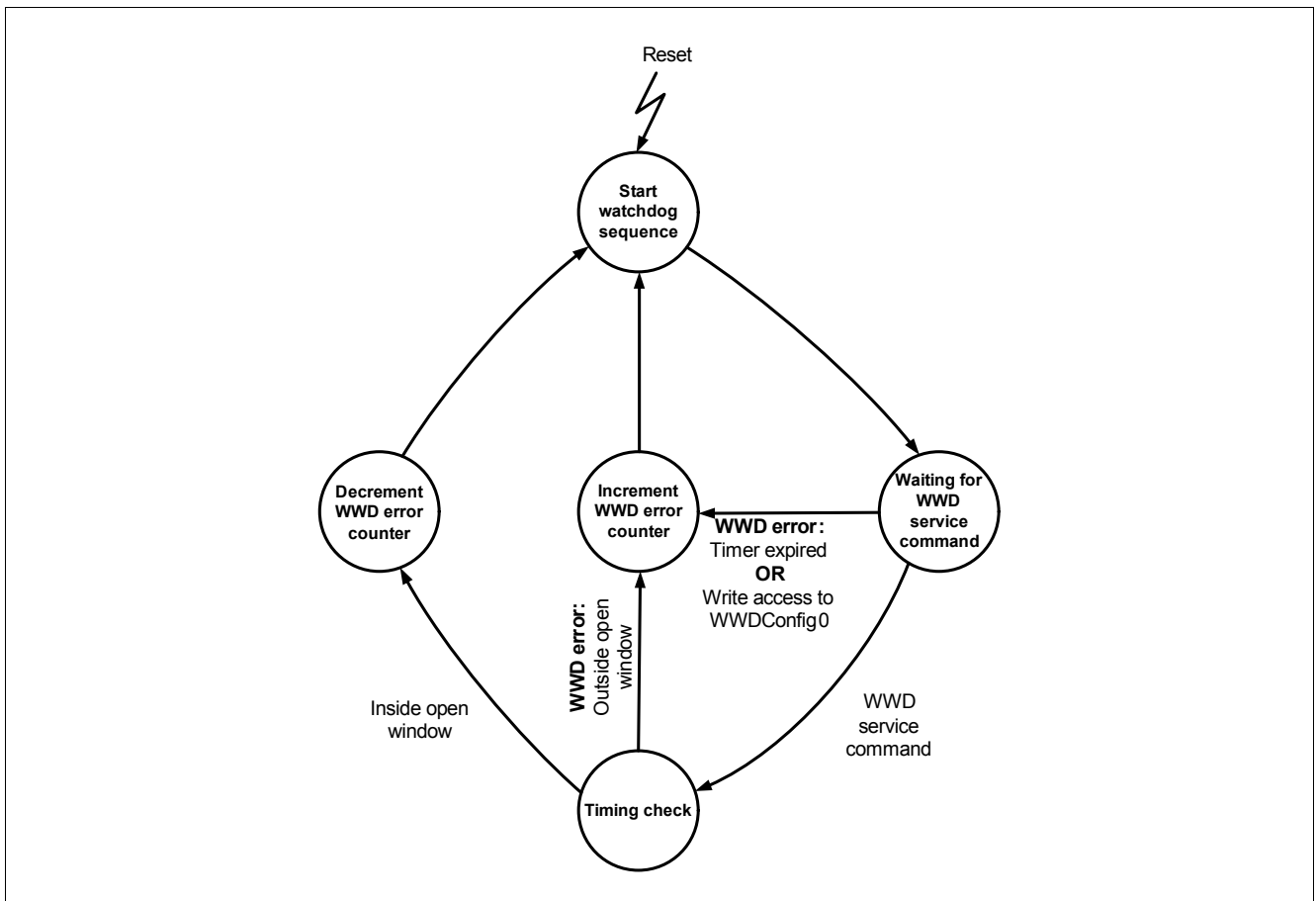


Figure 7 State Diagram of the Window Watchdog Module

Monitoring Watchdog Module (Signature Watchdog)

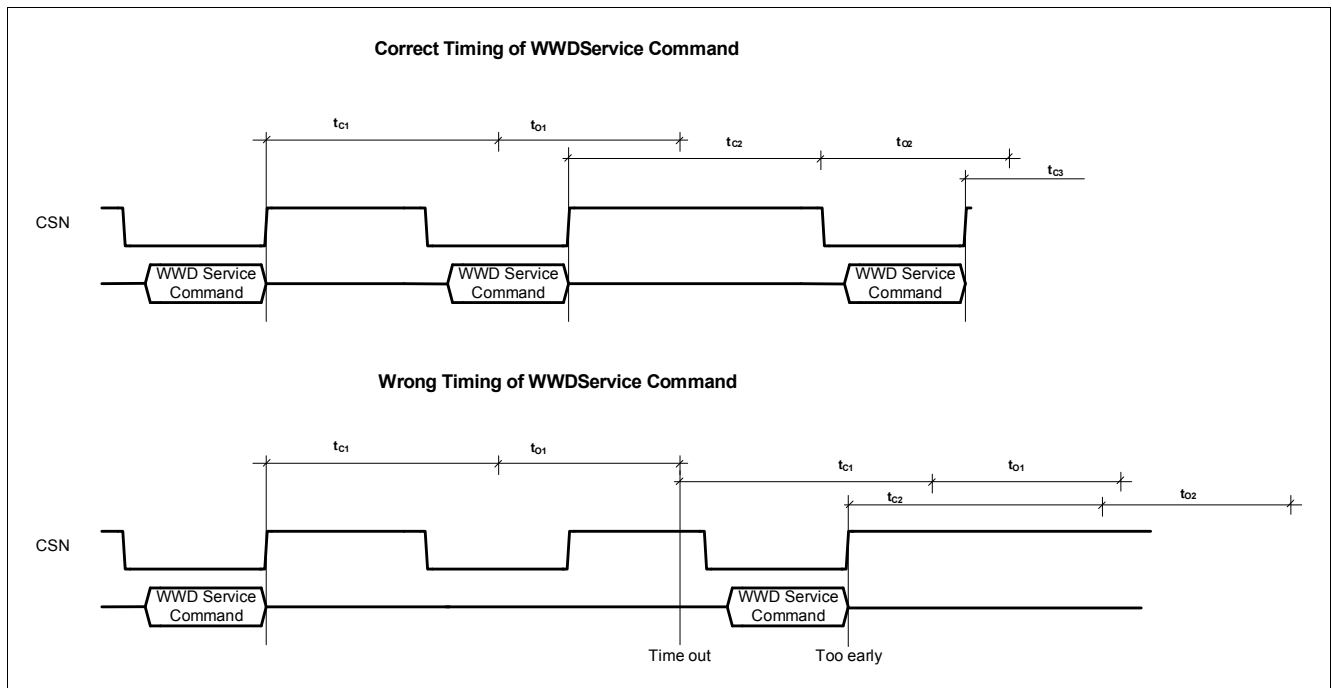


Figure 8 Watchdog Sequence Timing

6.2 Functional Watchdog

For the functional check the micro controller has to send with the commands **FWDRespCmd** (functional watchdog response command) or **FWDRespSyncCmd** (functional watchdog response and synchronisation command) the right four response bytes to the actual question defined by the TLE8888-1QK. The response bytes are checked for correctness.

A pass of the check triggers a decrement of the functional watchdog pass counter. A functional watchdog error (FWD error) is not affecting the functional watchdog pass counter but it is used for the total error counter as an input signal (see [Chapter 6.3](#)). A FWD error is defined as:

- received response byte 0 with **FWDRespCmd** and minimum one of the response bytes are wrong
- received response byte 0 with **FWDRespSyncCmd** and minimum one of the response bytes are wrong
- the watchdog heartbeat timer period synchronisation command **WDHBTPSyncCmd** is received

In the diagnosis register **WdDiag** the bit **FWDREA** signalizes an error of the received response bytes to the actual question and the bit **FWDREL** signalizes an error of the response bytes of the last answer. With a read out the diagnosis bits are not cleared.

To detect that the functional check is missing a heartbeat is implemented. With an heartbeat event the functional watchdog pass counter is incremented. An heartbeat event occurs:

- with expiring of the heartbeat period timer or
- with receiving the watchdog heartbeat period synchronisation command **WDHBTPSyncCmd** (response counter is also reset) or
- with receiving the functional watchdog response and synchronisation command **FWDRespSyncCmd** if response byte 0 is received

The heartbeat period can be set by a write access to the configuration register **WDConfig0** or by the watchdog heartbeat period synchronisation command **WDHBTPSyncCmd**. If the data is 000 0000_B the value of the heartbeat period is not changed.

Behavior of the heartbeat period in case of changing the period time:

 Monitoring Watchdog Module (Signature Watchdog)

- **WDHBTPSyncCmd**: the response counter and the heartbeat timer are reset and a heartbeat event is triggered, the new value of the period is executed with next period.
- write access to the configuration register **WDCConfig0**: the new value of the period is effective after the write command. If the new value is lower than the actual heartbeat timer value then the heartbeat event is immediately triggered otherwise the actual period length is immediately changed to the new value.

The functional watchdog pass counter is a six bit counter (see status register **FWDStat0**). The values for incrementation or decrementation can be set in the configuration register **FWDConfig**. The influence of the counter values to the operation behavior is shown in **Table 12** and **Table 13**.

In **Figure 9** the state machine of the functional watchdog is shown. There are two possible principles available to serve the function watchdog:

- unsynchronized heartbeat and use of functional watchdog response command **FWDRespCmd** and write access to the configuration register **WDCConfig0** to change the heartbeat period time or
- heartbeat is started with receiving the functional watchdog response and synchronisation command **FWDRespSyncCmd** and use of the watchdog heartbeat period synchronisation command **WDHBTPSyncCmd** for changing the heartbeat period

The commands can be used in all possible combinations without restrictions. Using **FWDRespCmd** has the advantage that with fast correct responses the decrement of the functional watchdog pass counter can be speed up.

The bit **FWDKQ** in the configuration register **WDCConfig1** is used to enable the keep question function for the functional watchdog. If the bit is set in case of a passed functional check the next functional check procedure is done with the same question if minimum one of the bits **WWDSCE** or **WWDTO** is set (window watchdog error).

Monitoring Watchdog Module (Signature Watchdog)

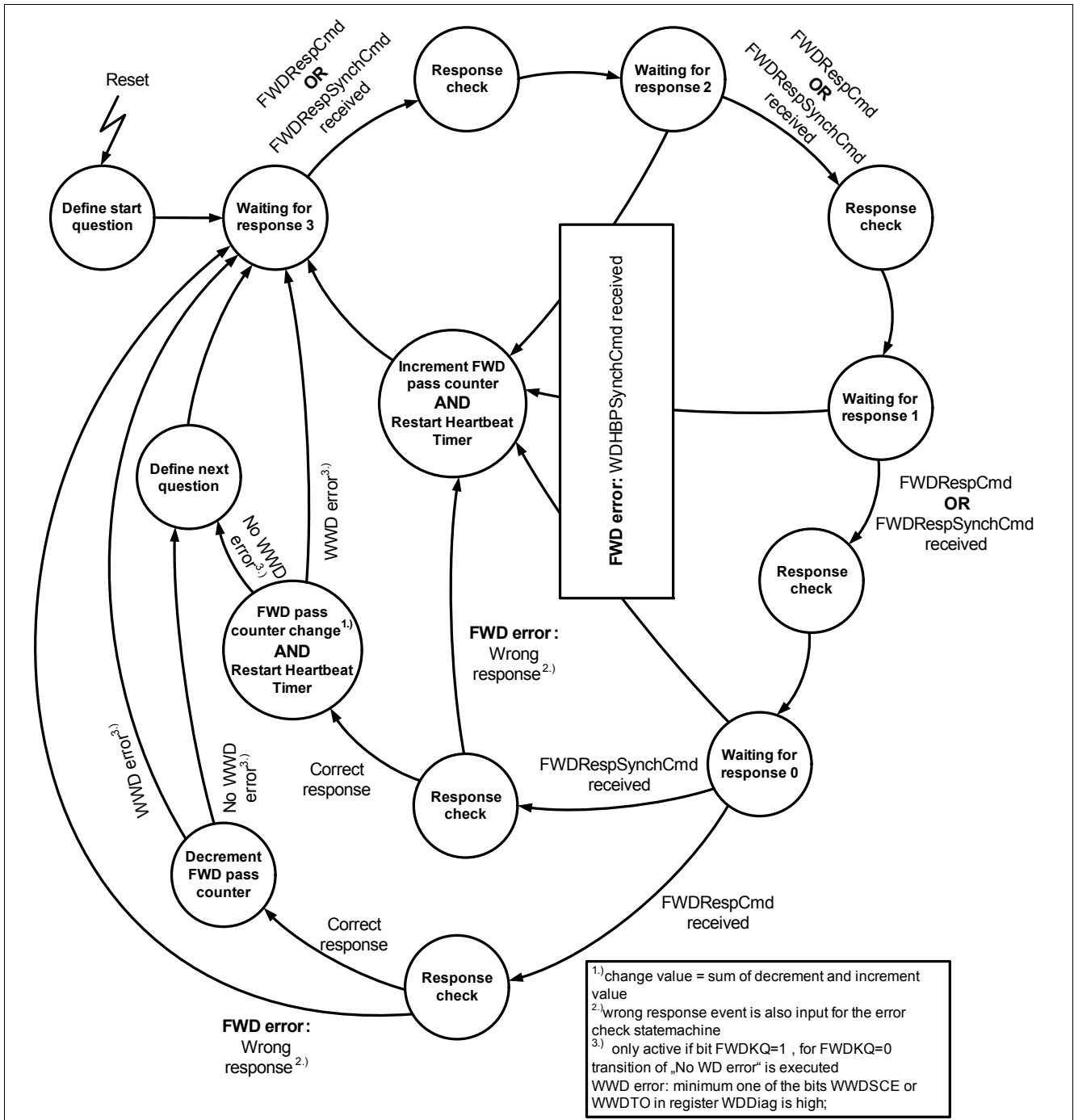


Figure 9 Functional Watchdog State diagram

6.2.1 Question and Response Definition

The bits **FWDQUEST** in the watchdog status register **FWDStat1** represent the actual valid question. The reset value is 0000_B and it will be changed regarding the definition of the state machine for the monitoring module (see **Figure 7**). The expected response is shown in **Table 11**. The answer of the micro controller is done by a write access to the command registers **FWDRespCmd** or **FWDRespSynchCmd**. The actual value of the bits **FWDRESPC** in the watchdog status register **FWDStat1** defines the interpretation of the 8 bit content of these commands as RESP3 to RESP0 (definition see **FWDRESPC**).

Monitoring Watchdog Module (Signature Watchdog)

The definition of the next question is done with a pseudo random algorithm. With the bit **FWDQG** in the configuration register **WDConfig1** the generation algorithm for the questions is defined. There are two settings:

- question pattern length 16: 16 question repeated every 16th watchdog sequence with a minimum hamming distance of 3
- question pattern length 256: every 256 question the order of the 16 questions is repeated, minimum hamming distance is 1

Table 11 Questions and related Response

QUEST[3:0]	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

6.3 Total Error Counter Module

The total error module is used to count the errors of the window watchdog and the functional watchdog. In **Figure 10** the error check state machine is shown. If a watchdog error of the functional or the window watchdog occurs the state machine enters the state “error occurred” and with the next heartbeat event (definition see **Chapter 6.2**) the total error counter is incremented.

The counter is also incremented if a functional watchdog error or at the same time a window watchdog error occurs by using the **FWDRespSyncCmd**. With the **WDHBTPSyncCmd** always an increment of the total error counter is done. A decrement of the total error counter is only possible by using the **FWDRespSyncCmd** and no errors are occurred.

The decrement and increment value of the total error counter can be set with the configuration register **TECConfig**. The status of the total error counter is available in the status register **TECStat**.

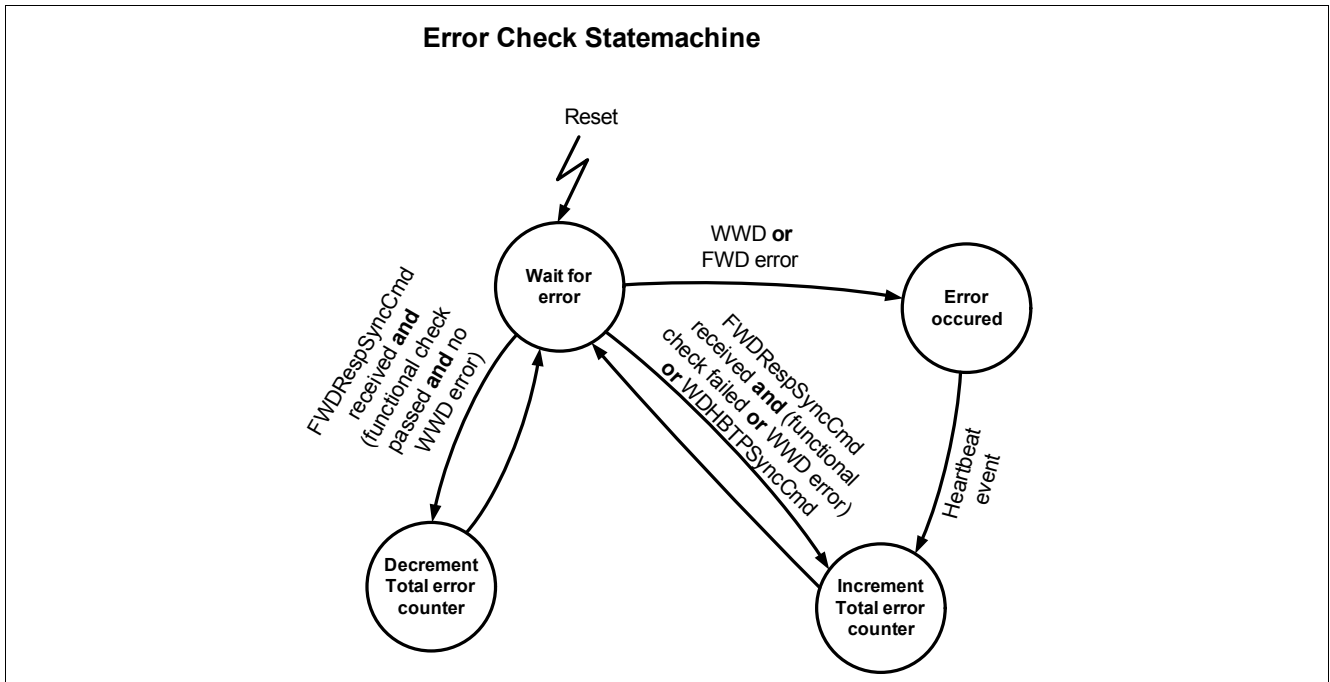


Figure 10 State diagram of the Error check State machine for the Total Error Counter Module

6.4 Watchdog Reset Counter

The watchdog reset counter is a three bit counter (bits **RESC** in **WdStat0**) and is triggered by an overflow of one of the three counters of the monitoring functions (see **Figure 11**). The reset counter can only be incremented by 1. Each time the watchdog reset counter changes the value a watchdog reset occurs depending on the status of watchdog reset enable bit **WDREN** in the configuration register **WdConfig1**. The counter stops counting if **WDREN** = “0” or at full scale. There are no further resets if full scale is reached. The behavior at the different reset conditions is defined in **Chapter 5.2 Table 6** and **Table 7**.

6.5 Power Down Counter

There are three power down counters with three bits implemented. The window watchdog power down counter (bits **WWDPC** in status register **WdStat0**) is triggered by an overflow of the window watchdog error counter, the functional watchdog power down counter (bits **FWDPC** in status register **WdStat1**) is triggered by an overflow of the functional watchdog pass counter and the total error power down counter (bits **TECPDC** in status register **WdStat1**) is triggered by an overflow of the total error counter (see **Figure 11**).

If a trigger occurs the dedicated power down counter is incremented by 1. Additionally all three power down counters are incremented by 1 if a software reset occurs. The power down counters are reset if the ready state is reached (see **Table 12** and **Table 13**).

With an overflow of minimum one of the three power down counters a power down of the TLE8888-1QK is performed if **KEY** is “low” (see **Chapter 5.1**). This function can not be disabled. The behavior at the different reset conditions is defined in **Chapter 5.2 Table 6** and **Table 7**.

6.6 Secure Shut Off Timer

The secure shut off timer (SSOT) is reset with **KEY** = 1 and the timer starts with an overflow of one of the three counters of the monitoring functions (see **Figure 11**) if it is enabled with **KEY** = 0. If the timer is expired after the **Secure shut off time** a power down of the TLE8888-1QK is performed (see **Chapter 5.1**).The behavior at the different reset conditions is defined in **Chapter 5.2 Table 6** and **Table 7**.

Monitoring Watchdog Module (Signature Watchdog)

6.7 Operation State Definition and Reset Generation

The values of the three counter of the monitoring module are affecting the operation state of the TLE8888-1QK. There are three states defined:

- the safe state: this is the reset state. The bits **O1E** to **O24E** and **IGN1E** to **IGN4E** in the configuration register **OEConfig0** to **OEConfig3** are set to "0" to ensure that all actuators are switched off.
- ready state: the device can be operated without restrictions.
- watchdog reset: a reset is performed according the definition in **Table 6** and **Table 7**.

The definition of the three states is shown in **Table 12**. The states are affecting the status of the pins *MON* and *RST*, the power down counter, the secure shut off timer and the reset counter (definition see **Table 13**).

Table 12 Definition of Reset, Safe and Ready State

Safe State	WWDEC > 32 _D OR FWDPC > 32 _D OR TEC > 32 _D
Ready State	WWDEC < 33 _D AND FWDPC < 33 _D AND TEC < 33 _D
Watchdog Reset	WWDEC overflow OR FWDPC overflow OR TEC overflow (for all counters > 63 _D)

Table 13 System Reaction to the watchdog status

	Ready State	Safe State	Watchdog Reset
<i>RST</i>	1	1	0 ¹⁾
<i>MON</i>	1	0	0
Power stages	no influence of normal operation	disabled	disabled
O1E to O24E , IGN1E to IGN4E	X	0	0
WWD error counter FWD pass counter Total error counter	no effect	no effect	reset ¹⁾
Reset counter	no effect	no effect	increment by 1
Window watchdog power down counter Total error power down counter Functional watchdog power down	reset	no effect	increment by 1 regarding the overflow source
Secure shut off timer	no effect	no effect	start of timer with the first overflow if <i>KEY</i> = 0

1) occurs for the defined reset time if watchdog reset is enabled

Monitoring Watchdog Module (Signature Watchdog)

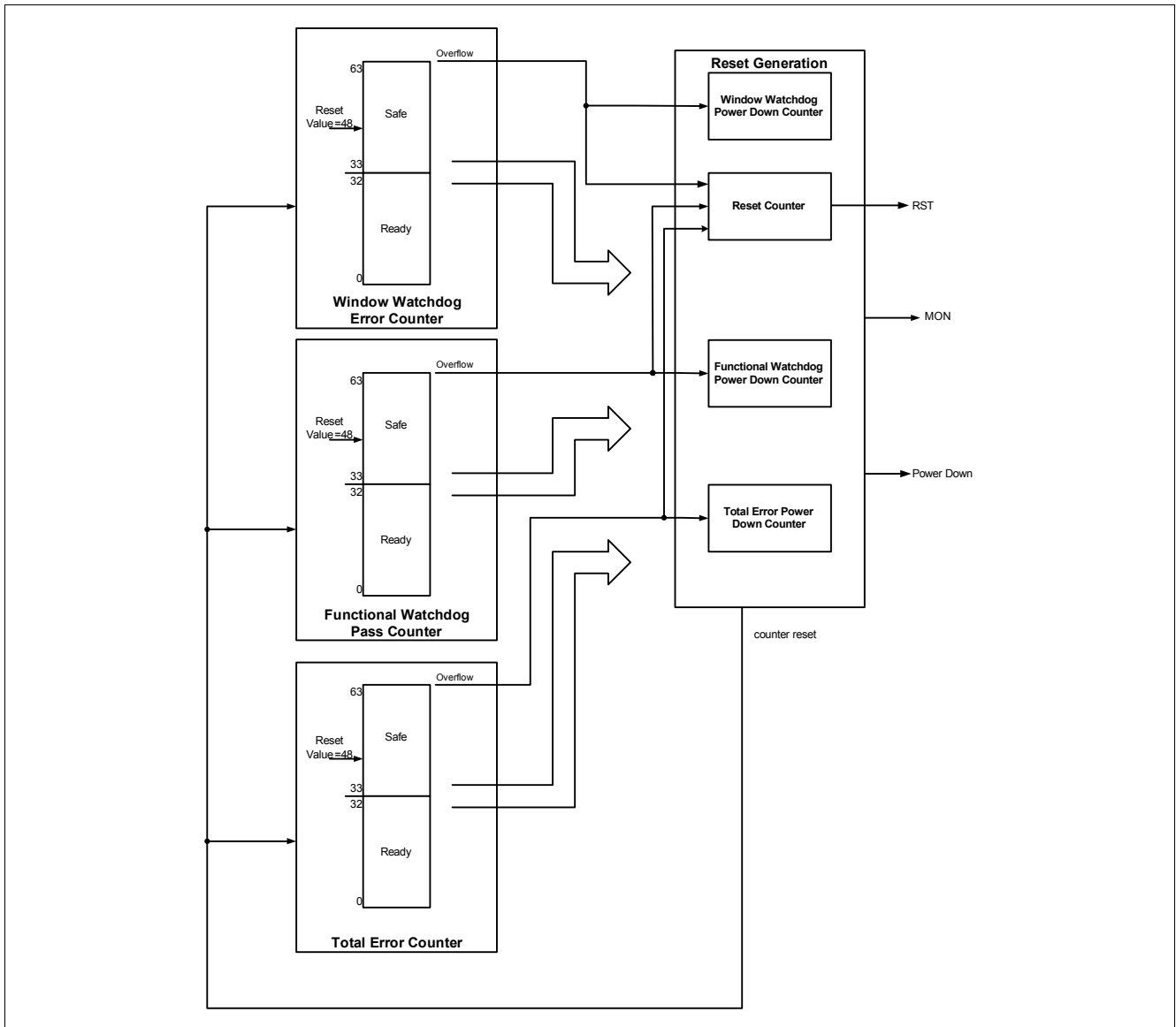


Figure 11 Block diagram of the Reset Generation

Behavior of the WWD error counter, the FWD pass counters and the total error counter in case of over and underflow:

The counters are designed to keep the same value:

- at incrementation if the new counter value is higher than the full scale value of the counter and
- at decrementation if the new counter value is lower than zero.

In [Figure 12](#) an example is shown.

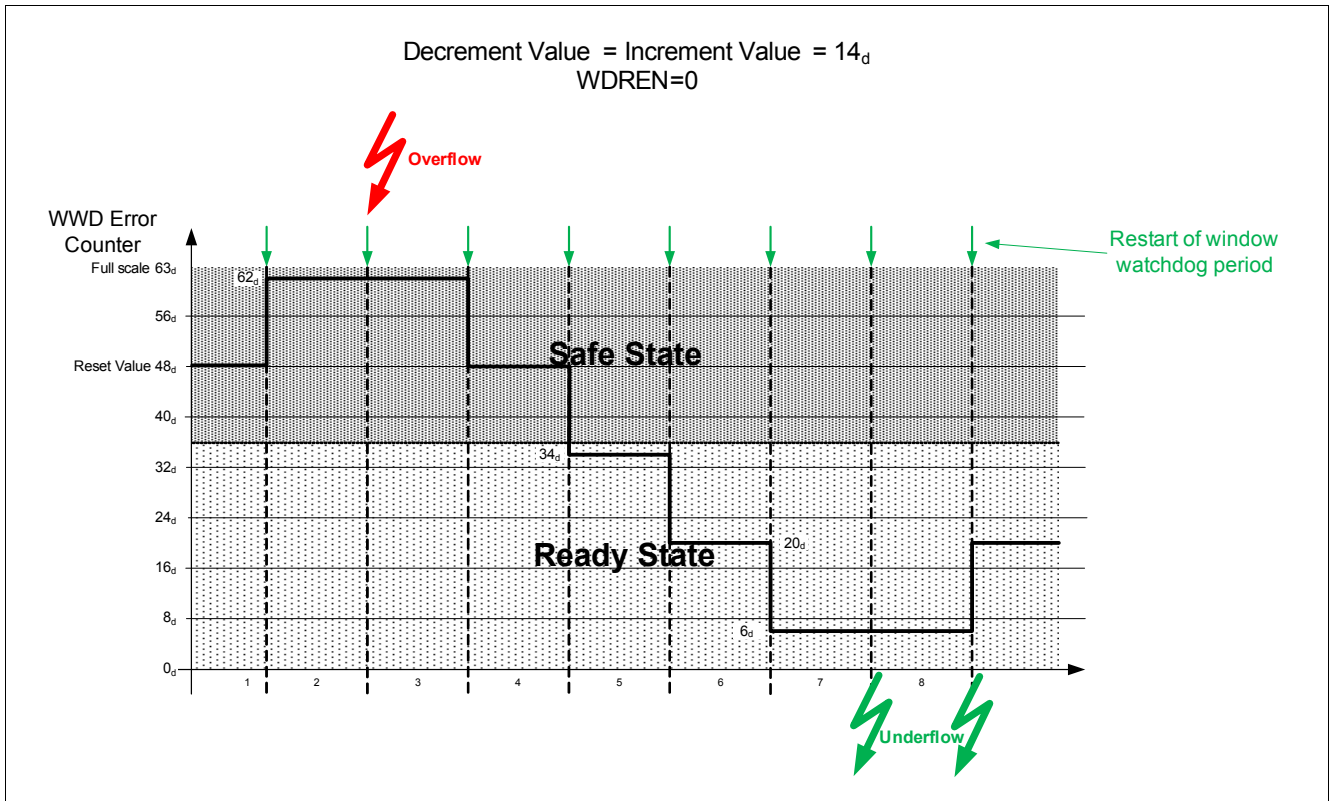


Figure 12 Example of WWD error counter behavior with decrement and increment value of 14d

6.8 Synchronisation of Window Watchdog Sequence and Heartbeat

In Figure 13 the relation between the heartbeat clock generation, the total error counter and the window watchdog sequence generation is shown. The window watchdog sequence generation and the heartbeat period generation have the same clock base with the accuracy of $t_{w,a}$.

The value of the pre-divider and the heartbeat timer can be read out with the status registers **WDHBT0** and **WDHBT1**. This can be used to measure the actual internal clock frequency. Therefore the value of the pre-divider and the heartbeat period counter must be sampled by sending a **Cmd0** command with an activated **WDHBTS** bit. With this command the value of the two registers are stored in the related status registers and the readout can be done.

With two sampled values the micro controller can correct the time information by the value of the actual frequency of the TLE8888-1QK. With such a correction of the micro controller timing check it is possible to use smaller open window times to improve the performance of the timing check. Additional it is possible to use this information for synchronization purpose for the check of the monitoring function of the TLE8888-1QK inside the micro controller.

Monitoring Watchdog Module (Signature Watchdog)

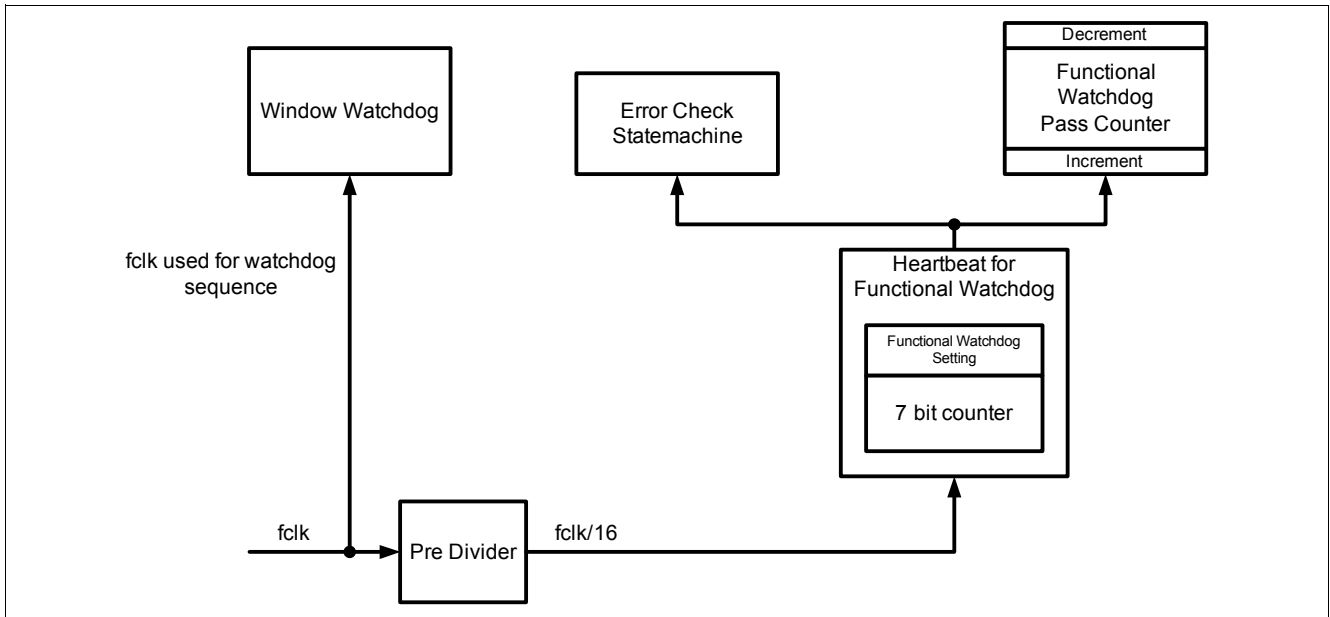


Figure 13 Clock Generation for the Watchdog Module

6.9 Electrical Characteristics Monitoring Watchdog Module

Table 14 Electrical Characteristics: Monitoring Watchdog Module

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^{\circ}C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Window watchdog closed window time	$t_{WWD,ct}$	1.6	–	100.8	ms	63 values	P_6.8.1
Window watchdog closed window time step	$t_{WWD,ct}$	–	1.6	–	ms	–	P_6.8.2
Window watchdog open window time 1	$t_{WWD,ot1}$	–	3.2	–	ms		P_6.9.1
Window watchdog open window time 2	$t_{WWD,ot2}$	–	6.4	–	ms		P_6.9.2
Window watchdog open window time 3	$t_{WWD,ot3}$	–	9.6	–	ms		P_6.9.3
Window watchdog open window time 4	$t_{WWD,ot4}$	–	12.8	–	ms	–	P_6.8.3
Clock frequency accuracy for window watchdog sequence and heartbeat	$t_{w,a}$	-5	–	+5	%	–	P_6.8.4
Heartbeat time period	$t_{HBT,pt}$	1.6	–	203.2	ms	127 values	P_6.9.4
Secure shut off time	t_{SSOT}	18	20	22	min	–	P_6.8.5

Table 15 Switching Behavior of Main Relay at Start Up (Transition ECU Sleep to Supply Ramp Up Mode)

$KEY = 0, WK = EOTWK = CANWK = 0$	-	<i>MR</i> is switched off	Supply is off
$KEY = 1, WK = EOTWK = CANWK = X$	-	<i>MR</i> is switched on	Supply is switched on
$KEY = 0, WK$ or $EOTWK$ or $CANWK = 1$	$BAT < V_{BAT,th}$	<i>MR</i> is switched on	
$KEY = 0, WK$ or $EOTWK$ or $CANWK = 1$	$BAT > V_{BAT,th}$	<i>MR</i> is switched off	

7.1 Wake Up Detection by Pin *KEY* and Key Off Delay

The input pin *KEY* is implemented to detect the status of the key switch in the car. With a high signal the start up of the TLE8888-1QK is initiated. During start up the implemented circuitry provides also the supply for switching the main relay. A deglitch filter is implemented to be robust against disturbances (see [Figure 16](#)). After ramp up the supply of the main relay is provided by the internal supply. To provide a direct access from the *KEY* signal to actuators a key off delay function is implemented.

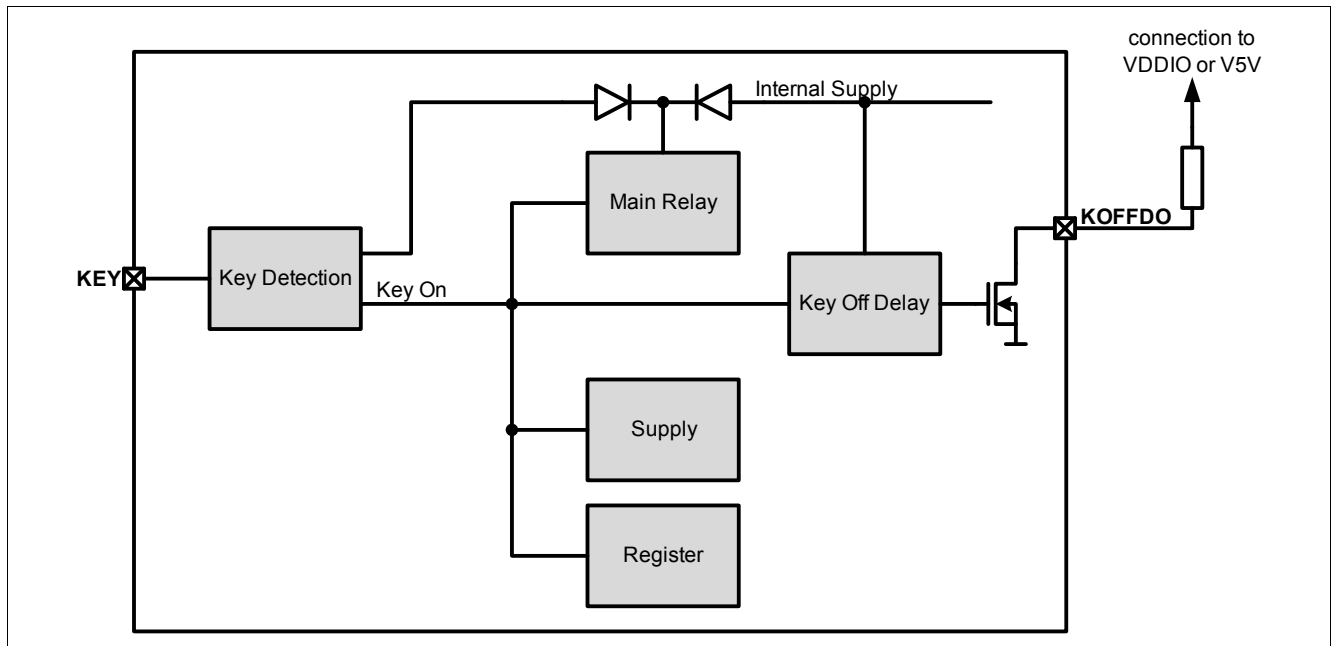


Figure 15 Block Diagram of the Key Detection

In [Figure 16](#) the effect of the filter time is shown. The status of the pin *KEY* including the filter time is reflected in bit *KEY* in the status register [OpStat0](#).

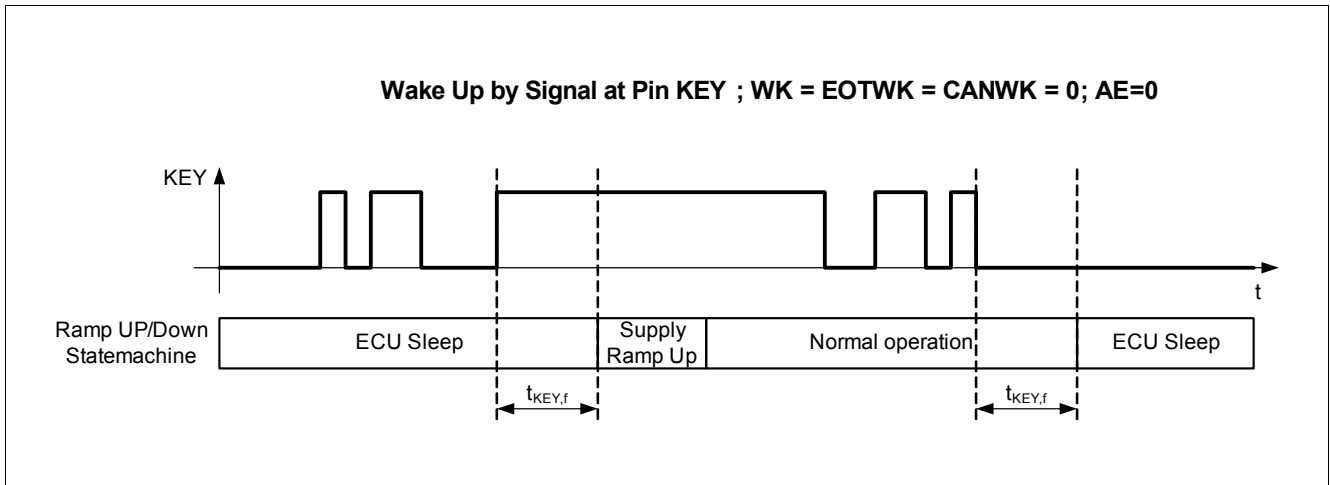


Figure 16 Function of Key detection filter time

The key off delay function provides the *KEY* signal at the open drain output *KOFFDO*. The positive edge is delayed by the **Key Detection Filter Time** and the negative edge by the **Key Off Delay Time 1** to **Key Off Delay Time 4** (according setup of the bits **KOD** in register **OpConfig0**) if the supply is available.

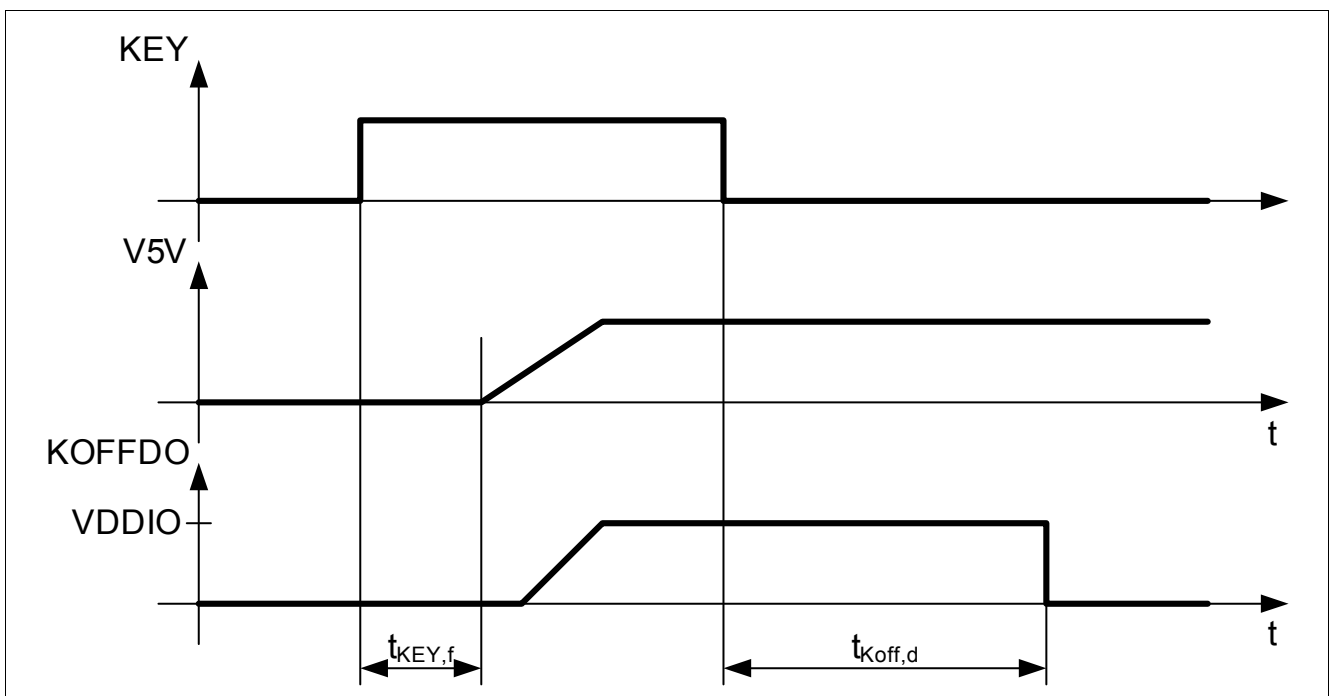


Figure 17 Timing Diagram of the Key Off Delay

7.2 Wake Up Detection by Pin *WK*

The pin *WK* is used e.g. for an external CAN device with wake up function on the ECU. With a high signal the start up of the TLE8888-1QK is initiated. During ramp up the supply for the main relay circuit is provided by the active wake up pin *WK*. After ramp up the supply of the main relay circuit is provided by the internal supply. In **Figure 18** the block diagram of the wake up detection by pin *WK* is shown.

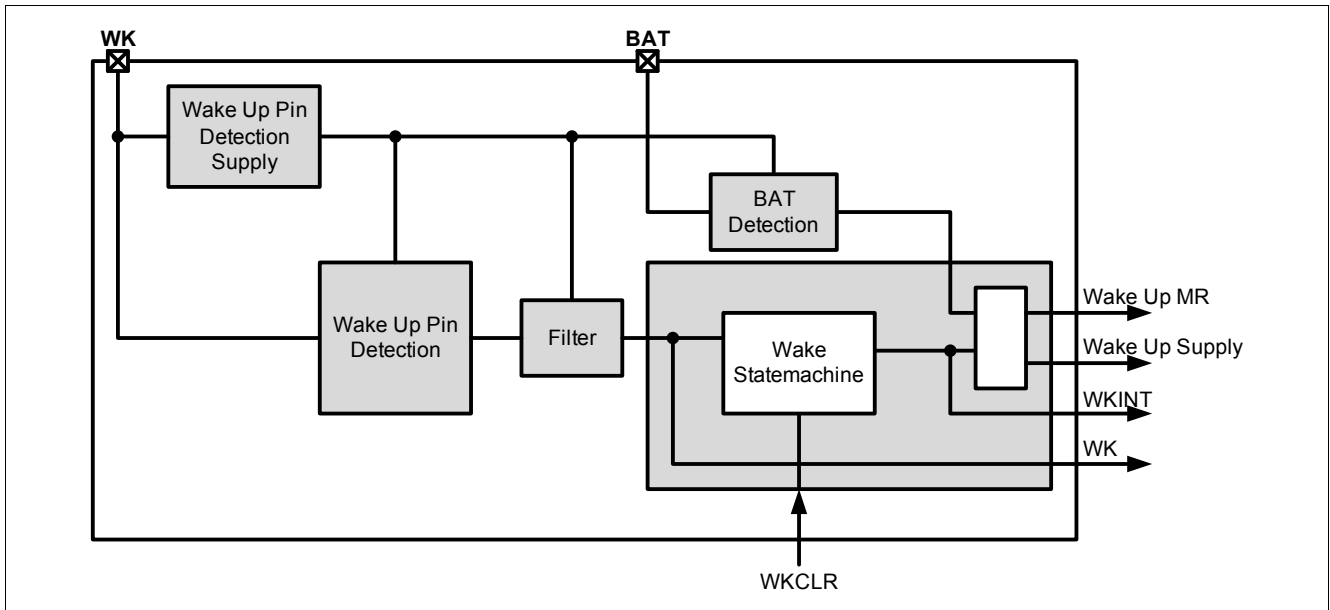


Figure 18 Block Diagram of the Wake Up Detection

For wake up by pin *WK* special functions are implemented.

- main relay is switched on depending on the voltage level at pin *BAT* (see [Table 15](#))
- power down procedure in case of a permanent *WK* = "1" and a blocked micro-controller (see description in [Chapter 5.1 Operation States](#))
- wake clear bit *WKCLR* in the command register *Cmd0* to clear the internal wake up signal in case of permanent *WK* = "1" signal
- deglitch filter of $t_{WK,f}$ for positive and negative edge at pin *WK*

In [Figure 19](#) the effect of the filter time is shown. The status of the pin *WK* including the filter time is reflected in bit *WK* in the status register *OpStat0*.

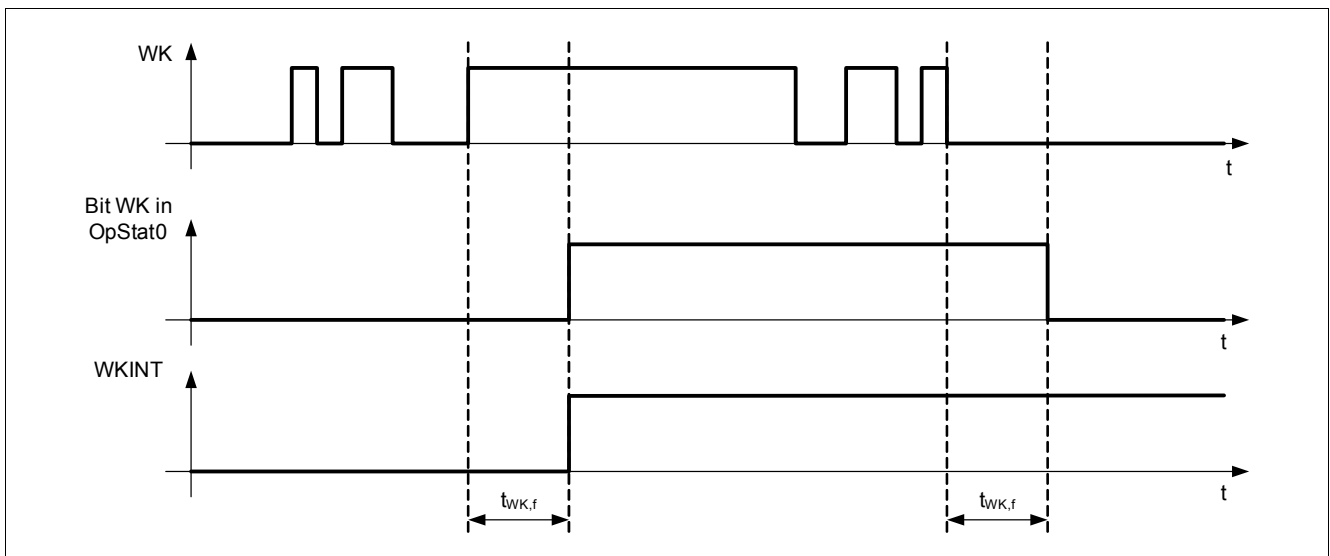


Figure 19 Function of *WK* detection filter time

To realize the power down procedure an internal wake up signal *WKINT* is used (status see bit *WKINT* in the status register *OpStat0*). In [Figure 20](#) the state diagram of the internal wake signal generation is shown. With a positive edge at pin *WK* the internal signal *WKINT* is set to "1" and a wake up is triggered. With a wake up clear command (set bit *WKCLR* to "1" in command register *Cmd0*) *WKINT* is reset (see [Figure 22](#)). The next wake up by pin *WK*

Wake Up Detection and Main Relay Driver

is only detected with a positive edge at pin *WK*. A permanent high level at pin *WK* doesn't lead to permanent wake up situation. Details of the operation behavior see [Chapter 5.1 Operation States](#).

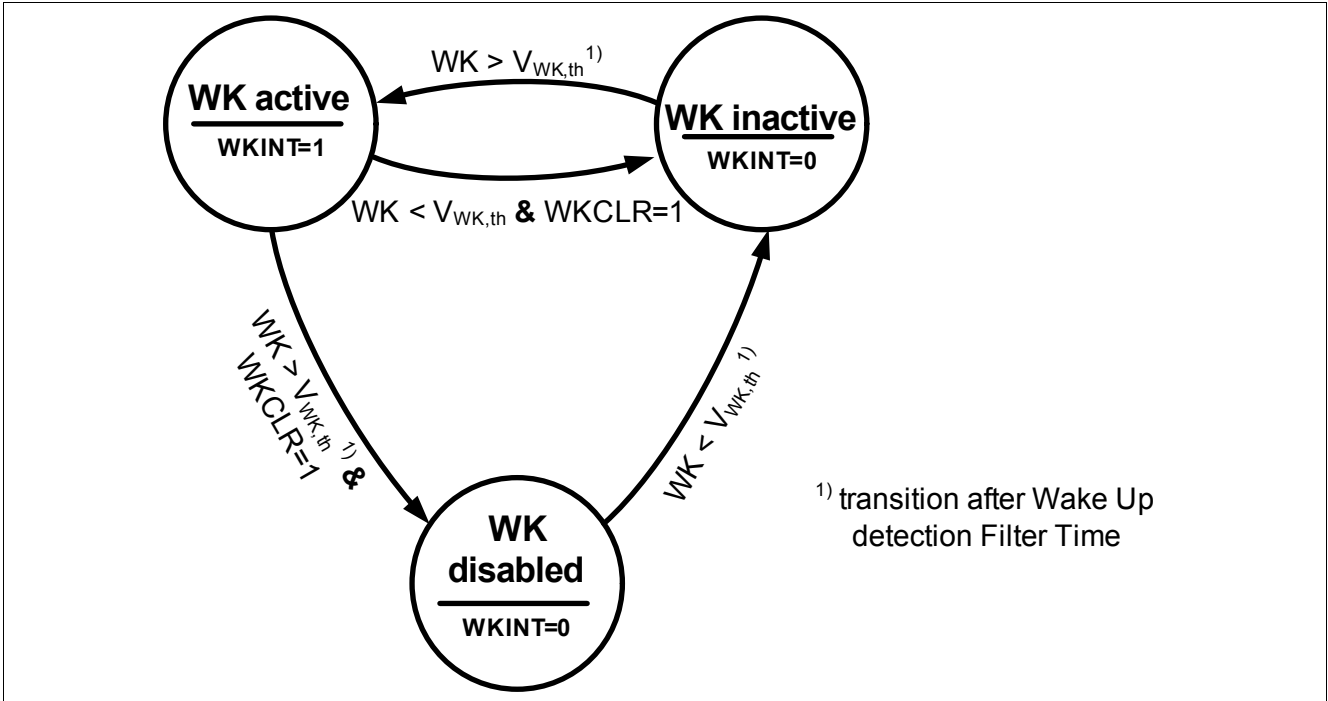


Figure 20 State Diagram of the Wake State Machine for Internal Wake Signal

At the beginning of the functional diagram of [Figure 21](#) a normal wake up sequence with a wake signal of the pin *WK* is shown. In the second part of the diagram the signal of pin *WK* stick at high (e.g. short to battery) and the micro controller must send a wake clear command (bit *WKCLR*=1 in command register *Cmd0*) for entering the ECU sleep mode. With a low at pin *WK* the wake state machine is set to the state “WK inactive” and a wake up by pin *WK* is enabled.

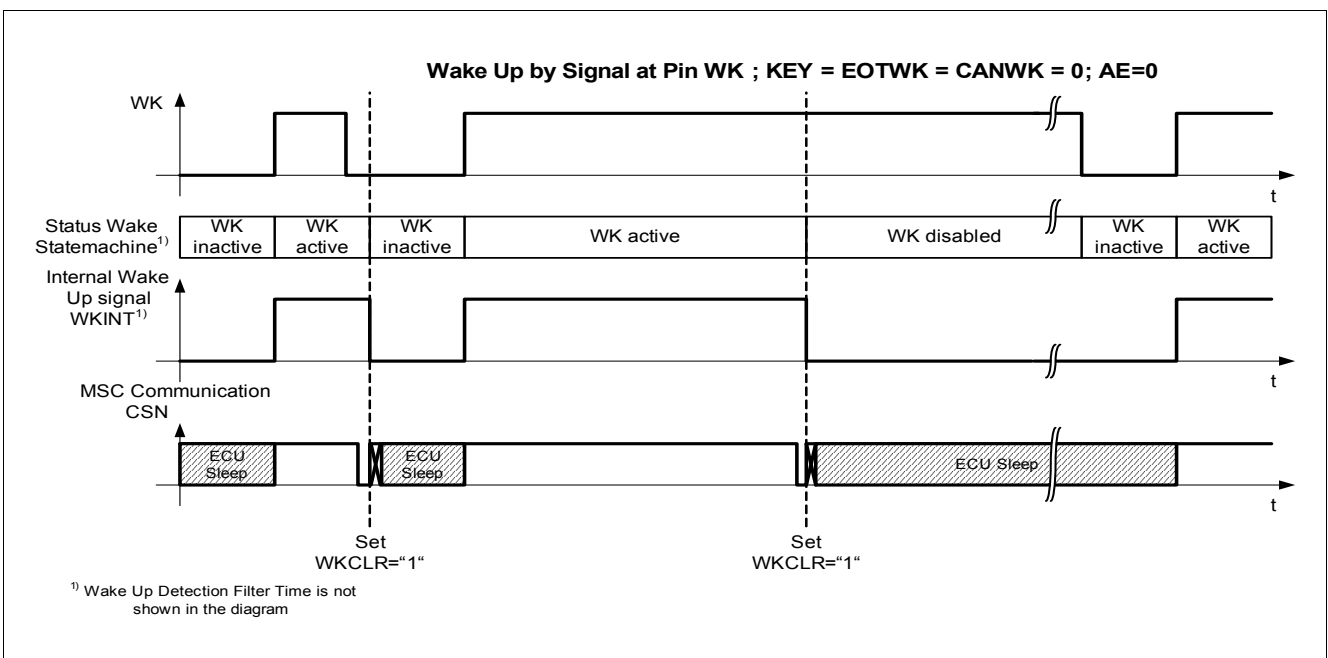


Figure 21 Functional Diagram for Internal Wake Signal

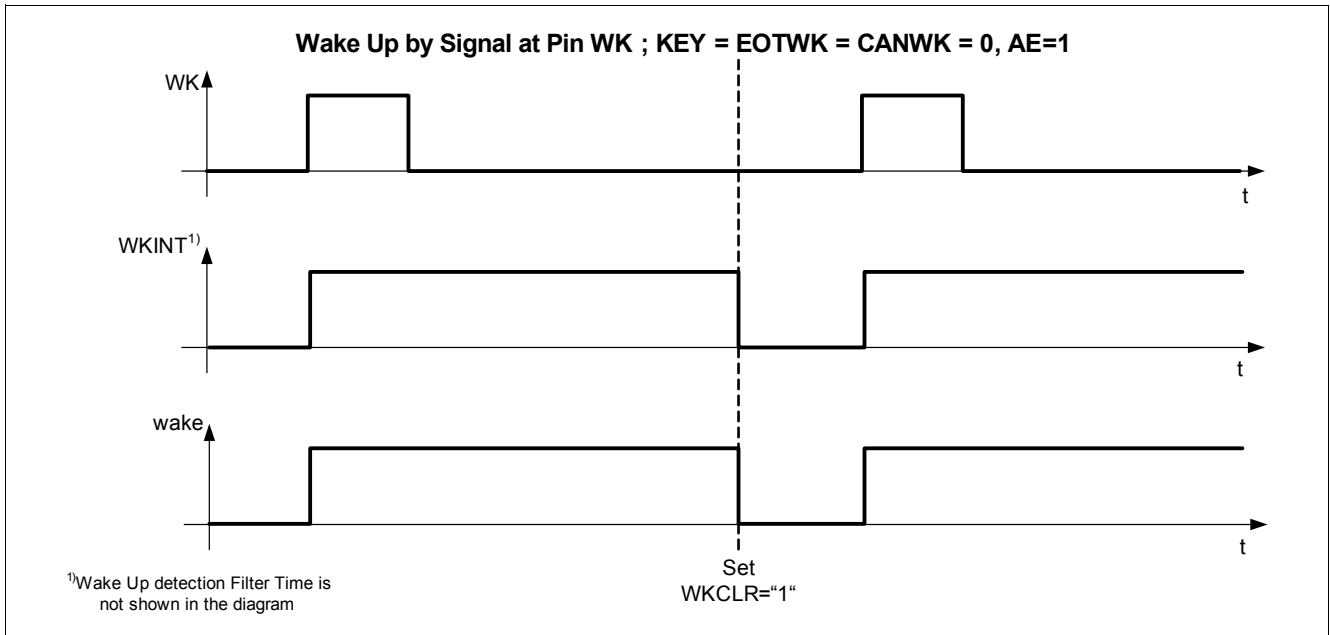


Figure 22 Functional Diagram of Detection of Two Internal Wake Signals

7.3 Main Relay Driver

The main relay driver is designed to switch on the main relay of engine management applications. It integrates a reverse protected low side switch with active clamping freewheeling. The output is protected against overload with an over-temperature detection and an over-current protection circuit. At low battery voltage ($V5V$ main supply is below under voltage detection threshold e.g. during cranking) the main relay stays on. The on resistance is related to the supply voltage at pin *BAT* and is defined down to 4.5V.

The main relay is automatically switched on with a wake up signal according to [Table 15](#). The main relay is normally switched off automatically according the power down procedure defined in [Chapter 5](#).

With write access to the command bit **MRON** of the command register **Cmd0** the main relay can be switched additionally by MSC/SPI control according to the status of *KEY*, *WK*, *EOTWK* and *CANWK* (see [Table 16](#)). The status of the main relay is available in the status register **OpStat0** bit **MR**.

Table 16 Effect of MSC/SPI Write Command Bit **MRON**

<i>KEY</i> = 0, <i>WK</i> = <i>EOTWK</i> = <i>CANWK</i> = X	<i>MR</i> is switched according to write command
<i>KEY</i> = 1, <i>WK</i> = <i>EOTWK</i> = <i>CANWK</i> = X	<i>MR</i> is always switched on

The main relay driver is protected against over-current and over-temperature. In the case of over-current and/or over-temperature the output is switched off and is switched on again after release of the failure condition. This leads to a repetitive switching. A minimum off time $t_{MR,off}$ is implemented to ensure no destruction due to repetitive switching.

7.4 Engine Off Timer

The engine off timer is integrated to measure the time in ECU sleep mode. Additionally the comparator mode is implemented to wake up the TLE8888-1QK after a defined time. It is internally supplied out of the standby supply pin *V5VSTBY*. With the pin *EOTEN* the function is enabled with a connection to *V5VSTBY* and disabled with a connection to *AGND*. It consists of an oscillator optimized for low current operation, a counter and a comparator. The counter counts up to 36 hours and if the counter value reaches the comparator threshold an internal wake up signal is generated. The activation of the comparator mode is done with a definition of a

Wake Up Detection and Main Relay Driver

comparator threshold greater than 0000_H in configuration registers **EOTConfig0** and **EOTConfig1**. There are two operation modes implemented:

- **Counter Mode:** only counter is working, no wake up with comparator threshold
- **Comparator Mode:** counter operation like counter mode, additional wake up with comparator threshold

In comparator mode the internal EOTWK flag is set if the counter is equal to compare value in the configuration registers **EOTConfig0** and **EOTConfig1**. The reset of the EOTWK flag is done with the bit **WKCLR** in the command register **Cmd0** if the counter value is not equal to the compare value.

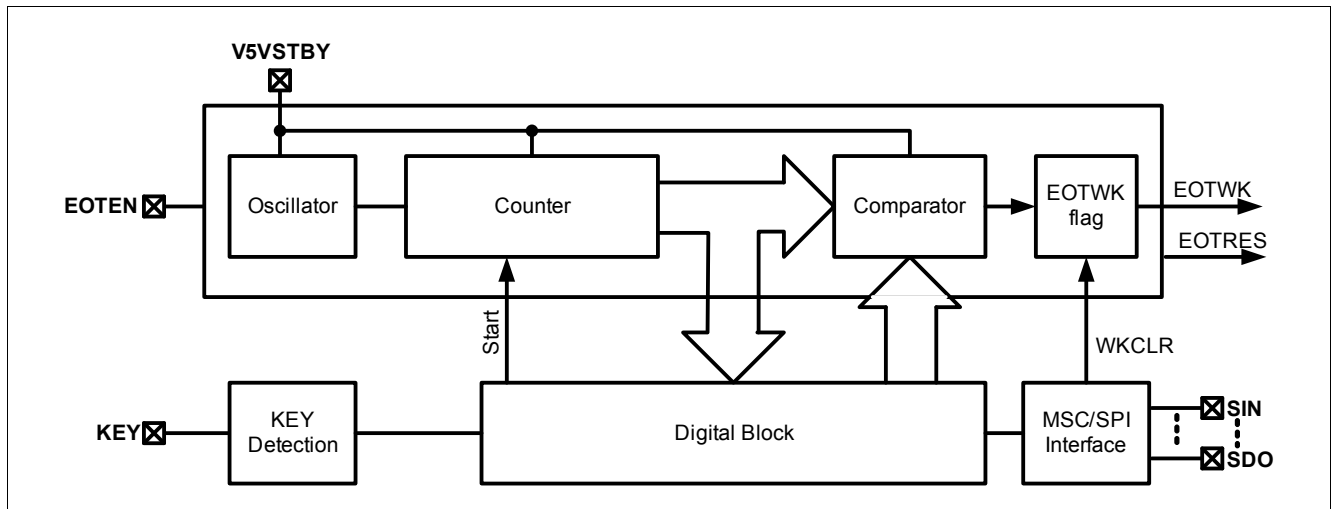


Figure 23 Block Diagram Engine Off Timer

The start of the counter can be configured with the bit **EOTCONF** in the configuration register **OpConfig0** to

- start by **KEY** signal (reset value) and
- start by MSC command

With the falling edge of the **KEY** signal or with the execution of the MSC command the counter is reset and starts counting (see **Figure 24**). The start command is performed with setting the bit **EOTS** to “1” in the command register **Cmd0**.

The status bit **EOTRES** (register **OpStat1**) is implemented to highlight that a standby reset has happened. With the start of the counter this bit is reset. Therefore the status of this bit must be readout before the start of the engine off timer.

The 24 bits of the counter are available in the status register **EOTStat0**, **EOTStat1** and **EOTStat2**. For easier access to the engine off timer status the multiple read command **MSCReadDiag0EOT** is implemented.

After wake up the counter doesn't stop counting. A readout of the counter value doesn't stop counting. With this behavior it is possible to measure the counting time with the micro controller (see **Figure 25**).

With a read out of two counter values in a defined time a correction factor can be calculated (difference of counter values divided by the time between the two read outs). With this measurement of the correction factor only the variation caused by the temperature of the timer are effective. The absolute variations are corrected by the correction factor. There are no restrictions for the measurement time but due to the resolution of the counter a minimum measurement time Δt of 1s is recommended.

After power up of the engine off timer circuit with a supply ramp up at pin **V5VSTBY** the counter value and the comparator threshold are reset to the reset value. Additionally the bit **EOTRES** in the status register **OpStat1** is set to “1”.

Any other resets like ECU power on reset have no impact to the engine off timer counter. The compare configuration register **EOTConfig0** and **EOTConfig1** are cleared with an ECU power on reset.

The counter stops counting at full scale. If a standby supply reset occurs the counter stops counting and is reset to “0”.

Wake Up Detection and Main Relay Driver

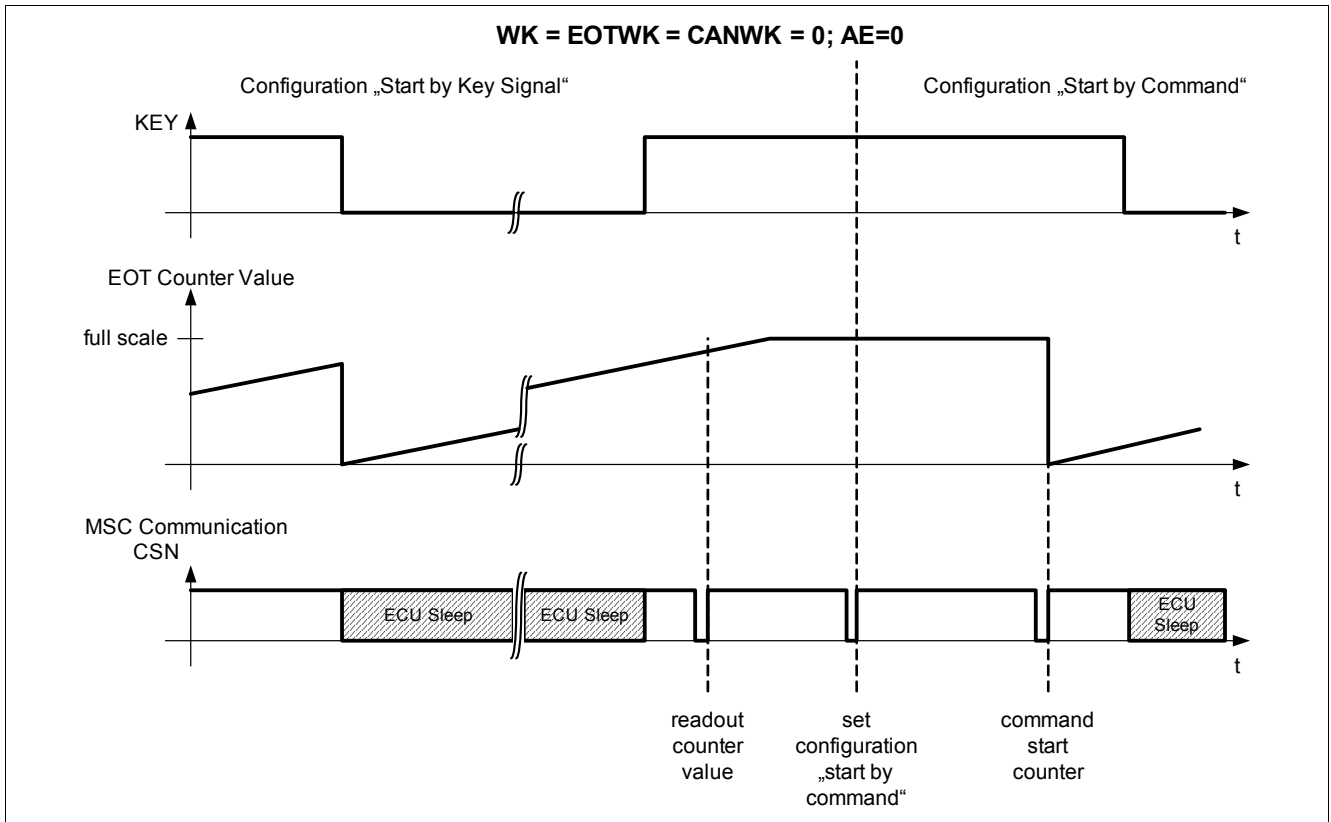


Figure 24 Function Diagram Engine Off Timer Counter Mode

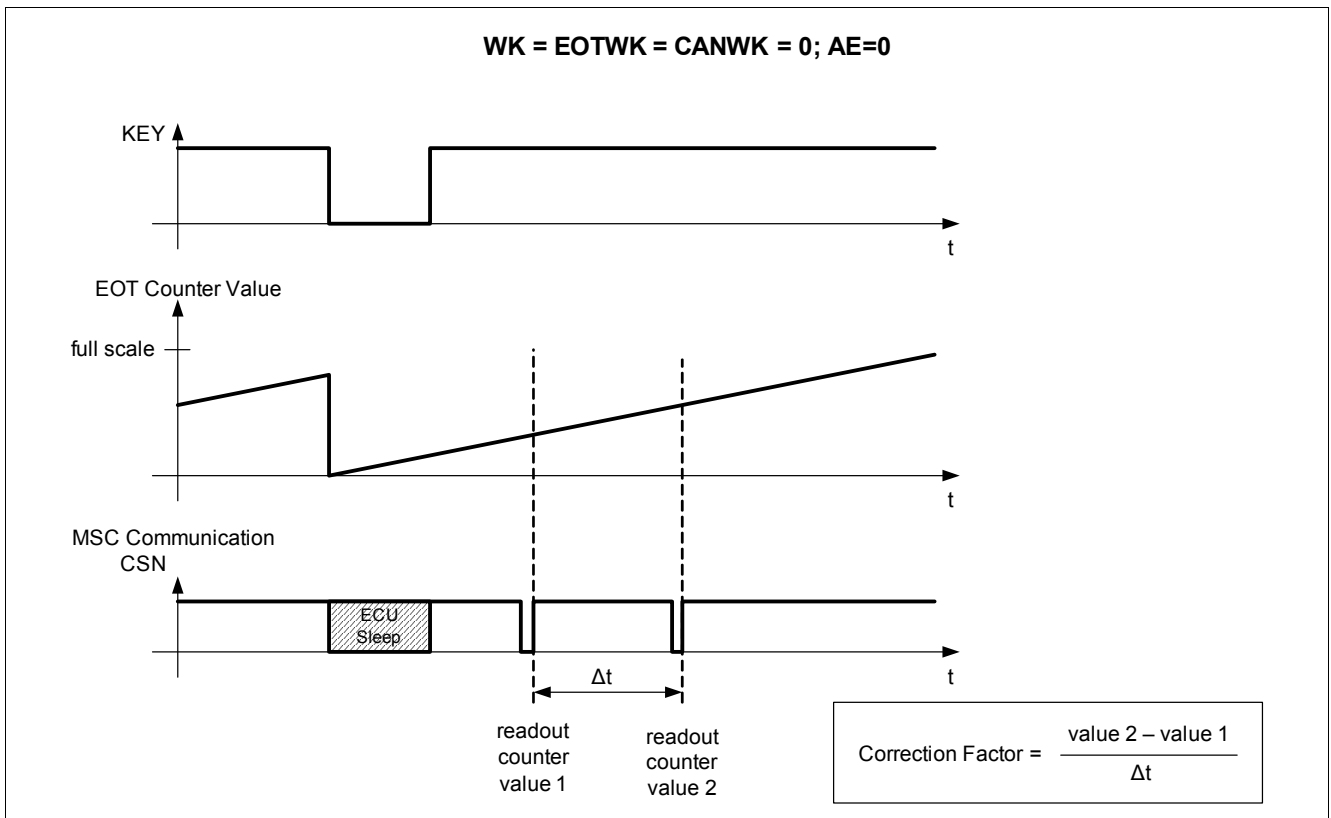


Figure 25 Function Diagram Engine Off Timer Correction Factor Measurement

Wake Up Detection and Main Relay Driver

In comparator mode there is no difference in the behavior of the counter as described above. Additionally a comparator threshold different to 0000_H for wake up is defined in the configuration register **EOTConfig0** and **EOTConfig1**. The comparator mode is enabled with a threshold value different to 0000_H. If the counter value is equal to the comparator threshold the internal wake up signal EOTWK (status see bit **EOTWK** in the status register **OpStat0**) of the TLE8888-1QK is active (see **Figure 26**).

With a wake up clear command (set bit **WKCLR** to "1" in command register **Cmd0**) the internal EOTWK signal is reset.

Table 17 Counter Definition

EOTC[23:0]		
000000 _H	reset value	
000001 _H to FFFFFFF _H	1/128s to 131071s = 36h + 24min + 31s	time resolution 1/128s

Table 18 Comparator Threshold Definition

EOTTH[15:0]		
0000 _H	reset value	comparator mode disabled
0001 _H to FFFF _H	2s to 131070s = 36h + 24min + 30s	comparator mode enabled, time resolution 2s

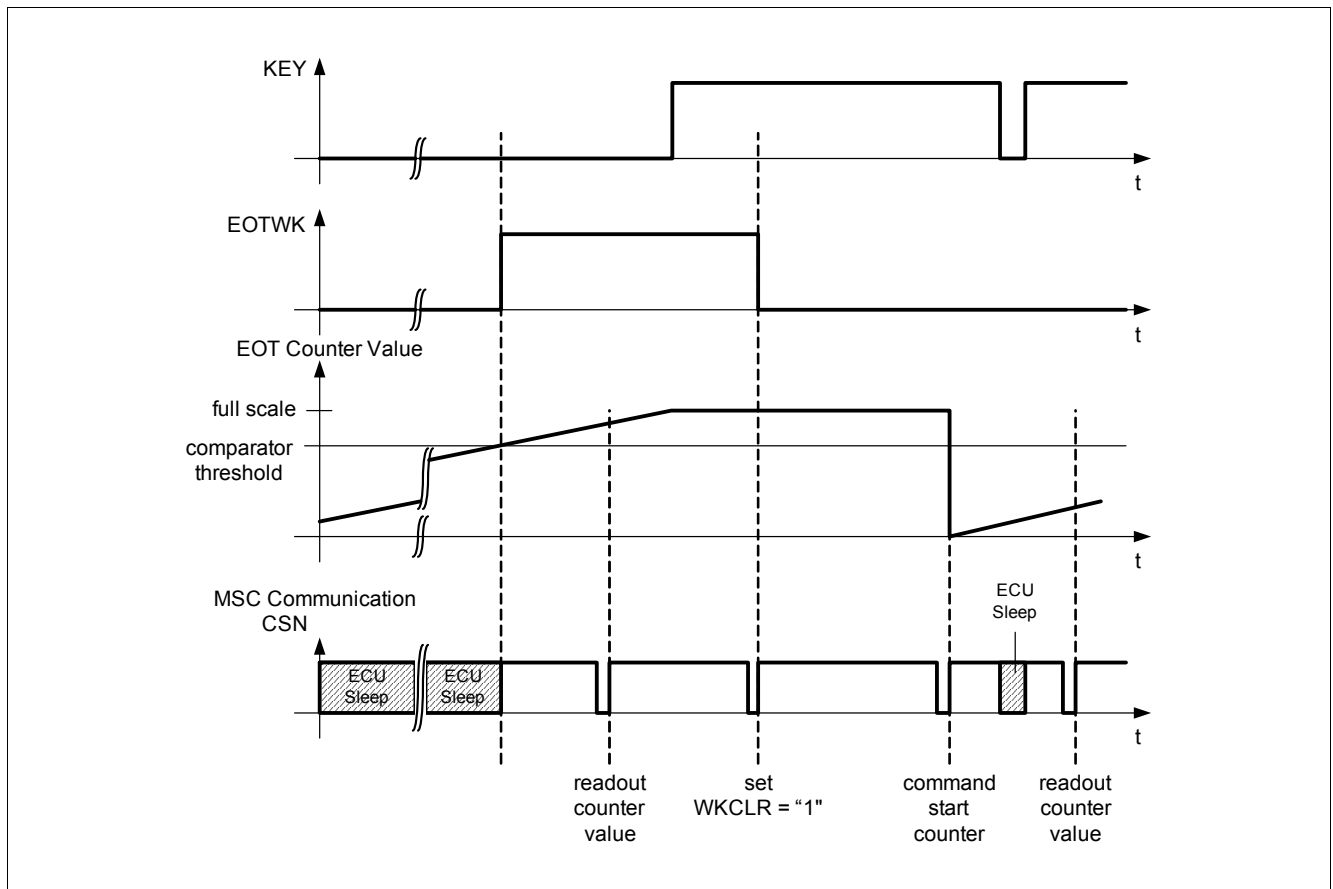


Figure 26 Function Diagram Engine Off Timer Comparator Mode

7.5 Electrical Characteristics Key Detection, Wake Up Detection and Main Relay Driver

Table 19 Electrical Characteristics Key Detection
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Key On Detection Threshold	$V_{KEY,th}$	3.6	–	4.5	V	rising edge	P_7.5.1
Key On Detection Hysteresis	$V_{KEY,h}$	140	250	400	mV	–	P_7.5.2
Input Current during wake up	I_{KEY}	–	–	0.55	mA	$V_{KEY}=5V^{1)}$	P_7.5.3
Input Current after wake up	I_{KEY}	–	–	0.7	mA	$V_{KEY}=V_{BAT}=4.5V$	P_7.5.31
Key Detection Filter Time	$t_{KEY,f}$	7.5	16	24	ms	$V_{KEY}=5V$	P_7.5.4
Key Off Delay Time 1	$t_{KEYoff,d,1}$	100	–	200	ms	–	P_7.5.5
Key Off Delay Time 2	$t_{KEYoff,d,2}$	200	–	400	ms	–	P_7.5.6
Key Off Delay Time 3	$t_{KEYoff,d,3}$	400	–	800	ms	–	P_7.5.7
Key Off Delay Time 4	$t_{KEYoff,d,4}$	800	–	1600	ms	–	P_7.5.8

Output *KOFFDO*

Output Current Capability	I_{KOFFDO}	15 ²⁾	–	–	mA	$V_{KOFFDO}=5V$	P_7.5.9
<i>KOFFDO</i> Output Low Level	$V_{KOFFDO,low}$	–	–	0.4	V	$I_{KOFFDO}<1mA$	P_7.5.30

1) not subject to production test, specified for design

2) Application must ensure that current into this pin does not exceed this value.

Table 20 Electrical Characteristics Wake Up Detection
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Wake Up Detection Threshold	$V_{WK,th}$	3.6	–	4.5	V	rising edge	P_7.5.10
Wake Up Detection Hysteresis	$V_{WK,h}$	140	250	400	mV	–	P_7.5.11
Input Current during Wake Up	I_{WK}	–	–	0.55	mA	$V_{WK}=5V^{1)}$	P_7.5.12
Wake Up Detection Filter Time	$t_{WK,f}$	1	2	3.5	ms	$V_{WK}=5V$	P_7.5.13
Battery Detection Threshold	$V_{Bat,th}$	3.5	–	5	V	$V_{WK}=5V$	P_7.5.14

1) not subject to production test, specified by design

Wake Up Detection and Main Relay Driver

Table 21 Electrical Characteristics Main Relay Driver
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
MR Operation Current	I_{MR}	–	–	0.8	A	–	P_7.5.15
MR Over Current Limitation	$I_{MR,oc}$	0.8	–	1.5	A	–	P_7.5.16
MR On Voltage	V_{MR}	–	–	1.35	V	$I_{MR}=0.3A$	P_7.5.17
MR switch off time in failure case	$t_{MR,off}$	16	27	–	ms	in case of over-current and/or over-temperature	P_7.5.32
MR On Voltage at Low Battery Voltage, low temperature	$V_{MR,I,LT}$	–	–	1.1	V	$I_{MR}=0.1A$, $V_{BAT}=4.5V$ (decreasing) $T_j<25^\circ\text{C}$	P_7.5.18
MR On Voltage at Low Battery Voltage, high temperature	$V_{MR,I,HT}$	–	–	1.05	V	$I_{MR}=0.1A$, $V_{BAT}=4.5V$ (decreasing) $T_j>25^\circ\text{C}$	P_7.5.19
MR Clamping Voltage	$V_{MR,cl}$	40	–	60	V	$I_{MR}=0.2A$	P_7.5.20
MR Clamping Energy ¹⁾	$E_{MR,cl}$	–	–	6.5	mJ	$I_{MR}<0.3A$, $T_j=150^\circ\text{C}$, $40 \cdot 10^6$ cycles	P_7.5.21
MR leakage current in off mode, positive voltage	$I_{MR,leak,pos}$	–	–	5	μA	$V_{MR}=13.5V$, $V_{KEY}=0V$ and $V_{WK}=0V$	P_7.5.22
MR leakage current in off mode, negative voltage	$I_{MR,leak,neg}$	-100	–	–	μA	$V_{MR}=-13.5V$, $V_{KEY}=0V$ and $V_{WK}=0V$	P_7.5.23

1) not subject to production test

Table 22 Electrical Characteristics Engine Off Timer
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Oscillator Accuracy	$\Delta f_{osc,a}$	-30	–	+30	%	$V_{V5VSTBY}=5V$	P_7.5.24
Oscillator Frequency Variation over Temperature	$\Delta f_{osc,T}$	-5	–	+5	%	$V_{V5VSTBY}=5V$, $T_j=-40^\circ\text{C}$ to 85°C , one single device	P_7.5.25
Counter Resolution	$C_{EOT,r}$	–	1/128	–	s	–	P_7.5.26
Counter Full Scale	$C_{EOT,fs}$	–	–	24	bit	–	P_7.5.27
		–	131071	–	s	–	

Wake Up Detection and Main Relay Driver

Table 22 Electrical Characteristics Engine Off Timer (cont'd)

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Additional current consumption at pin <i>BATSTBY</i> for enabled engine off timer function	I_{EOTSUP}	–	–	10	μA	$V_{V5VSTBY}=5V$ and no wake up	P_7.5.28
Additional current consumption at pin <i>BATSTBY</i> for enabled engine off timer function and wake up ¹⁾	$I_{EOTSUP,w}$	–	–	450	μA	$V_{V5VSTBY}=5V$ and wake up	P_7.5.29

1) not subject to production test, specified by design

8 Power Supply

The power supply unit generates the internal supply (including supply for CAN and pre-drivers, voltage reference and current biasing), the main supply voltage for the ECU ($V5V$) and sensor supplies for off-board sensors ($T5V1$ and $T5V2$). All supplies start working by the wake up signal generated by the key and wake up detection (see [Chapter 7.2](#) for details).

A linear pre-regulator with an external logic level power MOSFET is implemented to keep the power dissipation of the TLE8888-1QK low. The precise voltage supplies for the ECU and the sensor supplies are integrated inclusive the power transistor. All supplies with low drop functionality (main supply $V5V$, pre-regulator, sensor supplies $T5V1/T5V2$) are using an integrated charge pump to provide low drop behavior at low battery voltages.

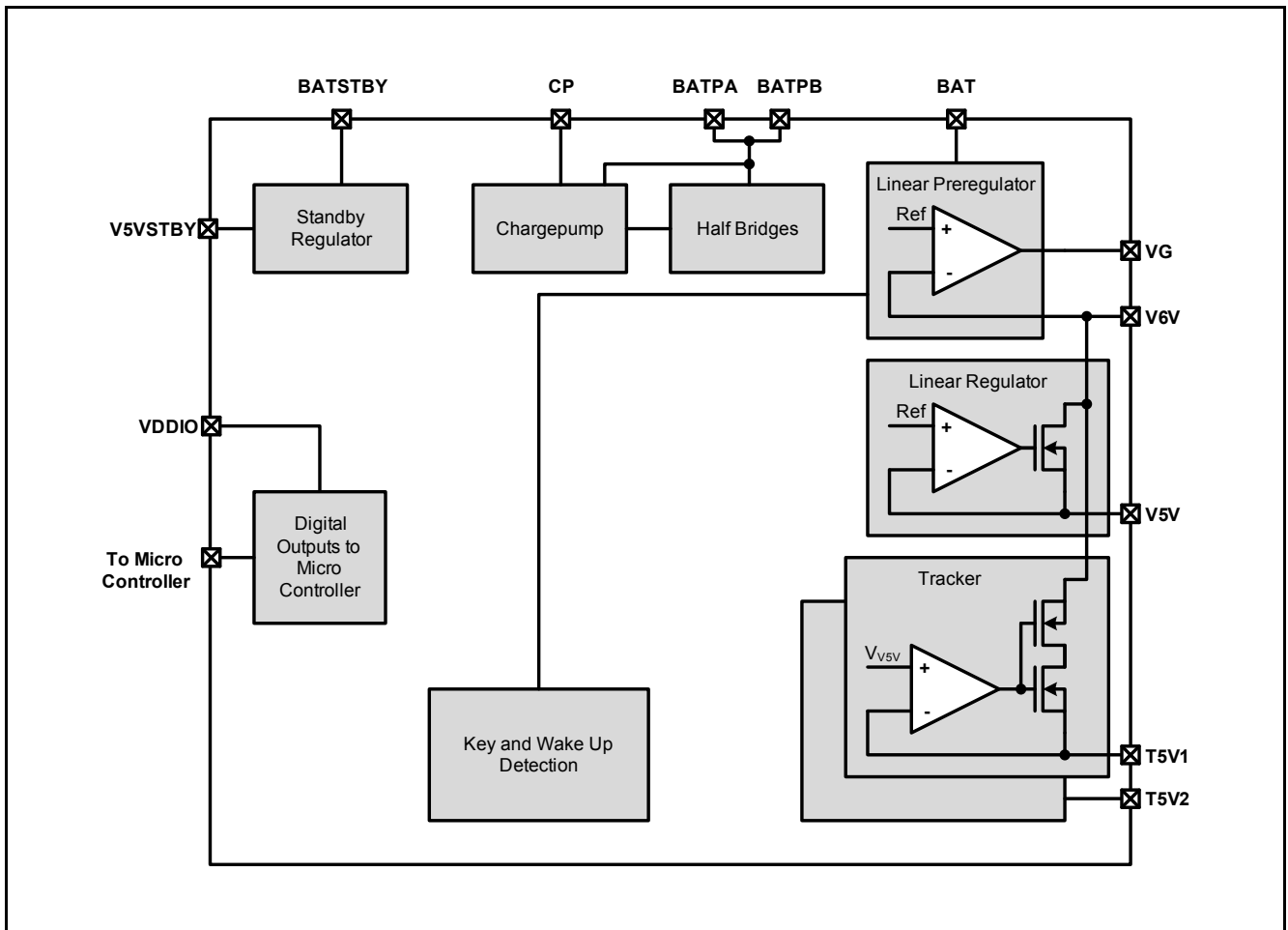


Figure 27 Block diagram of the power supply

8.1 Pre-Regulator

The pre-regulator uses an external logic level power MOSFET and regulates the voltage at pin $V6V$. The voltage at the pin is also the input voltage for the main supply of the ECU ($V5V$), the sensor supplies ($T5V1$, $T5V2$) and the internal supply. The circuit is designed for low drop operation.

It's not allowed to load the external MOSFET with anything else than $V6V$. The function of the pre-regulator is guaranteed with the MOSFET IPD30N06S2L-23 of Infineon.

8.2 5V Main Supply

The 5V main supply is designed to supply the ECU including micro controller and e.g. other power chips. Out of $V6V$ a high accurate voltage is provided at the pin $V5V$. The pin and the circuit is protected against overload and short circuit. For stabilization and ripple reduction an external buffer capacitor is required. For low drop operation of the regulator the pins $BATPA$ and $BATPB$ must be supplied.

8.3 Sensor Supply

There are two sensor supplies integrated providing an output voltage based on $V5V$ as reference. Out of $V6V$ a high accurate voltage is provided at the pins $T5V1$ and $T5V2$. The pins and the circuits are protected against overload, short circuit and reverse supply back to $V6V$. For stabilization and ripple reduction external buffer capacitors are required. For low drop operation of the regulator the pins $BATPA$ and $BATPB$ must be supplied.

8.4 IO Supply

The TLE8888-1QK provides an IO supply pin $VDDIO$ for 3.3V and 5V micro controller interfaces. This pin is used for the supply of the output driver and defines the output level of all logical interface pins.

8.5 Standby Supply

The TLE8888-1QK integrates a standby supply which is supplied by the pin $BATSTBY$ and provides a 5V output supply at pin $V5VSTBY$. It is not allowed to connect this pin to any other supply.

8.6 Charge Pump

There is a charge pump integrated to supply the half bridges out of $BATPA$ and $BATPB$. A capacitor has to be connected on the PCB (between CP and $BATPA/BATPB$) to buffer the voltage and reduce the ripple. It's not allowed to apply any external load to the pin CP .

8.7 Voltage Monitoring

The TLE8888-1QK provides voltage monitoring of the main ECU supply $V5V$, the sensor supplies $T5V1$ and $T5V2$ and the battery voltage. In [Chapter 5.2](#) the effect to the status of the TLE8888-1QK is described. All detection thresholds are implemented with a hysteresis and a filter time to suppress disturbances.

The status of the over- and under-voltage detection of BAT , $T5V1$ and $T5V2$ are available in the diagnosis resistor [Diag0](#) and the bits [BATOV](#), [T1UV](#), [T1OV](#), [T2UV](#) and [T2OV](#).

Under- and over-voltage of $V5V$ leads to a reset of the micro controller (see [Table 6](#) in [Chapter 5.2](#)). After release of the reset the cause of the reset is available in the status register [OpStat1](#) (bits [V5UVR](#) and [V5OVR](#)).

8.8 Electrical Characteristics Power Supply

Table 23 Electrical Characteristics Power Supply

$V_S=13.5V$, $V_{V5V}=5V$, $T_J=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
current consumption at pins $BATPA$, $BATPB$, BAT and $V6V$	$I_{BAT,sum}$	–	–	50	mA	static, all “off”, no PWM and MSC/SPI communication	P_8.8.1

Pre-Regulator

Table 23 Electrical Characteristics Power Supply (cont'd)
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pre-Driver Output Voltage $V6V$	V_{V6V}	5.5	6	6.5	V	with respect to $AGND$, with external MOS FET IPD30N06S2L-23	P_8.8.2
Gate Output Voltage VG	ΔV_{VG}	4	–	7.5	V	$V_{V6V}=5.5V$; $\Delta V_{VG}=V_{VG}-V_{V6V}$	P_8.8.3
Gate Output Voltage VG at low Supply	$\Delta V_{VG,l}$	1.7	–	–	V	$V_{BATPx}=4.5V$, $I_{VG}=1\mu A$; $\Delta V_{VG}=V_{VG}-V_{V6V}$	P_8.8.4
Buffer Capacitor at $V6V^{1)}$	C_{V6V}	1	20	1000	μF	^{2) 3)}	P_8.8.37
ESR of Buffer Capacitance at $V6V^{1)}$	ESR_{V6V}	0.01		2	Ω	for $C_{V6V}<15\mu F$, $f_{ESR}=10kHz$	P_8.8.38
ESR of Buffer Capacitance at $V6V^{1)}$	ESR_{V6V}	0.5		2	Ω	for $15\mu F<C_{V6V}<20\mu F$, $f_{ESR}=10kHz$	P_8.8.39
ESR of Buffer Capacitance at $V6V^{1)}$	ESR_{V6V}	1		2	Ω	for $20\mu F<C_{V6V}<1000\mu F$, $f_{ESR}=10kHz$	P_8.8.40
Buffer Capacitor at $VG^{1)}$	C_{VG}	–	4.7	15	nF	²⁾³⁾	P_8.8.41
ESR of Buffer Capacitance at $VG^{1)}$	ESR_{VG}	–	–	1	Ω	$f_{ESR}=10kHz$	P_8.8.42
5V Main Supply $V5V$							
Output Voltage $V5V$	V_{V5V}	4.9	–	5.1	V	$-5mA < I_{V5V} < -500mA$, with respect to $AGND$	P_8.8.5
Voltage Drop $V6V-V5V$ at low Supply	$V_{V5V,d}$	–	–	0.6	V	$I_{V5V}=-500mA$; $V_{BAT}=V_{BATPx}=V_{KEY}=V_{V6V}=4.5V$	P_8.8.6
Voltage Drop $V6V-V5V$ at low Supply and low temperature	$V_{V5V,d,CT}$	–	–	0.45	V	$T_j=-40^\circ C$; $I_{V5V}=-500mA$; $V_{BAT}=V_{BATPx}=V_{KEY}=V_{V6V}=4.5V^{1)}$	P_8.8.7
Current Limitation	$I_{V5V,lim}$	-1200	–	-500	mA	–	P_8.8.8
Buffer Capacitor at $V5V^{1)}$	C_{V5V}	0.1	10	220	μF	²⁾³⁾	P_8.8.9
ESR of Buffer Capacitance at $V5V^{1)}$	ESR_{V5V}	0.01		2	Ω	for $C_{V5V}<10\mu F$, $f_{ESR}=10kHz$	P_8.8.43
ESR of Buffer Capacitance at $V5V^{1)}$	ESR_{V5V}	0.1		2	Ω	for $10\mu F<C_{V5V}<47\mu F$, $f_{ESR}=10kHz$	P_8.8.44

Table 23 Electrical Characteristics Power Supply (cont'd)
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ESR of Buffer Capacitance at $V5V^{1)}$	ESR_{V5V}	0.5		2	Ω	for $47\mu F < C_{V5V} < 220\mu F$, $f_{ESR}=10kHz$	P_8.8.45

Sensor Supplies $T5V1$ and $T5V2$

Output voltage tracking accuracy	ΔV_{T5Vx}	-10	–	10	mV	$\Delta V_{T5Vx}=V_{V5V}-V_{T5Vx}$, $4V < V_{V5V} < 5.1V$, $V_{V6V} > 5.5V$, $V_{IGNx} \geq 0V$	P_8.8.10
Current Limitation	$I_{T5Vx,lim}$	-300	–	-100	mA		P_8.8.11
Buffer Capacitor at $T5V1$ and $T5V2^{1)}$	C_{T5Vx}	–	–	400	nF		P_8.8.12

IO Supply $VDDIO$

IO Supply Voltage Range	V_{VDDIO}	3	–	5.5	V	–	P_8.8.13
Current Consumption at pin $VDDIO$	I_{DDIO}	–	–	2	mA	$V_{VDDIO}=5V$, $INx=0V$, $CSN=LINTX=CANTX=5V$, MON and RST open ¹⁾	P_8.8.14

Standby Supply $V5VSTBY$

Output Voltage $V5VSTBY$	$V_{V5VSTBY}$	4.75	–	5.25	V	$-10\mu A < I_{V5VSTBY} < -15mA$	P_8.8.15
Total Standby Current Consumption at pins $BATSTBY$, BAT , $V6V$ and MR	I_{STBY}	–	–	120	μA	ECU sleep mode, $T_j=25^\circ C$, $I_{V5VSTBY}=0mA$, $V_{BATSTBY}=V_{BAT}=V_{MR}=13.5V$, $EOTEN=CANW$ $KEN=0V$	P_8.8.16
Buffer Capacitor at $V5VSTBY^{1)}$	$C_{V5VSTBY}$	27	100	270	nF	²⁾³⁾	P_8.8.46
ESR of Buffer Capacitance at $V5VSTBY^{1)}$	$ESR_{V5VSTBY}$	0.01	–	1	Ω		P_8.8.47

Charge Pump

Charge pump Output Voltage	ΔV_{CP}	4	5	7	V	$\Delta V_{CP}=V_{CP}-V_{BAT}$ no external load currents	P_8.8.17
Charge pump Output Voltage at low supply	ΔV_{CP}	3.5	–	–	V	$V_{BAT}=4.5V$ after start up, $\Delta V_{CP}=V_{CP}-V_{BATPx}$	P_8.8.18
Buffer Capacitor at $CP^{1)}$	C_{CP}	–	4.7	–	nF		P_8.8.19

Voltage Monitoring

Table 23 Electrical Characteristics Power Supply (cont'd)
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<i>V5V</i> Under Voltage Detection Threshold, decreasing	$V_{UV,V5V,dec}$	4.45	–	4.7	V	V_{V5V} decreasing	P_8.8.20
<i>V5V</i> Under Voltage Detection Threshold, increasing	$V_{UV,V5V,inc}$	4.45	–	4.8	V	V_{V5V} increasing	P_8.8.21
<i>V5V</i> Under Voltage Detection Hysteresis	$V_{Hys,UV,V5V}$	10	50	–	mV	–	P_8.8.22
<i>V5V</i> Under Voltage Filter Time	$t_{f,UV,V5V}$	5	10	15	μs	–	P_8.8.23
<i>T5V1</i> and <i>T5V2</i> Under Voltage Detection Threshold	$V_{UV,T5Vx,dec}$	4.45	–	4.7	V	V_{T5Vx} decreasing	P_8.8.24
<i>T5V1</i> and <i>T5V2</i> Under Voltage Detection Threshold	$V_{UV,T5Vx,inc}$	4.45	–	4.8	V	V_{T5Vx} increasing	P_8.8.25
<i>T5V1</i> and <i>T5V2</i> Under Voltage Detection Hysteresis	$V_{Hys,UV,T5Vx}$	10	50	–	mV	–	P_8.8.26
<i>T5V1</i> and <i>T5V2</i> Under Voltage Filter Time	$t_{f,UV,T5Vx}$	5	10	15	μs	–	P_8.8.27
<i>V5V</i> Over Voltage Detection Threshold	$V_{OV,V5V}$	5.2	–	5.6	V	V_{V5V} increasing	P_8.8.28
<i>V5V</i> Over Voltage Detection Hysteresis	$V_{Hys,OV,V5V}$	10	–	100	mV	–	P_8.8.29
<i>V5V</i> Over Voltage Filter Time	$t_{f,OV,V5V}$	5	10	15	μs	–	P_8.8.30
<i>T5V1</i> and <i>T5V2</i> Over Voltage Detection Threshold	$V_{OV,T5Vx}$	5.2	–	5.6	V	V_{T5Vx} increasing	P_8.8.31
<i>T5V1</i> and <i>T5V2</i> Over Voltage Detection Hysteresis	$V_{Hys,OV,T5Vx}$	10	–	100	mV	–	P_8.8.32
<i>T5V1</i> and <i>T5V2</i> Over Voltage Filter Time	$t_{f,OV,T5Vx}$	5	10	15	μs	–	P_8.8.33
<i>BAT</i> Over Voltage Detection Threshold	$V_{OV,BAT}$	28	–	30.4	V	V_{BAT} increasing	P_8.8.34
<i>BAT</i> Over Voltage Detection Hysteresis	$V_{Hys,BAT}$	50	–	500	mV	–	P_8.8.35
<i>BAT</i> Over Voltage Filter Time	$t_{f,OV,BAT}$	5	10	15	μs	–	P_8.8.36

1) not subject to production test, specified by design

2) Defined minimum value is needed for regulator stability. Application might need higher value than minimum.

 3) additionally in parallel a capacitance up to $0.1 \cdot C_{VxV}$ and low ESR is allowed

9 Power Stages

In the TLE8888-1QK there are 14 low side power stages, 4 half bridges, 4 push-pull outputs for on board and external ignition driver and 6 push-pull outputs for on board MOSFETs implemented. The 14 low side power stages are designed for various inductive and resistive loads, 4 stages to drive especially injectors, 3 with a higher operating current to drive e.g. O₂-heaters and 7 stages to drive relays.

For the injector output stages (*OUT1* to *OUT4*) the common enable input *INJEN* and for the ignition outputs the common enable input *IGNEN* are implemented. The half bridges can be used with high or low side load, with active or passive freewheeling or in full bridge configuration.

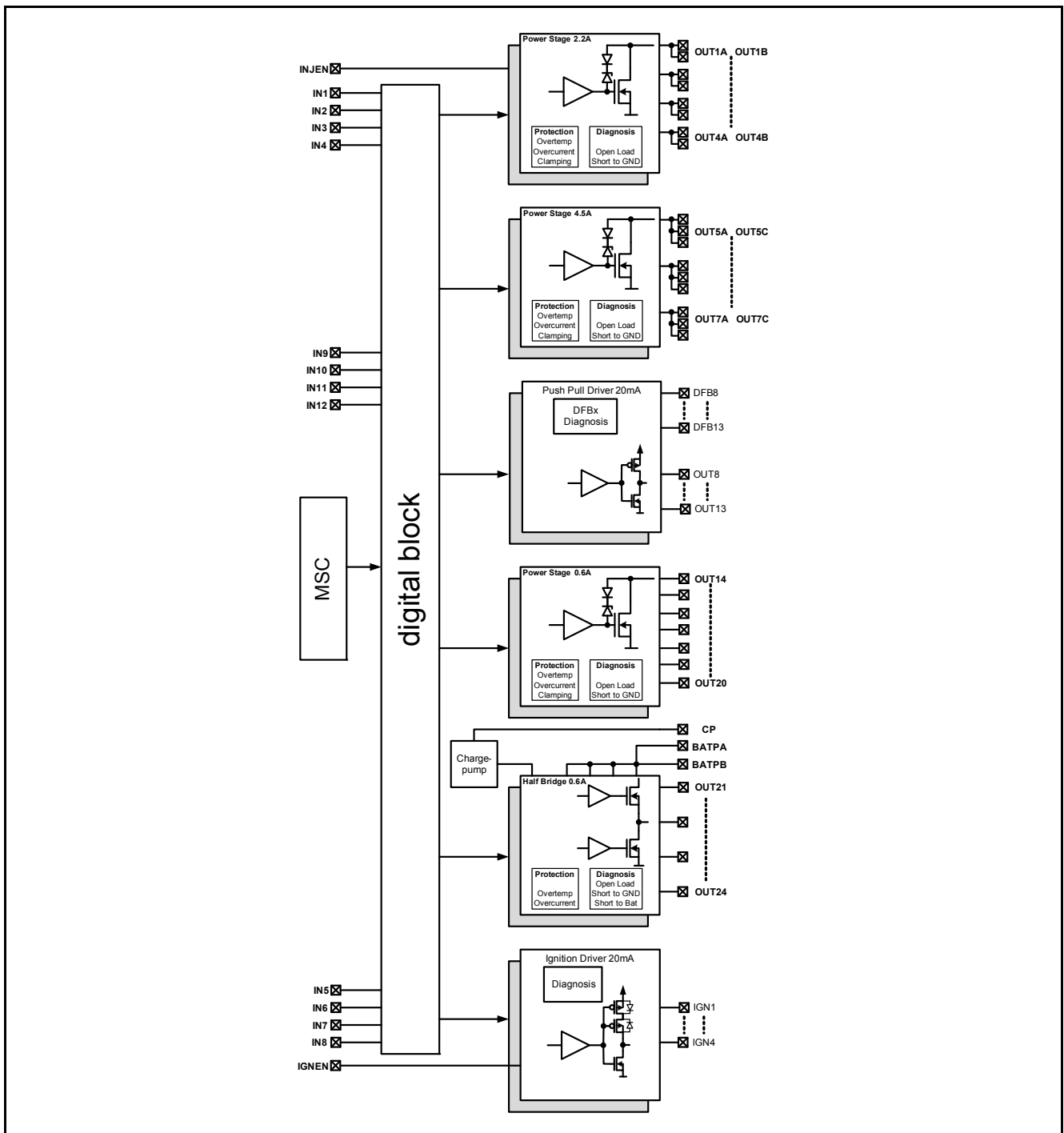


Figure 28 Block Diagram of the Power stages

Table 24 Overview Power Stages

	Type	maximum operation current	Ron	active clamping	Diagnosis in on	Diagnosis in off
<i>OUT1 to OUT4</i>	Low side switch	2.2A	550mΩ	yes	over current (short to battery) over temperature	open load short to GND over temperature
<i>OUT5 to OUT7</i>	Low side switch	4.5A	350mΩ	yes	over current (short to battery) over temperature	open load short to GND over temperature
<i>OUT8 to OUT13</i>	5V push pull output	20/-20mA	–	no	at pin DFBx: short to battery at pin OUTx: over voltage	at pin DFBx: open load short to GND at pin OUTx: over voltage
<i>OUT14 to OUT20</i>	Low side switch	0.6A	1.5Ω	yes	over current (short to battery) over temperature	open load short to GND over temperature
<i>OUT21 to OUT24</i>	Half bridge	0.6A	2.4Ω	no	over current (short to battery/short to GND) over temperature	open load short to battery/short to GND over temperature
<i>IGN1 to IGN4</i>	5V push pull output	20/-20mA	–	no	short to battery short to GND open load	short to battery

9.1 Power Stage Control

The output stages will be controlled either by the MSC/SPI data frame or command frame and the control register **Cont0** to **Cont3** (see [Chapter 14.6](#)) or the direct drive inputs *INI* to *INI2*. The configuration which control mode is active is done in the configuration register **DDConfig0** to **DDConfig3** (see [Chapter 14.5](#)).

A “1” in the control register/data frame bit or a “high” at the direct drive inputs switches on the corresponding output. In [Table 25](#) the assignment of the direct drive inputs to the output stages is shown. The set up is valid for MSC and SPI operation.

The status of the power stages is also affected by the operation state and conditions of the TLE8888-1QK and is described in [Chapter 5](#). All power stages are switched off if a micro channel time out occurs. Description of the effect to the control of the power stages see [Chapter 13.1.1, Downstream Supervisory Functions](#).

Table 25 Direct Drive Input Assignment to Output Stages

Input	Output	Note
<i>IN1</i> to <i>IN4</i>	<i>OUT1</i> to <i>OUT4</i>	configuration for direct drive: bits O1DD to O4DD of the configuration register DDConfig0 fix assignment of the inputs to the outputs
<i>IN5</i> to <i>IN8</i>	<i>IGN1</i> to <i>IGN4</i>	configuration for direct drive: bits IGN1DD to IGN4DD of the configuration register DDConfig3 fix assignment of the inputs to the outputs
<i>IN9</i> to <i>IN12</i>	<i>OUT5</i> to <i>OUT24</i>	configuration for direct drive: bits O5DD to O24DD of the configuration registers DDConfig0 to DDConfig2 assignment of input pins: configuration register InConfig0 to InConfig3 only 4 of this output stages can be switched directly

All direct drive inputs have implemented a pull down current source to define the input voltage. For a multiple assignment of two direct drive inputs for one output stage (wrong configuration) the output is switched off independent of the status of the direct drive inputs.

9.2 Power Stages Enable

To enable the power stages a central output enable bit **OE** is defined. The status of the bit is shown in the status register **OpStat1** and can be set with the command register **CmdOE**. Additionally a dedicated output enable bit for each output is defined (see register **OEConfig0** to **OEConfig3**) to avoid uncontrolled repetitive switching in failure case. These enable bits are reset by the protection function of each channel and block switch on of the channels. The bits could not be set if a protection function is active.

With setting the central enable bit to “1” all dedicated output enable bits are set to “1” (if no protection function is active) and all channels are enabled and can be controlled according their configuration.

With setting the central enable bit to “0” all dedicated output enable bits are set to “0” and all channels are disabled. For the injector channels *OUT1* to *OUT4* the common enable input *INJEN* must be set to “high” and for the ignition outputs *IGN1* to *IGN4* the common enable input *IGNEN* must be set to “high” to enable the channels.

Procedure to switch on after failure condition occurred:

- Read out of diagnosis bits
- Second read out to verify that the failure conditions are not remaining
- Set of the dedicated output enable bit of the affected channel if the diagnosis bit is not active anymore
- Switch on of the channel

Switch off during battery over voltage:

To protect the power stages against high energy during freewheeling they are switched off for battery voltages greater than the “**BAT Over Voltage Detection Threshold**” (see **Table 23** in **Chapter 8.8**).

9.3 Power Stages Configuration

The power stages can be configured according the configuration bits in the configuration registers **OutConfig0** to **OutConfig5**, **BriConfig0**, **BriConfig1** and **IGNConfig**. The direct drive input configuration is described in **Table 25**.

Table 26 Configuration Overview Power Stages

	Configuration	Configuration Register
<i>OUT1</i> to <i>OUT4</i>	over current: current limitation or switch off diagnosis in off: pull down current activated/deactivated	OutConfig0
<i>OUT5</i> to <i>OUT7</i>	over current: current limitation or switch off diagnosis in off: pull down current activated/deactivated	OutConfig1
<i>OUT8</i> to <i>OUT13</i>	at pin DFBx: diagnosis in off: pull down current activated/deactivated diagnosis in on: short to battery detection thresholds	OutConfig2 and OutConfig3 bits 0 to 3
<i>OUT14</i> to <i>OUT20</i>	mode set up: delayed switch off mode for <i>OUT17</i> over current: current limitation or switch off diagnosis in off: pull down current activated/deactivated (<i>OUT14</i> to <i>OUT17</i>) pull up and down current activated/deactivated (<i>OUT18</i> to <i>OUT20</i>)	OutConfig3 bits 4 and 5, OutConfig4 , OutConfig5
<i>OUT21</i> to <i>OUT24</i>	mode set up: active or passive freewheeling high or low side switch mode half or full bridge mode delayed switch off mode for <i>OUT21</i>	BriConfig0 and BriConfig1
<i>IGN1</i> to <i>IGN4</i>	open load in activation/deactivation open load current setting open load detection time	IGNConfig

9.4 Special Function “Delayed Switch Off” for *OUT17* and *OUT21*

A special set up for the control behavior of *OUT17* and *OUT21* is implemented. With the delayed switch off functionality the outputs are suited to drive loads (e.g. starter relay) which must be on during very low battery voltages even if the micro controller is in reset e.g. due to under-voltage. In this operation conditions all other power stages are normally switched off.

With the bits **O17D** in the configuration register **OutConfig4** and **O21D** in the configuration register **BriConfig1** both outputs can be configured to:

- normal control mode according description in **Chapter 9.1**
- delayed switch off mode

Note: For delayed switch off mode *OUT17* and *OUT21* must be configured as controlled by MSC/SPI (bits **O17DD/O21DD** in configuration register **DDConfig2** are set to “0”)

Delayed switch off mode for *OUT21* is only allowed in high or low side switch configuration. Fullbridge configuration is not allowed.

Note: The delayed switch off mode keeps the two outputs on for the time $t_{on,del}$ after an trigger event. With the trigger events in normal control mode the outputs are switched off.

In delayed switch off mode the delayed switch off timer starts with following trigger events:

Note: The channel must be on before a trigger event, switch on of all channels during the delayed switch off mode is not possible

- under-voltage of the main supply $V5V$ is detected
- or over-voltage of the main supply $V5V$ is detected
- or the MSC time out occurs
- or an active signal ("0") at pin MON
- or an active signal ("0") at pin RST

With the bit **RDOT** in the command register **Cmd0** the delayed switch off timer is restarted and the on time is increased.

The delayed off mode is terminated with following events:

- overflow of delayed off timer
- O17/O21 are switched off with command **CmdOE**, set control register bits **O17ON/O21ON** or the configuration register bits **O17E/O21E** to "0"
- **O17D/O21D** are set to "0"
- Ready State is active and no trigger event is active

The outputs are switched off immediately if an internal power on reset occurs. According to the definition in **Chapter 5.1** if the conditions for a state change to ECU sleep mode are fulfilled the delayed off is terminated and the transition is executed.

Normally the related register bits of $OUT17$ and $OUT21$ are reset during undervoltage of the main supply $V5V$ or an active signal ("0") at pin RST (definition see **Table 6** and **Table 7** in **Chapter 5.2**). In delayed switch off configuration following register bits are not reset:

- **OE** in status register **OpStat1**
- **O17E**, **O21E** in configuration register **OEConfig2**
- **O17D**, **O17OL**, **O17OC** in configuration register **OutConfig4**
- **O21F**, **O21M** in configuration register **BriConfig0**
- **O21D** in configuration register **BriConfig1**

For illustration in **Figure 29** and **Figure 30** two examples for the delayed switch off mode for are shown.

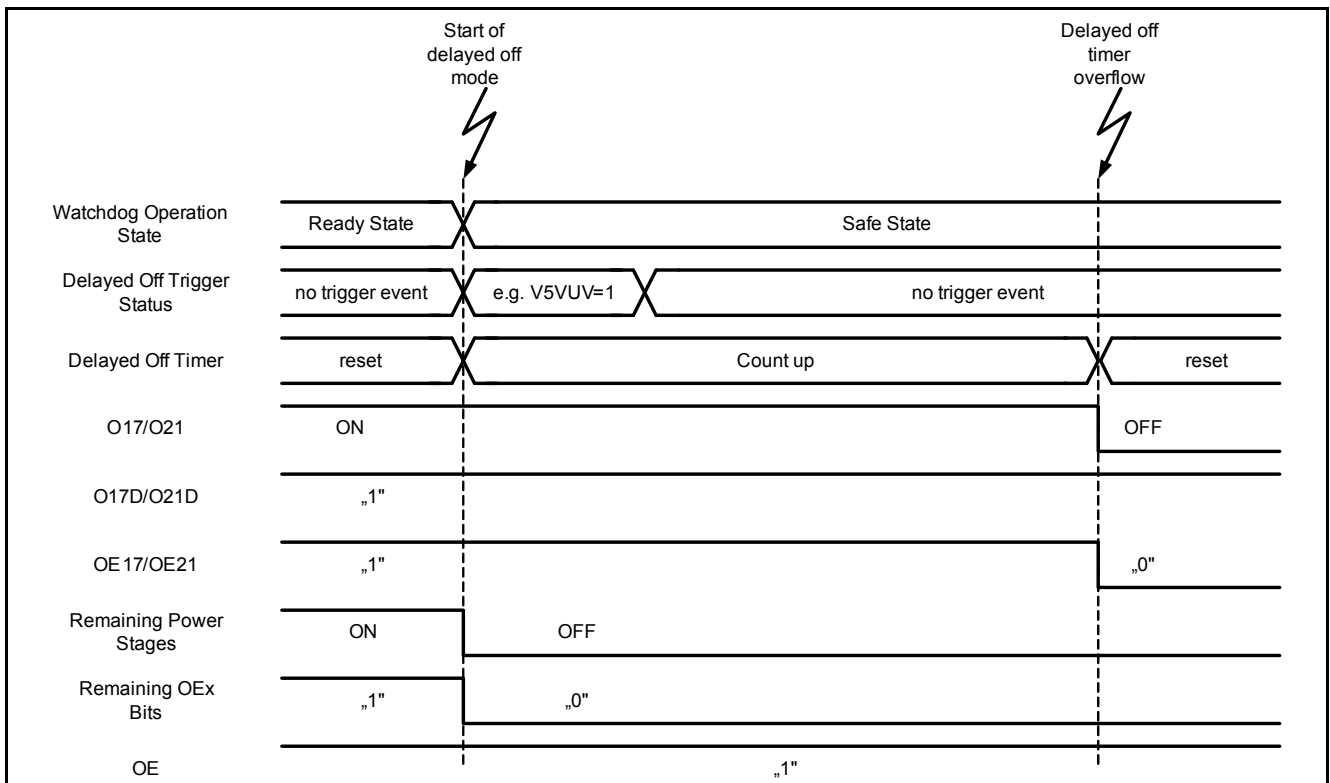


Figure 29 Example for Delayed Off Behavior: Overflow of Delayed Off Timer

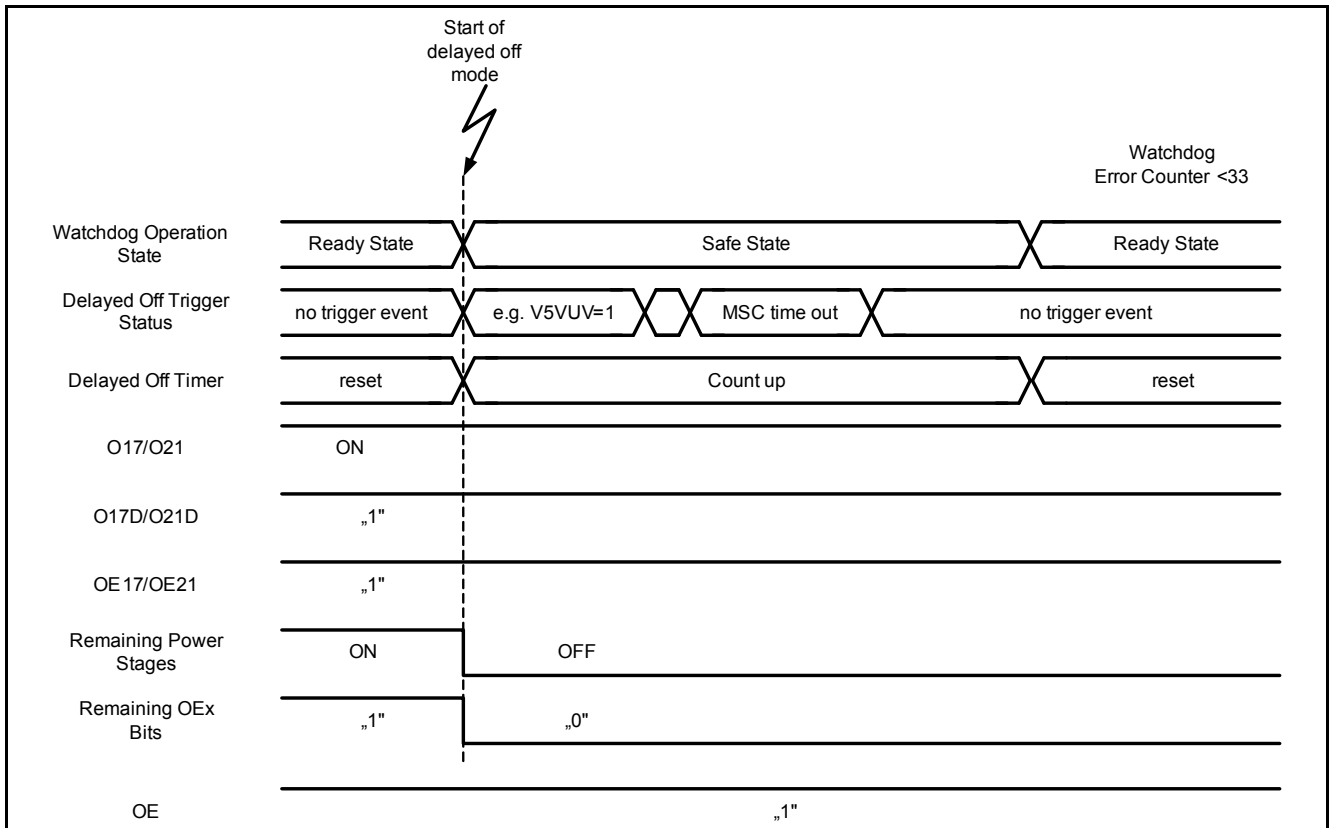


Figure 30 Example for Delayed Off Behavior: Stop of Delayed Off Timer with Ready State

9.5 Electrical Characteristics Direct Drive Inputs

Table 27 Electrical Characteristics Direct Drive Inputs

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Direct Drive Inputs <i>IN1</i> to <i>IN12</i>							
Low Level Input Voltage	$V_{IN,l}$	-0.3	–	0.9	V	–	P_9.5.1
High Level Input Voltage	$V_{IN,h}$	2	–	V_{VDDIO}	V	–	P_9.5.2
Input Voltage Hysteresis	$V_{IN,hys}$	50	200	–	mV	–	P_9.5.3
Pull Down Current	$I_{IN,pd}$	25	–	100	μA	$V_{IN}=V_{VDDIO}$	P_9.5.4
Pull Down Current	$I_{IN,pd}$	2.4	–	–	μA	$V_{IN}=0.6V$	P_9.5.5
Delayed Switch Off for <i>OUT17</i> and <i>OUT21</i>							
Switch On Time in Delayed Switch Off Mode	$t_{on,del}$	400	–	800	ms	–	P_9.5.6

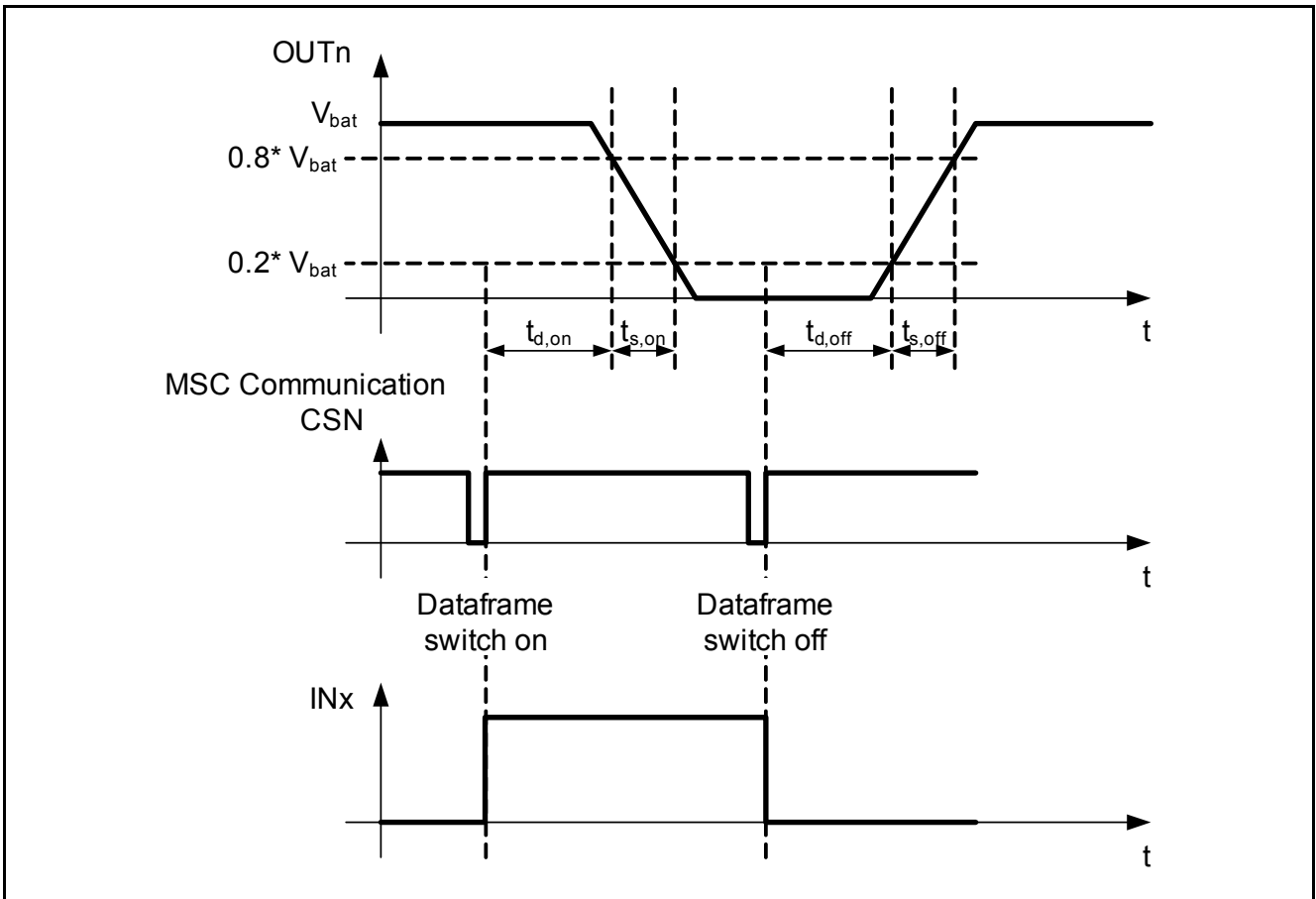


Figure 31 Switching Behavior

9.6 Low Side Switches *OUT1* to *OUT7* and *OUT14* to *OUT20*

The low side switches are designed to withstand repetitive clamping events which occurs in automotive applications. The outputs are fully protected and various diagnosis functions are implemented.

They are controlled and enabled like all power stages according the description in [Chapter 9.1](#) and [Chapter 9.2](#). To enable the low side switches *OUT1* to *OUT4* additionally the enable pin *INJEN* must be “high”.

The outputs are fully protected against over current and over temperature and various diagnosis functions are implemented. For the description of the diagnosis function see [Chapter 9.6.2](#).

All power stages are switched off if a micro channel time out occurs. Description of the effect to the control of the power stages see [Chapter 13.1.1, Downstream Supervisory Functions](#).

9.6.1 Protection of *OUT1* to *OUT7* and *OUT14* to *OUT20*

The outputs are fully protected against over current and over temperature.

The current protection of the power stages *OUT1* to *OUT7* and *OUT14* to *OUT20* can be configured to current limitation or switch off in case of over current (configuration register [OutConfig0](#), [OutConfig1](#), [OutConfig3](#) to [OutConfig5](#) bits [O10C](#) to [O70C](#) and [O140C](#) to [O200C](#)). In failure case (e.g. short to battery) the output current of the low side switches are always limited and an over current condition is detected if the over current signal is valid longer than the “[Over-current Detection Filter Time](#)”. With the detection the corresponding diagnosis bits are set according the priority shown in [Table 28](#) and for switch off configuration additionally the output is switched off.

To cover all failure conditions the over temperature protection is implemented. Especially for the over current limitation configuration the over temperature is the only protection function against over load. After exceeding the temperature threshold the outputs are switched off till the temperature is decreased by the “[Over Temperature Hysteresis](#)”.

For the procedure to switch on an affected channel after failure condition see [Chapter 9.2](#).

9.6.2 Diagnosis of *OUT1* to *OUT7* and *OUT14* to *OUT20*

For the low side outputs various diagnosis function are implemented. For short to battery in on diagnosis the protection function over current and over temperature are used to set the diagnosis information and for open load and short to GND (SCG) in off a special circuit is implemented.

To detect the open load/short to GND a push pull circuits is active which leads to the function of the voltage and currents of the outputs shown in [Figure 32](#). With the defined detection threshold the load condition can be detected.

With the off signal of the output stage the open load/short to GND detection circuit is enabled. To suppress disturbances the output of the detection circuit is stored in the diagnosis register [OutDiag0](#) to [OutDiag4](#) after the “[Diagnosis Filter Time for open load and short to GND in off](#)” $t_{diag,f}$ and according the priority shown in [Table 28](#). With the readout of the diagnosis register the content is updated to the actual diagnosis.

For the outputs *OUT1* to *OUT7* and *OUT14* to *OUT17* the diagnosis pull down current of the open load/short to GND in off detection could be switched off (see configuration register [OutConfig1](#) to [OutConfig4](#)). With deactivated pull down current open load in off detection is not active and the diagnosis information 10_B will never occur and is deactivated. With deactivated pull down current the short to GND detection is active.

For the outputs *OUT18* to *OUT20* the diagnosis pull up and down currents could be switched off (bits [O18OL](#) and [O20OL](#) in configuration register [OutConfig5](#)). In this case no diagnosis information in off is active and the bits [O18DIAG1](#), [O19DIAG1](#) and [O20DIAG1](#) are “0”.

In [Figure 32](#) the behavior open load/short to GND in off detection of the output current as a function of the output voltage is shown.

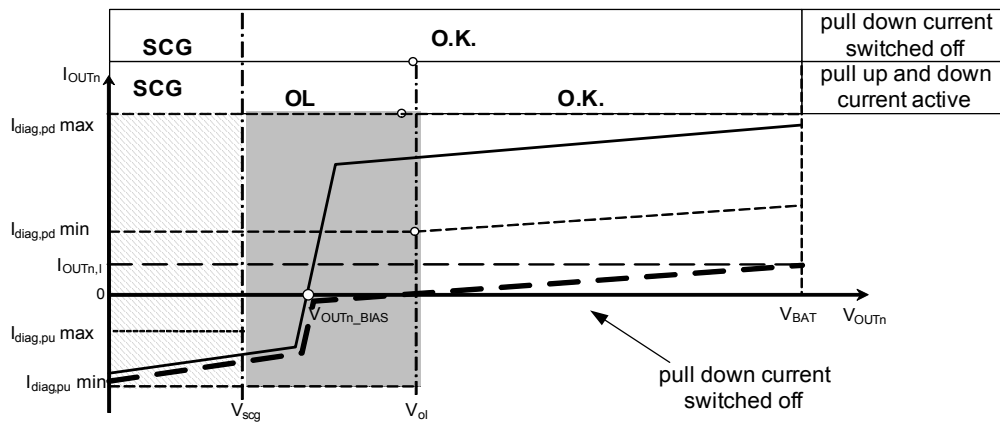


Figure 32 Output behavior with active diagnosis in off

Table 28 Description of Diagnosis Information

OnDIAG[1:0]	Priority (1 = highest priority)	Description
00	4	no failure
01	1	short circuit to battery (over current) or over temperature
10	2	open load in off ^{1) 2)}
11	3	short circuit to ground in off ²⁾

1) no open load in off detection with deactivated pull down current

2) no open load and short to GND in off signalization for *OUT18* to *OUT20* if pull up and down currents are switched off

9.6.3 Electrical Characteristics Low Side Switches *OUT1* to *OUT7* and *OUT14* to *OUT20*

Table 29 Electrical Characteristics Low Side Switches *OUT1* to *OUT7* and *OUT14* to *OUT20*

$V_S=13.5V$, $V_{VS}=5V$, $T_j=-40$ to $150^{\circ}C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
OUT1...4, n=1 to 4							
Operation Current	I_{OUTn}	–	–	2.2	A		P_9.6.1
Limitation Current in Over-current condition	$I_{OUTn,lim}$	2.2	–	4	A		P_9.6.2
Over-current Detection Filter Time	$t_{oc,f}$	40	–	70	μs		P_9.6.3
On Resistance	$R_{OUTn,on}$		–	550	m Ω	$I_{OUTn}=2.2A$	P_9.6.4
Clamping Voltage	$V_{OUTn,cv}$	50	–	60	V	$I_{OUTn}=0.2A$	P_9.6.5

Table 29 Electrical Characteristics Low Side Switches *OUT1* to *OUT7* and *OUT14* to *OUT20*
 (cont'd)

 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Repetitive Clamping Energy	$E_{OUTn,cl}$	–	–	4	mJ	$I_{OUTn}<1.4A$, $T_j=125^\circ C$, $648*10^6$ cycles ¹⁾	P_9.6.6
Leakage Current 1	$I_{OUTn,l,1}$	–	–	5	μA	$V_{OUTn}=13.5V$, $V_{BAT}=0V$, $T_j=60^\circ C$ ¹⁾²⁾	P_9.6.7
Leakage Current 2	$I_{OUTn,l,2}$	–	–	10	μA	$V_{OUTn}=28V$, $V_{BAT}=0V$, $T_j=60^\circ C$ ¹⁾²⁾	P_9.6.8
Leakage Current 3	$I_{OUTn,l,3}$	–	–	20	μA	$V_{OUTn}<28V$, $V_{BAT}=0V$, $T_j=150^\circ C$ ²⁾	P_9.6.9
Turn On Delay Time	$t_{d,on}$	1	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.10
Turn Off Delay Time	$t_{d,off}$	1	–	8	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.11
Switch On Time	$t_{s,on}$	1.8	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.12
Switch Off Time	$t_{s,off}$	1.8	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.13

OUT5...7, n=5 to 7

Operation Current	I_{OUTn}	–	–	4.5	A		P_9.6.14
Limitation Current in Over-current condition	$I_{OUTn,lim}$	4.5	–	8	A		P_9.6.15
Over-current Detection Filter Time	$t_{oc,f}$	40	–	70	μs		P_9.6.16
On Resistance	$R_{OUTn,on}$		–	350	m Ω	$I_{OUTn}=3A$	P_9.6.17
Clamping Voltage	$V_{OUTn,cv}$	50	–	60	V	$I_{OUTn}=0.2A$	P_9.6.18
Repetitive Clamping Energy	$E_{OUTn,cl}$	–	–	22	mJ	$I_{OUTn}<1.05A$, $T_j=125^\circ C$, $1*10^9$ cycles ¹⁾	P_9.6.19
Leakage Current 1	$I_{OUTn,l,1}$	–	–	5	μA	$V_{OUTn}=13.5V$, $V_{BAT}=0V$, $T_j=60^\circ C$ ¹⁾²⁾	P_9.6.20
Leakage Current 2	$I_{OUTn,l,2}$	–	–	10	μA	$V_{OUTn}=28V$, $V_{BAT}=0V$, $T_j=60^\circ C$ ¹⁾²⁾	P_9.6.21
Leakage Current 3	$I_{OUTn,l,3}$	–	–	30	μA	$V_{OUTn}<28V$, $V_{BAT}=0V$, $T_j=150^\circ C$ ²⁾	P_9.6.22

Table 29 Electrical Characteristics Low Side Switches *OUT1* to *OUT7* and *OUT14* to *OUT20*
 (cont'd)

 $V_S=13.5V$, $V_{SV}=5V$, $T_j=-40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn On Delay Time	$t_{d,on}$	1	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.23
Turn Off Delay Time	$t_{d,off}$	1	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.24
Switch On Time	$t_{s,on}$	1.4	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.25
Switch Off Time	$t_{s,off}$	1.4	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=2.2A$, resistive load ³⁾	P_9.6.26

OUT14...20, n=14 to 20

Operation Current	I_{OUTn}	–	–	0.6	A		P_9.6.27
Limitation Current in Over-current condition	$I_{OUTn,lim}$	0.6	–	1.5	A		P_9.6.28
Over-current Detection Filter Time	$t_{oc,f}$	40	–	70	μs		P_9.6.29
On Resistance	$R_{OUTn,on}$		–	1.5	Ω	$I_{OUTn}=0.6A$	P_9.6.30
<i>OUT17</i> On Resistance at Low Battery Voltage	$R_{OUT17,on,l}$		–	1.7	Ω	$I_{OUTn}=0.1A$, $V_{BATPx}=4.5V$	P_9.6.31
Clamping Voltage	$V_{OUTn,cv}$	50	–	60	V	$I_{OUTn}=0.2A$	P_9.6.32
Repetitive Clamping Energy	$E_{OUTn,cl}$	–	–	6.5	mJ	$I_{OUTn}<0.3A$, $T_j=125^\circ\text{C}$, $40 \cdot 10^6$ cycles ¹⁾	P_9.6.33
Leakage Current 1	$I_{OUTn,l,1}$	–	–	5	μA	$V_{OUTn}=13.5V$, $V_{BAT}=0V$, $T_j=60^\circ\text{C}^{1)2)}$	P_9.6.34
Leakage Current 2	$I_{OUTn,l,2}$	–	–	15	μA	$V_{OUTn}=28V$, $V_{BAT}=0V$, $T_j=60^\circ\text{C}^{1)2)}$	P_9.6.35
Leakage Current 3	$I_{OUTn,l,3}$	–	–	35	μA	$V_{OUTn}=28V$, $V_{BAT}=0V$, $T_j=150^\circ\text{C}^{2)}$	P_9.6.36
Turn On Delay Time	$t_{d,on}$	1	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=0.3A$, resistive load ³⁾	P_9.6.37
Turn Off Delay Time	$t_{d,off}$	1	–	7	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=0.3A$, resistive load ³⁾	P_9.6.38
Switch On Time	$t_{s,on}$	1.1	–	5.6	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=0.3A$, resistive load ³⁾	P_9.6.39

Table 29 Electrical Characteristics Low Side Switches *OUT1* to *OUT7* and *OUT14* to *OUT20*
 (cont'd)

 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Switch Off Time	$t_{s,off}$	1.1	–	5.6	μs	$V_{OUTn}=13.5V$, $I_{OUTn}=0.3A$, resistive load ³⁾	P_9.6.40
Delayed Off Time after trigger event for <i>OUT17</i>	$t_{off,del}$	400	–	800	ms		P_9.6.41

Diagnosis *OUT1* to 7 and *OUT14* to 20

Over Temperature Switch Off Threshold	$T_{OUTn,ot}$	150	–	200	$^\circ\text{C}$	1)	P_9.6.42
Over Temperature Hysteresis	$T_{OUTn,ot,hys}$	–	10	–	$^\circ\text{C}$	1)	P_9.6.43
Open Load in Off Detection Threshold	V_{ol}	$V5V-0.15$	$V5V$	$V5V+0.15$	V		P_9.6.44
Short to GND in Off Detection Threshold	V_{scg}	$0.6*V5V-0.15$	$0.6*V5V$	$0.6*V5V+0.15$	V		P_9.6.45
Diagnosis Pull Up Current	$I_{diag,pu}$	-270	–	-150	μA	$V_{OUTn}=0V$, $V_{IGNx}\geq 0V$	P_9.6.46
Diagnosis Pull Down Current	$I_{diag,pd}$	280	–	500	μA	$V_{ol}<V_{OUTn}<V_{BAT}$, $V_{IGNx}\geq 0V$	P_9.6.47
Diagnosis Filter Time for open load and short to GND in off	$t_{diag,f}$	60	–	135	μs		P_9.6.48

Direct Drive Inputs *INJEN*

Low Level Input Voltage	$V_{IN,l}$	-0.3	–	0.9	V		P_9.6.49
High Level Input Voltage	$V_{IN,h}$	2	–	V_{VDDIO}	V		P_9.6.50
Input Voltage Hysteresis	$V_{IN,hys}$	50	200	–	mV		P_9.6.51
Pull Down Current	$I_{IN,pd}$	25	–	100	μA	$V_{IN}=V_{VDDIO}$	P_9.6.52
Pull Down Current	$I_{IN,pd}$	2.4	–	–	μA	$V_{IN}=0.6V$	P_9.6.53

1) Parameter is not subject of production test, specified by design

 2) additionally diagnosis currents are active in operation mode; exception *OUT18* to *OUT20* in diagnosis current switch off configuration

 3) see [Figure 31](#)

9.7 Half Bridges *OUT21* to *OUT24*

The TLE8888-1QK integrates 4 half bridges which can be used as half bridge, full bridge, low side power stage or high side power stage. They are fully protected against overload and over-temperature and diagnosis fits to the chosen setup of the load. For the description of the diagnosis function see [Chapter 9.7.2](#).

They are controlled and enabled like all power stages according the description in [Chapter 9.1](#) and [Chapter 9.2](#). In [Table 30](#) the effect of [O21E](#) to [O24E](#) and [O21ON](#) to [O24ON](#) to the high side and low side switch of the half bridge is shown.

The half bridges can be configured via MSC/SPI for high or low side loads (setup see [Figure 33](#)) and for passive or active freewheeling (freewheeling is done with bulk diode or actively with switching on the freewheeling path). In [Table 30](#) the configuration is shown. With the bits [O21M](#) to [O24M](#) of the configuration register [BriConfig0](#) the switching mode is defined. With this configuration the low or the high side transistor is defined to switch on the load. For low side switch mode the load is connected to the battery, for high side switch mode the load is connected to GND (see [Figure 33](#)). With the bits [O21F](#) to [O24F](#) of the configuration register [BriConfig0](#) the freewheeling behavior is defined. The freewheeling is done for low side switch mode with the high side transistors. For passive freewheeling the bulk diode is used and the freewheeling transistor is always off. For the active freewheeling mode the freewheeling transistor is on during an off signal. This is the so called half bridge mode. The alternate switching of the high side and low side switch is done with a break before make phase. The definition of the switching mode is important for the correct diagnosis in off (see [Chapter 9.7.2](#)). The bits [FB1E](#) and [FB2E](#) (full bridge enable) are only used for the diagnosis in off for full bridge set up. [FB1E](#) = "1" is used for loads connected between *OUT21* and *OUT22*. [FB2E](#) = "1" is used for loads connected between *OUT23* and *OUT24*. The diagnosis in off setup is changed to the special situation of full bridge mode. The setting with [O21M](#) to [O24M](#) and [O21F](#) to [O24F](#) are valid.

Note: for full bridge set up the same set up for the two half bridges is recommended!

Table 30 Configuration of the Half Bridge

OnM ¹⁾	OnF ¹⁾	OnE ¹⁾	OnON=1 ¹⁾	OnON=0 ¹⁾	Description
0	0	0	high side =off low side = off	high side =off low side = off	low side switch mode and passive freewheeling at high side: ²⁾ both switches are disabled
0	0	1	high side =off low side = on	high side =off low side = off	low side switch mode and passive freewheeling at high side: ²⁾ high side switch always off, bulk diode of high side switch is used for passive freewheeling
0	1	0	high side =off low side = off	high side =off low side= off	low side switch mode and active freewheeling at high side: ²⁾ both switches are disabled
0	1	1	high side =off low side = on	high side =on low side= off	low side switch mode and active freewheeling at high side: ²⁾ high side switch on during freewheeling
1	0	0	high side =off low side= off	high side =off low side= off	high side switch mode and passive freewheeling at low side: ²⁾ both switches are disabled
1	0	1	high side =on low side= off	high side =off low side= off	high side switch mode and passive freewheeling at low side: ²⁾ low side switch always off, bulk diode of low side switch is used for passive freewheeling

Table 30 Configuration of the Half Bridge (cont'd)

OnM ¹⁾	OnF ¹⁾	OnE ¹⁾	OnON=1 ¹⁾	OnON=0 ¹⁾	Description
1	1	0	high side =off low side= off	high side =off low side= off	high side switch mode and active freewheeling at low side: ²⁾ both switches are disabled
1	1	1	high side =on low side= off	high side =off low side= on	high side switch mode and active freewheeling at low side: ²⁾ low side switch on during freewheeling

1) n=21 to 24 for the selected half bridge channel

2) setup definition see [Figure 33](#)

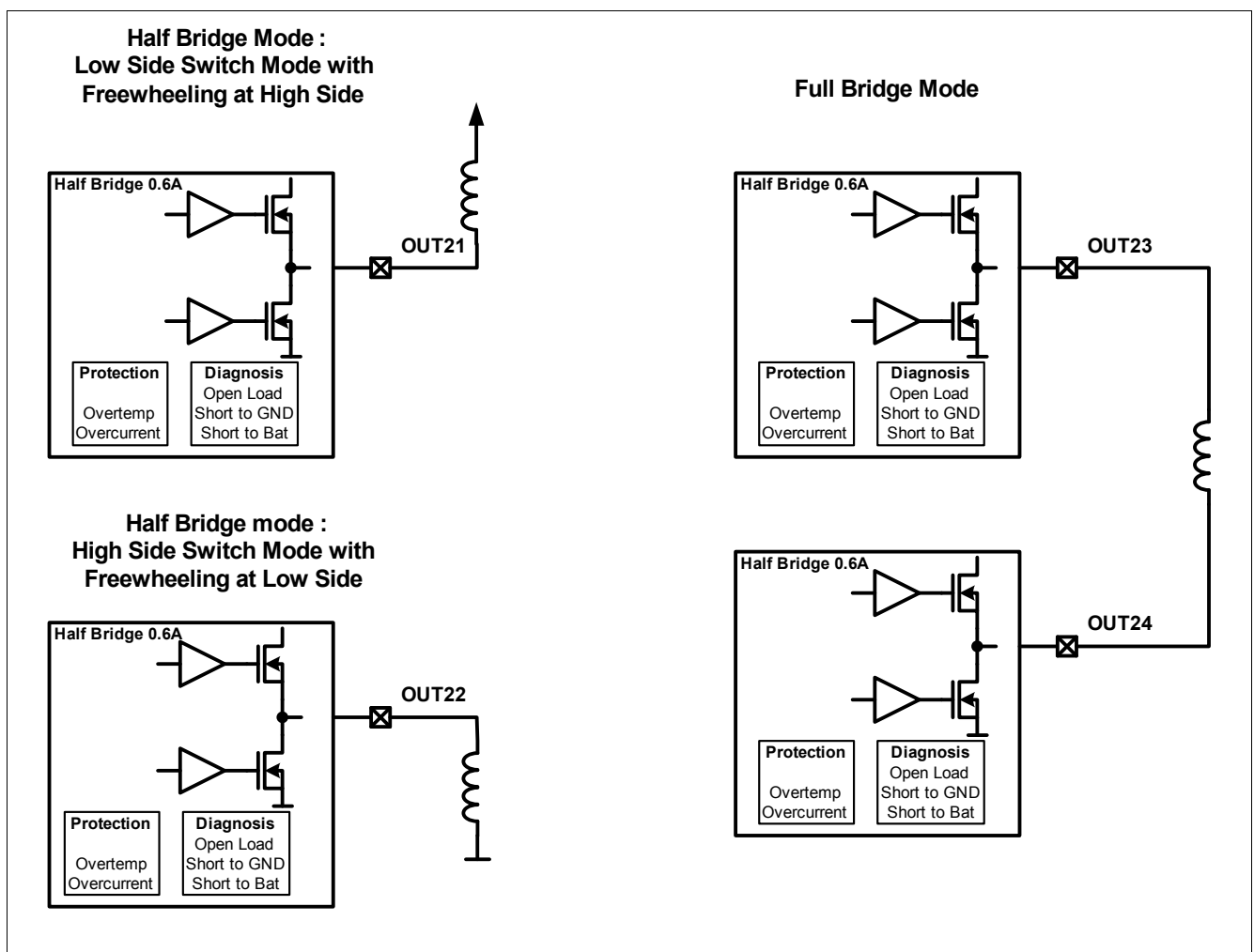


Figure 33 Load setups for half and full bridge mode

9.7.1 Protection of Half Bridges *OUT21* to *OUT24*

The half bridge outputs are fully protected against over-current and over-temperature.

In failure case (e.g. short to GND) the affected transistor is switched off after the “**Over-current Switch Off Filter Time**” and the diagnosis bit is set. The half bridge output is high ohmic (tristate).

To cover all failure conditions the over temperature protection is implemented. After exceeding the temperature threshold the half bridge outputs are switched off till the temperature is decreased by the “**Over Temperature**”

Hysteresis”.

For the procedure to switch on an affected channel after failure condition see [Chapter 9.2](#).

9.7.2 Diagnosis of Half Bridges *OUT21* to *OUT24*

For the half bridge outputs various diagnosis function are implemented. For short to battery and short to GND in on diagnosis the protection function over current is used (diagnosis bits **O21OC** to **O24OC** in diagnosis register **BriDiag1**). Over temperature is signalized with the diagnosis bits **B1OT** and **B2OT** in diagnosis register **BriDiag1**. For open load and short to GND (SCG) in off a special circuit is implemented. The diagnosis bits **O21DIA** to **O24DIA** in diagnosis register **BriDiag0** are set according the setup of the channels and according the priority shown in [Table 31](#).

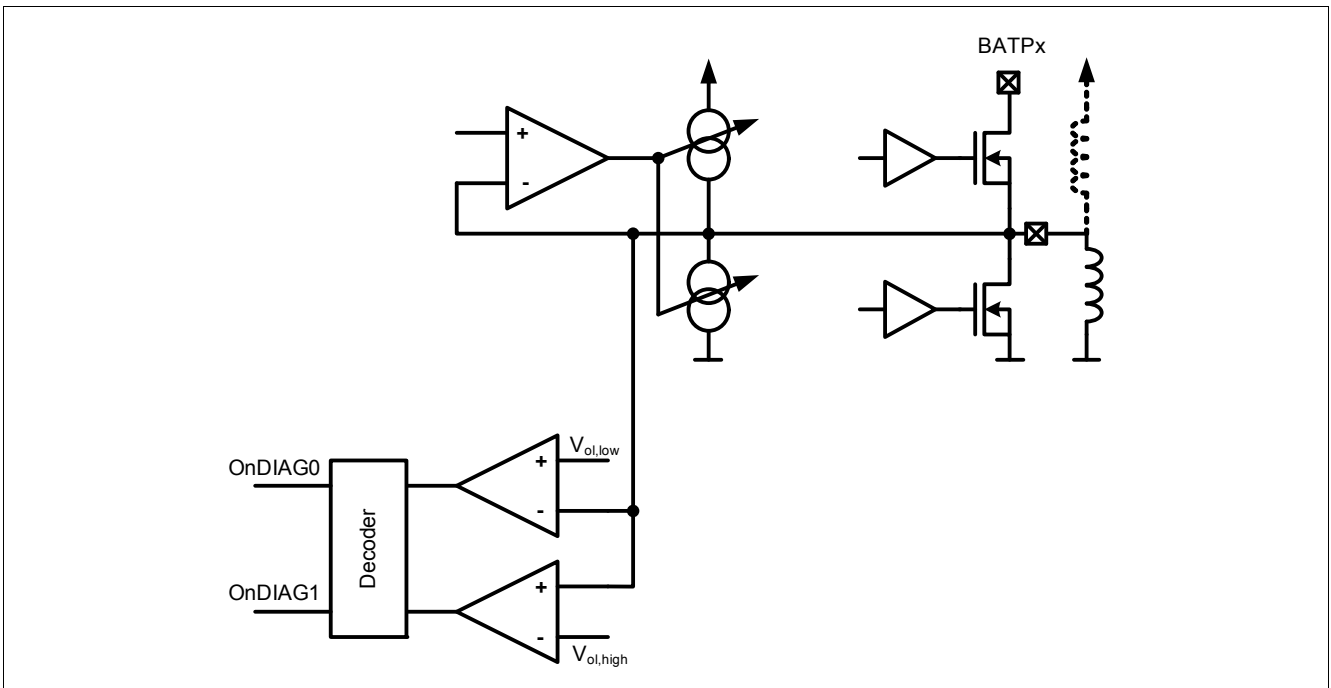


Figure 34 Open Load and Short to GND/Battery Detection Circuit for Half Bridge Configuration (Low or High Side Load)

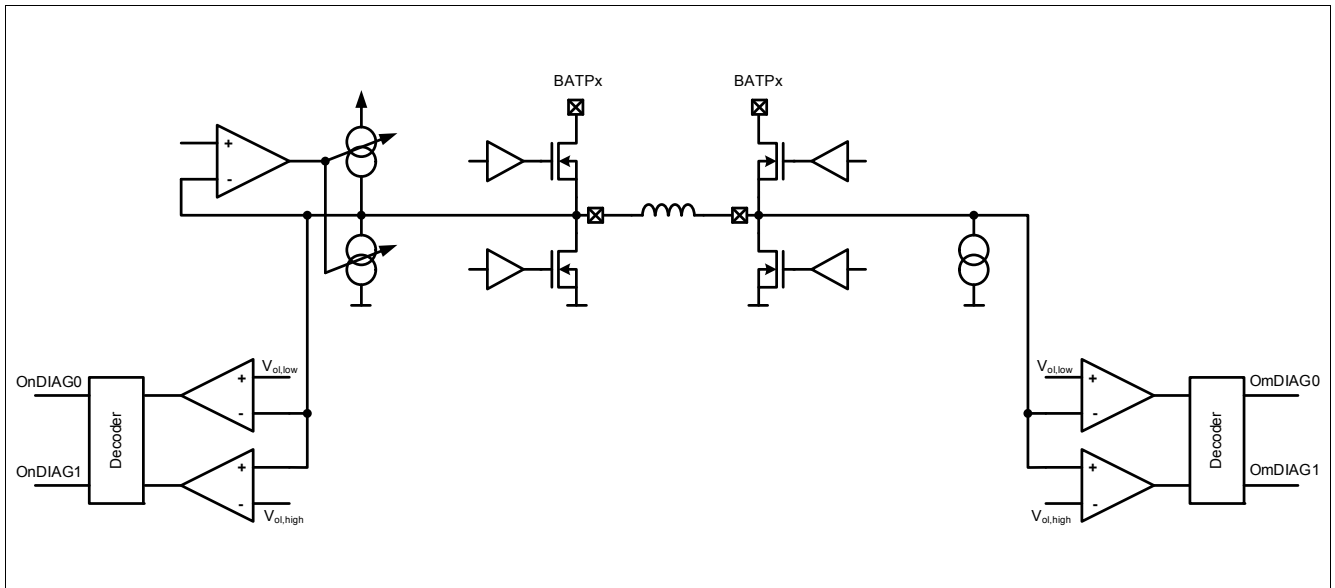


Figure 35 Open Load and Short to GND/Battery Detection Circuit for Full Bridge Configuration

In **Figure 36** and **Figure 37** the behavior of the output current as a function of the output voltage in the different configurations are shown.

The detection in off for open load is the same for both settings but for the short detection there is a difference for low side and high side switch mode.

- High side switch mode: short to battery detection in off
- Low side switch mode: short to GND detection in off

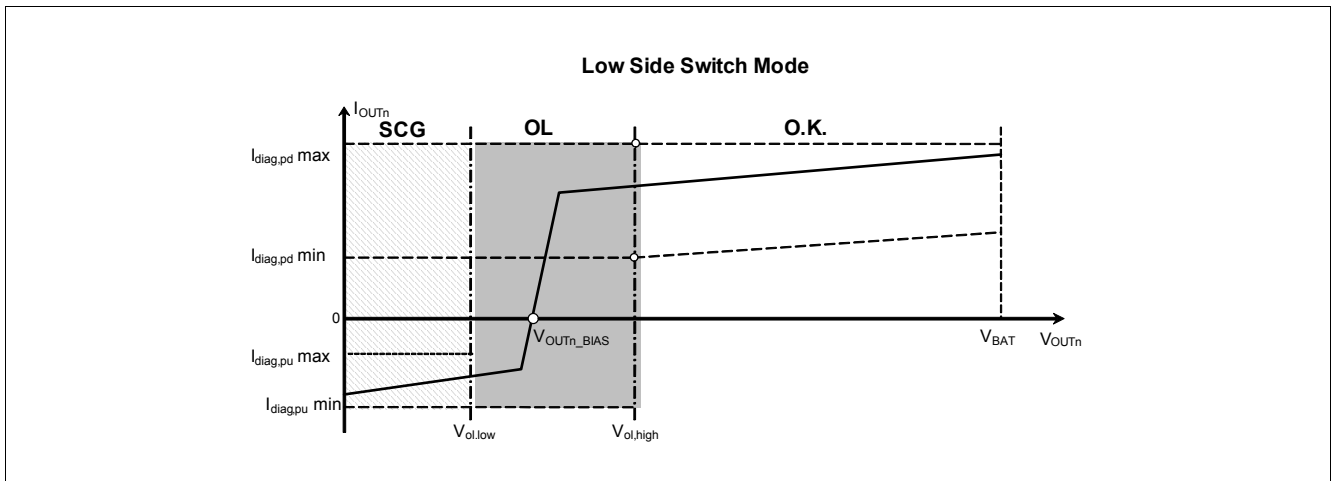


Figure 36 Output Behavior in Off for Low Side Switch Configuration with Open Load and Short to GND Detection

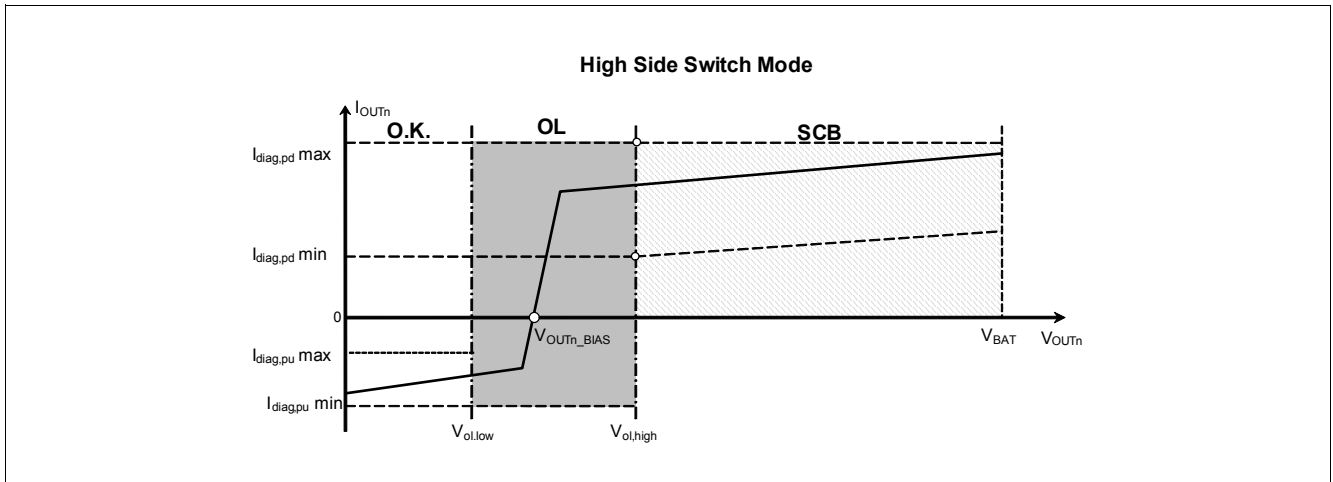


Figure 37 Output Behavior in Off for High Side Switch Configuration with Open Load and Short to Battery Detection

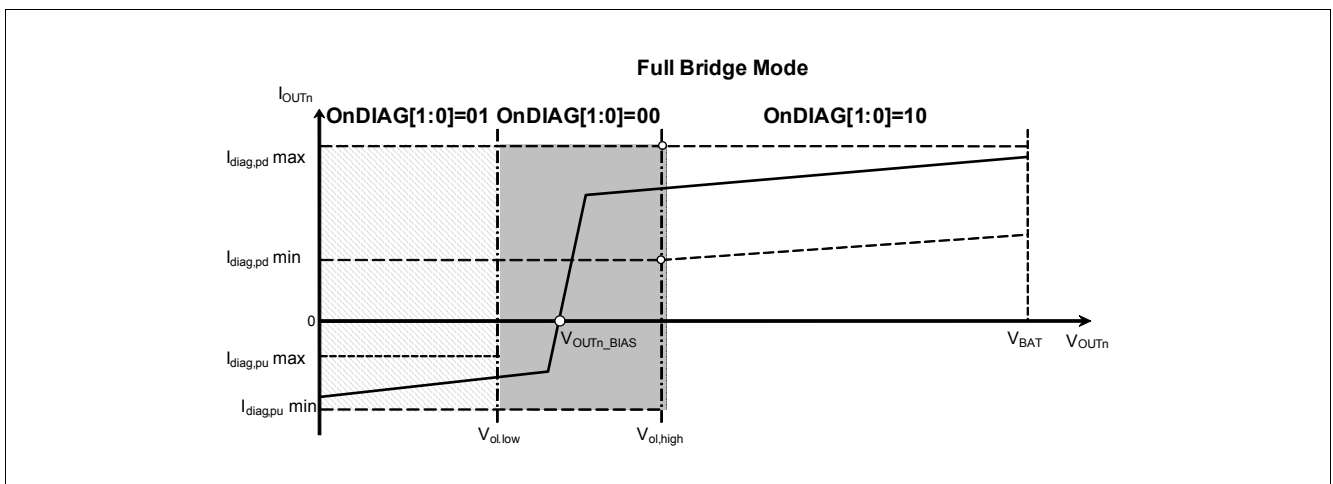


Figure 38 Output Behavior in Off for Full Bridge Mode Configuration

The detection is active if the high side and the low side switch are off and the diagnosis activation timer $t_{br,diag,act}$ starts counting. For activation of the open load in off detection in active freewheeling configuration the half bridge must be disabled by setting the bits **O21E** to **O24E** of configuration register **OEConfig2** to “low”, for passive freewheeling a normal off signal (**IN9** to **IN12** or **O21ON** to **O24ON** in control register **Cont2** is set to “low”) is sufficient. For full bridge mode both half bridges must be off or disabled regarding the setting of the half bridge. After the **Bridge Diagnosis Activation Time** $t_{br,diag,act}$ the output of the detection circuit is stored in the diagnosis register **BriDiag0** according the priority shown in **Table 31**. After activation of the open load in off detection a filter time $t_{br,diag,f}$ to suppress disturbances is implemented. The diagnosis register bits are set after the specified filter times. With the readout of the diagnosis register the content is updated to the actual diagnosis.

In **Table 31** the definition of the diagnosis bits for single switch usage is defined, in **Table 32** the definition for full bridge mode.

Note: especially for full bridge mode it is recommended to read out the diagnosis register twice due to transition states and possible misleading diagnosis register entries

Table 31 Description of Diagnosis Information Single Switch Usage

OnDIAG[1:0] ¹⁾	Priority (1 = highest priority)	High Side Switch Mode	Low Side Switch Mode
00	3	no failure	no failure
01	2	open load in off	n.a.
10	2	n.a.	open load in off
11	1	short circuit to battery in off	short circuit to ground in off

1) n from 21 to 24

Note: For high side switch mode (low side load) after start up there will be a short to ground detection before the output is configured to high side load and the diagnosis bits are set to "11". This detection is not right and it is recommended to read out the diagnosis registers twice after start up to avoid wrong diagnosis information.

Table 32 Description of Diagnosis Information in Full Bridge Mode

OnDIAG[1:0] ¹⁾	OmDIAG[1:0] ¹⁾	Full Bridge Mode
00	00	no failure
Single Failure		
00	01	open load in off (or double fault open load and short to GND at <i>OUT22</i> / <i>OUT24</i>)
10	10	short circuit to battery in off
01	01	short circuit to ground in off (or double fault open load and short to GND at <i>OUT21</i> / <i>OUT23</i>)
Double Failure		
00	10	open load and short circuit to bat at <i>OUT22</i> / <i>OUT24</i> in off
01	10	short circuit to ground at <i>OUT21</i> / <i>OUT23</i> and short circuit to battery at <i>OUT22</i> / <i>OUT24</i> in off
10	01	short circuit to battery at <i>OUT21</i> / <i>OUT23</i> and short circuit to ground or open load at <i>OUT22</i> / <i>OUT24</i> in off
Remaining Combinations		
10	00	not existing or transition states after switch off
xx	11	
11	xx	
01	00	

1) n = 21 and m=22 or n=23 and m=24

9.7.3 Electrical Characteristics Half Bridges

Table 33 Electrical Characteristics Half Bridges
 $V_S=13.5V$, $V_{VSV}=5V$, $T_j=-40$ to 150°C , all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
OUT21...24, n=21 to 24							
Operation Current	I_{OUTn}	–	–	0.6	A		P_9.1
Over-current Switch Off Threshold	$I_{OUTn,oc}$	0.6	–	1.5	A		P_9.2
Over-current Switch Off Filter Time	$t_{oc,f}$	0.5	–	2	μs		P_9.3
On Resistance	$R_{OUTn,on}$		–	2.4	Ω	$I_{OUTn}=0.3A$	P_9.4
<i>OUT21</i> On Resistance at Low Battery Voltage, low temperature	$R_{OUT21,on,l,LT}$		–	2.4	Ω	$I_{OUTn}=0.1A$, $V_{BAT}=4.5V$ $T_j<100^\circ\text{C}$	P_9.5
<i>OUT21</i> On Resistance at Low Battery Voltage, high temperature	$R_{OUT21,on,l,HT}$		–	2.6	Ω	$I_{OUTn}=0.1A$, $V_{BAT}=4.5V$ $T_j>100^\circ\text{C}$	P_9.6
Leakage Current, low side	$I_{OUTn,l,low}$	–	–	20 ¹⁾	μA	$V_{OUTn}=13.5V$	P_9.7
Leakage Current, high side	$I_{OUTn,l,high}$	-20 ¹⁾	–	–	μA	$V_{OUTn}=0V$	P_9.8
Turn On Delay Time ²⁾	$t_{d,on}$	–	–	10	μs	$I_{OUTn}=0.3A$, resistive load	P_9.9
Turn Off Delay Time ²⁾	$t_{d,off}$	0.1	–	10	μs	$I_{OUTn}=0.3A$, resistive load	P_9.10
Switch On Time ²⁾	$t_{s,on}$	0.9	–	2.5	μs	$I_{OUTn}=0.3A$, resistive load	P_9.11
Switch Off Time ²⁾	$t_{s,off}$	0.9	–	2.5	μs	$I_{OUTn}=0.3A$, resistive load	P_9.12
Diagnosis OUT21 to 24							
Over Temperature Switch Off Threshold	$T_{OUTn,ot}$	150	–	200	$^\circ\text{C}$	³⁾	P_9.13
Over Temperature Hysteresis	$T_{OUTn,ot,hys}$	–	10	–	$^\circ\text{C}$	³⁾	P_9.14
Open Load in Off Detection Threshold High Limit	$V_{ol,high}$	$0.9*V5V$ -0.2	$0.9*V5V$	$0.9*V5V$ +0.2	V		P_9.15
Open Load in Off Detection Threshold Low Limit	$V_{ol,low}$	$0.5*V5V$ -0.2	$0.5*V5V$	$0.5*V5V$ +0.2	V		P_9.16
Diagnosis Pull Up Current	$I_{diag,pu}$	-980	–	-220	μA		P_9.17
Diagnosis Pull Down Current	$I_{diag,pd}$	150	–	300	μA		P_9.18
Bridge Diagnosis Activation Time	$t_{br,diag,act}$	60	–	135	μs		P_9.19
Bridge Diagnosis Filter Time	$t_{br,diag,f}$	0.5	–	2	μs		P_9.20

1) In operation leakage current covered by open load current

2) see [Figure 31](#) for timing definition

3) not subject to production test, specified by design

9.8 Push Pull Stages *OUT8* to *OUT13* and *DFB8* to *DFB13*

These 5V push pull stages are designed for driving on-board MOSFET's. The outputs are fully protected and various diagnosis functions are implemented.

They are controlled and enabled like all power stages according the description in [Chapter 9.1](#) and [Chapter 9.2](#). In off ("0" in control register or "low" at the configured direct drive input pin) the low side transistor of the push/pull stage is on and forces a "low voltage level at the pin.

9.8.1 Protection of *OUT8* to *OUT13*

There are functions implemented to detect short to battery at the external MOSFET and to protect the driver outputs.

For the short to battery detection feedback pins *DFB8* to *DFB13* are implemented to sense the voltage at the drain of the external MOSFET. The short to battery detection in on is done by comparing the voltage level of the drain feedback pins with the short to bat detection threshold.

A short is detected after the "[Short to Battery Detection Filter Time](#)". In case of short to battery the output is switched off and the corresponding diagnosis bits in the diagnosis register [OutDiag1](#) to [OutDiag3](#) are set according the priority shown in [Table 34](#). There are four different thresholds, "[Short to Battery Detection Threshold in On 1](#)" to "[Short to Battery Detection Threshold in On 4](#)", implemented so that the detection threshold can be adapted to the used MOSFET. The diagnosis of the push pull stages can be set in three groups. The configuration is done with the bits [PP0D](#) to [PP2D](#) in the configuration register [OutConfig2](#) and [OutConfig3](#). The protection of the driver output pins is done by comparing the output voltage on the pins *OUT8* to *OUT13* with the "[Over Voltage Detection Threshold](#)". An over voltage (e.g. short to battery) is detected after the "[Over Voltage Diagnosis Filter Time](#)" and the corresponding diagnosis bits in the diagnosis register [PPOVDiag](#) is set. In case of over voltage high and low side transistors of the push pull driver are switched off (high ohmic state).

9.8.2 Diagnosis of *OUT8* to *OUT13*

For the push pull stages *OUT8* to *OUT13* various diagnosis functions for the external MOSFETs are implemented. The open load, short to ground in off and short to battery in on detection is done via the drain feedback *DFB8* to *DFB13*. The diagnosis pull down current of the open load/short to ground in off detection can be switched off (see configuration register [OutConfig2](#)). With deactivated pull down current open load in off detection is not active and the diagnosis information of $OnDIAG[1:0]=10_B$ will never occur. With deactivated pull down current the short to ground detection is active.

In [Figure 39](#) the behavior of the output current as a function of the output voltage is shown.

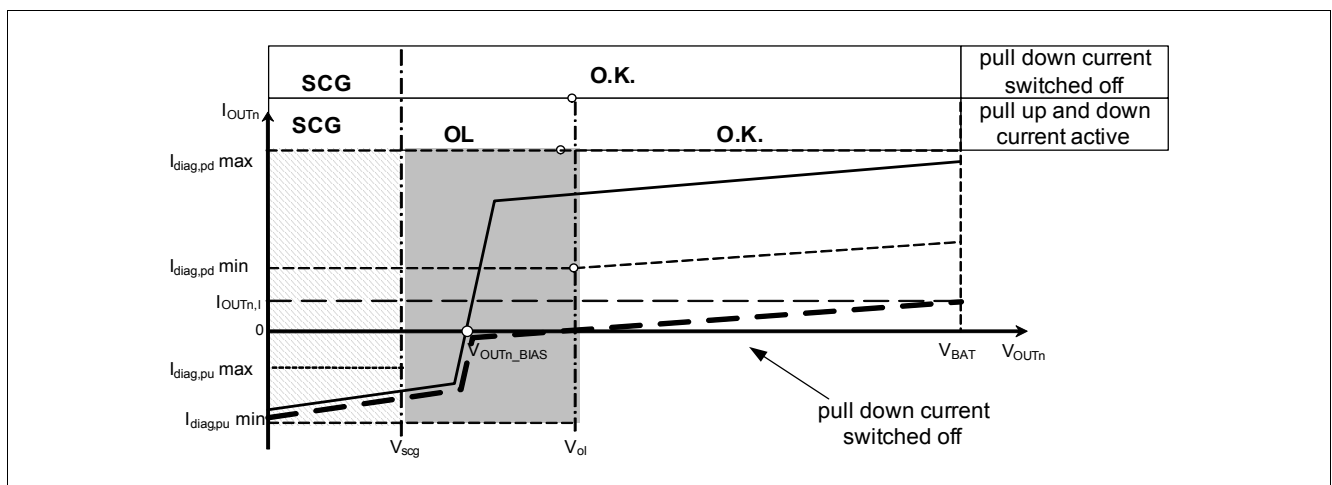


Figure 39 Output behavior in off with open load and short to GND detection of *DFB8* to *DFB13*

Whenever the push pull stages are off the open load/short to GND detection circuit is enabled. To suppress disturbances the output of the detection circuit is stored in the diagnosis register **OutDiag1** to **OutDiag3** after the **Diagnosis Filter Time for Open Load and Short to GND in Off Detection** $t_{diag,f}$ and according to the priority shown in **Table 34**. With the readout of the diagnosis register the content is updated to the actual diagnosis.

Table 34 Description of Diagnosis Information (DFB8 to DFB13)

OnDIAG[1:0]	Priority (1 = highest priority)	Description
00	4	no failure
01	1	short circuit to battery
10	2	open load in off ¹⁾
11	3	short circuit to ground in off

1) no open load in off detection with deactivated pull down current

9.8.3 Electrical Characteristics Push Pull Stages *OUT8* to *OUT13*

Table 35 Electrical Characteristics Push Pull Stages *OUT8* to *OUT13*

Stages on or off, $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
OUT8...13, n=8 to 13							
High Level Output Voltage	$V_{OUTn,h}$	4	–	5.5	V	$I_{OUTn}=-5mA$	P_9.8.1
Low Level Output Voltage	$V_{OUTn,l}$	–	–	0.6	V	$I_{OUTn}=5mA$	P_9.8.2
Pull up current	$I_{OUTn,pu}$	–	–	-20	mA	$V_{OUTn}=0V$, OUTn on	P_9.8.3
Pull down current	$I_{OUTn,pd}$	20	–	–	mA	$V_{OUTn}=5V$, OUTn off	P_9.8.4
Over Voltage Detection Threshold	$V_{OUTn,ov,th}$	5.5	–	7.7	V		P_9.8.5
Over Voltage Diagnosis Filter Time	$t_{OUTn,ov,f}$	5	–	10	μs		P_9.8.6
Diagnosis DFB8 to DFB13							
Short to Battery Detection Threshold in On 1	$V_{DFBn,sb,1}$	90	125	150	mV	referred to <i>PGND</i>	P_9.8.7
Short to Battery Detection Threshold in On 2	$V_{DFBn,sb,2}$	180	225	250	mV	referred to <i>PGND</i>	P_9.8.8
Short to Battery Detection Threshold in On 3	$V_{DFBn,sb,3}$	350	400	450	mV	referred to <i>PGND</i>	P_9.8.9
Short to Battery Detection Threshold in On 4	$V_{DFBn,sb,4}$	0.7	0.8	0.9	V	referred to <i>PGND</i>	P_9.8.10
Short to Battery Detection Filter Time	$V_{DFBn,sb,fl}$	10	–	15	μs		P_9.8.11
Open Load in Off Detection Threshold	V_{ol}	$V5V-0.2$	$V5V$	$V5V+0.2$	V		P_9.8.12

Table 35 Electrical Characteristics Push Pull Stages *OUT8* to *OUT13* (cont'd)

Stages on or off, $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Short to GND in Off Detection Threshold	V_{scg}	$0.5 \cdot V_{V5V} - 0.2$	$0.5 \cdot V_{V5V}$	$0.5 \cdot V_{V5V} + 0.2$	V		P_9.8.13
Diagnosis Pull Down Current in Off	$I_{diag,pd}$	220	–	600	μA	$V_{DFBn}=13.5V$	P_9.8.14
Diagnosis Pull Up Current in Off	$I_{diag,pu}$	-300	–	-100	μA	$V_{DFBn}=0V$	P_9.8.15
Diagnosis Filter Time for Open Load and Short to GND in Off Detection	$t_{diag,f,off}$	60	–	135	μs		P_9.8.16
Pull Down Current in On	$I_{diag,pd,on}$	–	–	1.8	μA	$V_{DFBn}=5V$	P_9.8.17

9.9 Push Pull Stages *IGN1* to *IGN4*

The *IGN1* to *IGN4* are 5V push pull stages for on- and off-board ignition power stages (e.g. with IGBT's, darlington transistors). For off board ignition power stages the outputs *IGN1* to *IGN4* are equipped with a back supply suppression (in case of a short circuit from *IGN1* to *IGN4* to battery there is no parasitic current flow back to 5V).

They are controlled and enabled like all power stages according the description in [Chapter 9.1](#) and [Chapter 9.2](#). Additionally a “high” at the pin *IGNEN* is needed to enable the outputs. In off (“0” in control register or “low” at the configured direct drive input pin or *IGNEN* is “low”) the low side transistor of the push/pull stage is on and forces a “low voltage level at the pin.

The outputs are fully protected and various diagnosis functions are implemented.

9.9.1 Protection of *IGN1* to *IGN4*

The protection of the outputs is done by detecting short to battery and short to ground. This is done by comparing the output voltage level with the “[Short to Battery Detection Threshold](#) and [Short to Ground Detection Threshold](#)”. To suppress disturbances the output signal of the short to GND and short to battery detection circuit is stored in the diagnosis register *IgnDiag* after the “[Diagnosis Filter Time for Short to GND and Battery Detection](#)” $t_{diag,f,sc}$ and according the priority shown in [Table 36](#).

During detected short to GND the output is switched off (low side transistor of push/pull stage is on), during detected short to battery the output is high ohmic (tristate).

The short to battery detection is always active. The short to ground detection is enabled with the on signal of the output stage.

Additionally an over temperature protection is implemented. There is one common sensor for *IGN1* and *IGN2* and one for *IGN3* and *IGN4*.

9.9.2 Diagnosis of *IGN1* to *IGN4*

An open load detection during the switch on phase is implemented and can be enabled with the bit *IOLA* in the configuration register *IGNConfig*. In [Figure 40](#) the detection principle is shown. When the open load detection in on is enabled, first the output is pulled up by a defined current, which is set by the bits *IOLI* in the configuration register *IGNConfig*.

The output voltage, which is passed to the detection circuit, is filtered (“[Diagnosis Filter Time for Open Load Detection](#)”) to suppress disturbances. After the open load time (“[Open Load Time 1](#)” to “[Open Load Time 4](#)” selected in configuration register *IGNConfig* bits *IOLT*) the filtered output is compared with the [Open Load](#)

Detection Threshold V_{ol} . The diagnosis register **IgnDiag** is set if the filtered output is higher than the **Open Load Detection Threshold** and the output is fully switched on.

The failures are stored in the diagnosis register according the priority shown in **Table 36** with “1” is the highest priority. With the readout of the diagnosis register **IgnDiag** the content is updated to the actual diagnosis.

Table 36 Description of Diagnosis Information (IGN1 to IGN4)

IGNnDIAG[1:0]	Priority (1 = highest priority)	Description
00	4	no failure
01	1	short circuit to battery or over temperature
10	2	open load
11	3	short circuit to ground in on

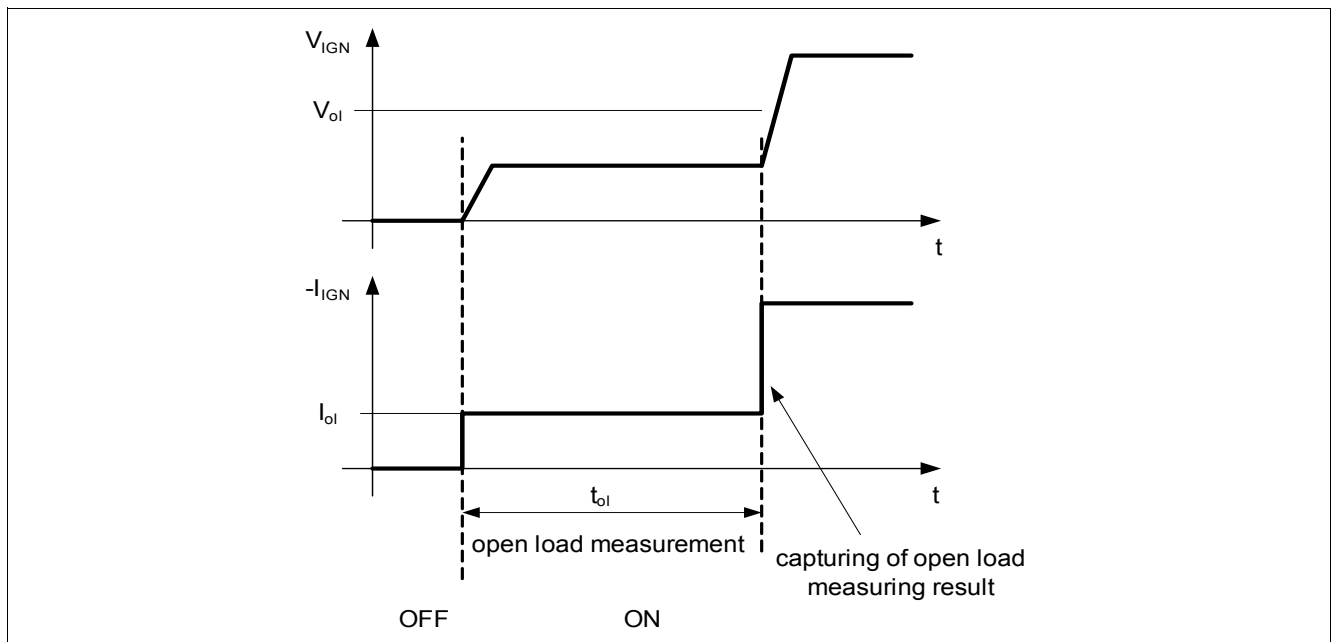


Figure 40 Ignition Output Open Load Detection

9.9.3 Electrical Characteristics Push Pull Stages *IGN1* to *IGN4*

Table 37 Electrical Characteristics Push Pull Stages

Stages on or off, $V_S=13.5V$, $V_{VSV}=5V$, $T_j=-40$ to $150^{\circ}C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
IGN1...4, n=1 to 4							
High Level Output Voltage	$V_{IGNn,h}$	4.35	–	–	V	$I_{IGNn}=-15mA$,	P_9.9.1
Low Level Output Voltage	$V_{IGNn,l}$	–	–	0.6	V	$I_{IGNn}=5mA$	P_9.9.2
Pull up current	$I_{IGNn,pu}$	–	–	-20	mA	$V_{IGNn}=0V$, IGNn on	P_9.9.3

Table 37 Electrical Characteristics Push Pull Stages (cont'd)

Stages on or off, $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull down current	$I_{IGNn,pd}$	20	–	–	mA	$V_{IGNn}=5V$, IGNn off	P_9.9.4
Leakage current	I_{L_IGNn}	–	–	120	μA	$V_{IGNn}=13.5V$	P_9.9.5
Leakage current to $V5V$	$I_{L_IGNn,V5V}$	–	–	1	μA	$V_{IGNn}=13.5V$	P_9.9.26
Over Temperature Switch Off Threshold	$T_{IGNx,ot}$	150	–	200	$^\circ C$	1)	P_9.9.6
Over Temperature Hysteresis	$T_{IGNx,ot,hys}$		10		$^\circ C$	1)	P_9.9.7

Diagnosis *IGN1* to *IGN4*

Short to Battery Detection Threshold	$V_{IGNn,scb}$	6.4	–	7.5	V		P_9.9.8
Short to Ground Detection Threshold	V_{scg}	1.6	–	2.3	V		P_9.9.9
Diagnosis Filter Time for Short to GND and Battery Detection	$t_{diag,f,sc}$	5	–	10	μs		P_9.9.10
Open Load Detection Threshold	V_{ol}	4	–	4.5	V		P_9.9.11
Open Load Switch On Current 1	$I_{olf,1}$	-120	-100	-40	μA		P_9.9.12
Open Load Switch On Current 2	$I_{olf,2}$	-500	-400	-300	μA		P_9.9.13
Open Load Switch On Current 3	$I_{olf,3}$	-1.2	-1	-0.4	mA		P_9.9.14
Open Load Switch On Current 4	$I_{olf,4}$	-5	-4	-2.5	mA		P_9.9.15
Open Load Time 1	$t_{ol,1}$	50	60	70	μs		P_9.9.16
Open Load Time 2	$t_{ol,2}$	210	250	290	μs		P_9.9.17
Open Load Time 3	$t_{ol,3}$	450	510	570	μs		P_9.9.18
Open Load Time 4	$t_{ol,4}$	690	775	860	μs		P_9.9.19
Diagnosis Filter Time for Open Load Detection	$t_{diag,f,olf}$	6	10	14	μs		P_9.9.20

Direct Drive Inputs *IGNEN*

Low Level Input Voltage	$V_{IN,l}$	-0.3	–	0.9	V		P_9.9.21
High Level Input Voltage	$V_{IN,h}$	2	–	V_{VDDIO}	V		P_9.9.22
Input Voltage Hysteresis	$V_{IN,hys}$	50	200	–	mV		P_9.9.23
Pull Down Current	$I_{IN,pd}$	25	–	100	μA	$V_{IN}=V_{VDDIO}$	P_9.9.24
Pull Down Current	$I_{IN,pd}$	2.4	–	–	μA	$V_{IN}=0.6V$	P_9.9.25

1) Parameter is not subject of production test, specified by design

10 VR and Hall Sensor Interface

The variable reluctance (VR) sensor interface converts an output signal of a VR sensor into a push-pull logic level signal suited for micro controller input ports. To achieve the best accuracy for the positive and the negative edge of the VR_{OUT} signal the switching point is the zero crossing. For robustness against disturbances the next zero crossing is enabled only if a signal peak (minimum or maximum of the signal) is detected. The amplitude of the VR sensor signal is limited by an internal clamping circuit to avoid damage of the device due to over voltage caused by the VR sensor signal.

There are three operation modes for VR sensor applications and one Hall sensor mode implemented. The manual VR sensor mode with static setup of the detection parameter under control of the micro controller via MSC/SPI and an auto mode with an adaptive algorithm to ensure best detection performance. The semi auto mode is less accurate than the auto mode.

The diagnosis VR sensor interface setup could be done by measuring the voltage between the two input pins during diagnosis mode. Additionally three diagnosis bits for short to battery, short to GND and open load (directly at the pins) are available.

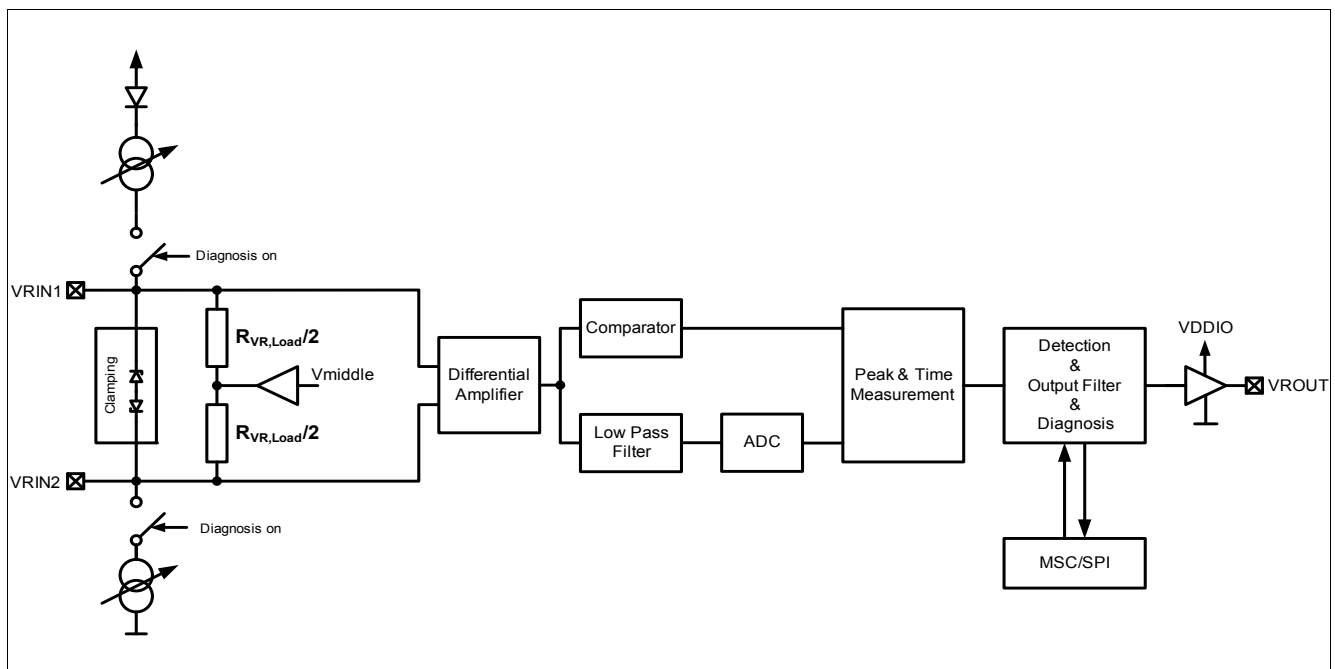


Figure 41 VR Sensor Interface Block diagram

10.1 Signal Detection

The signal detection for Hall sensor mode is a comparator with the switching threshold $V_{VRIN1,th,hall}$ and the hysteresis $V_{VRIN1,hys,hall}$. The detection of the VR signal consist of the zero crossing detection, peak detection and the output filter. At the input there is a clamping circuit between the pins $VRIN1$ and $VRIN2$ suited to clamp the maximum current of VR sensors.

The zero crossing detection ensures that the influence of the input signal slope is eliminated for both edges. To avoid disturbances due to the floating input signal a middle voltage is applied with the integrated load resistance. The clamping circuit between the pins $VRIN1$ and $VRIN2$ clamps the input voltage in both direction to protect the input structures. The clamping is suited for VR sensors with a maximum output current of $DI_{VR,clamp}$ (see [Table 38](#)).

The peak detection is done by measuring the voltage difference by the analog to digital converter and the detection of the slope of the input signal. If the gradient of the slope changes the sign the next zero crossing detection is enabled. The detection of the sign is done by comparing the absolute value of the signal with the peak detection

threshold ($V_{VR,peak,min,1}$ to $V_{VR,peak,min,4}$ according setup). A sign change is only valid if the absolute value of the signal is larger than peak detection threshold ($V_{VR,peak,min,1}$ to $V_{VR,peak,min,4}$ according setup) for a time longer than the peak detection time $t_{VR,peak,min,1}$ to $t_{VR,peak,min,2}$ according setup (see [Figure 42](#)).

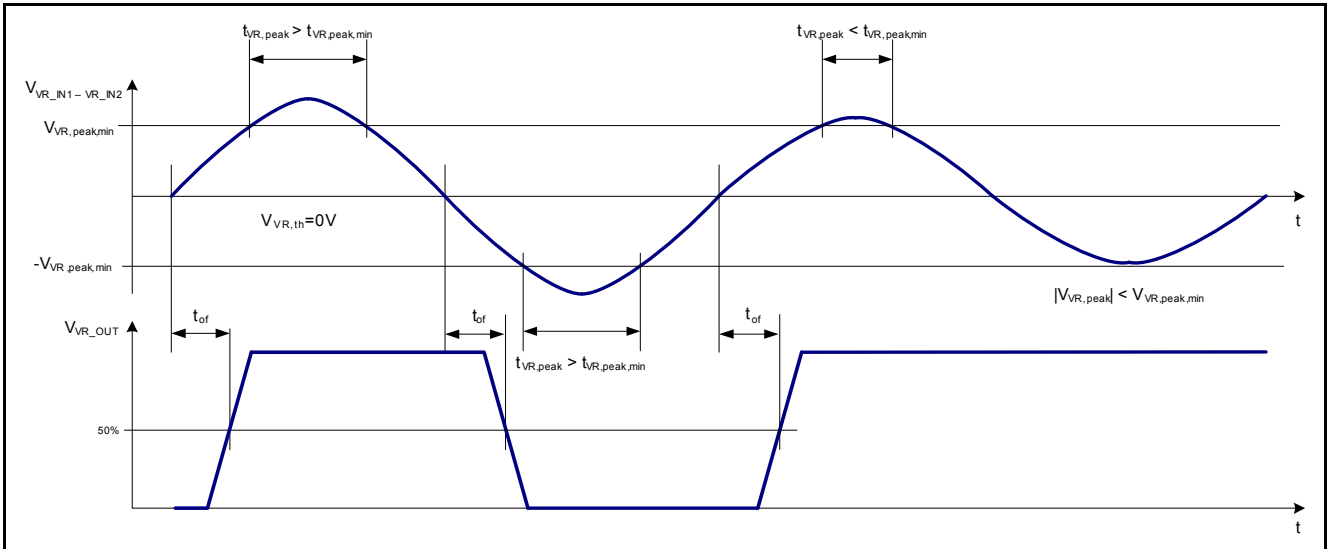


Figure 42 Timing Characteristics of the VR Sensor Interface

The output filter is implemented for all operation modes to suppress disturbances with high frequencies. The function is shown in [Figure 43](#). The output signal V_{ROUT} is filtered with the time $t_{of,1}$. The output signal of the internal zero crossing detection must be stable for a time longer than $t_{of,1}$.

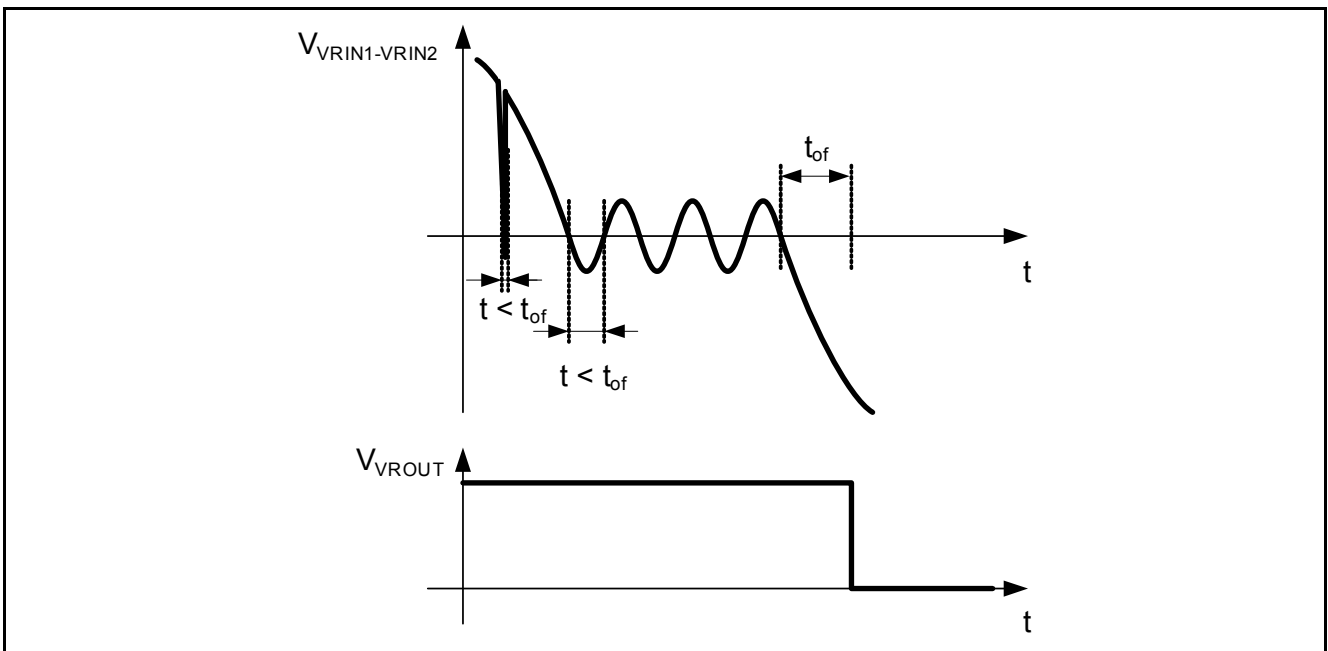


Figure 43 Output Filter Behavior

Following parameters could be set by MSC/SPI communication:

- peak detection threshold $V_{VR,peak,min,1}$ to $V_{VR,peak,min,4}$ with the bits **VRSPV** in the configuration register **VRSCfg0**
- peak detection time $t_{VR,peak,min,1}$ to $t_{VR,peak,min,2}$ with the bit **VRSPt** in the configuration register **VRSCfg0**
- output filter time $t_{of,1}$ to $t_{of,4}$ with the bits **VRSF** in the configuration register **VRSCfg0**

10.2 Detection Modes

The TLE8888-1QK integrates four detection modes:

- auto detection mode for VR sensor signals
- manual detection mode for VR sensor signals
- semi auto detection mode for VR sensor signals
- detection mode for Hall sensor signals

To select the various detection modes the bits **VRSM** in the configuration register **VRSCfg1** must be set.

Auto detection mode for VR sensor signals: In the auto detection mode an algorithm is setting all parameters to the optimal values to achieve the best detection behavior. The peak detection time is set due to the actual speed value, the peak detection threshold is set due to the level of the previous peaks. The output filter time ($t_{of,1}$ to $t_{of,4}$) is set by the micro controller independently to increase the robustness against short disturbances at the inputs. Write access to the registers bits of **VRSPT** and **VRSPV** are ignored in auto detection mode.

Semi auto detection mode for VR sensor signals: The algorithm of the semi auto mode is based on less number of measurement information as the auto detection mode. This leads to a simpler implementation of the detection algorithm. The output filter time ($t_{of,1}$ to $t_{of,4}$) is set by the micro controller independently to increase the robustness against short disturbances at the inputs. Write access to the registers bits of **VRSPT** and **VRSPV** are ignored in semi auto detection mode.

Manual detection mode for VR sensor signals: In the manual detection mode the micro controller has the full control of all parameters of the detection and the algorithm of the auto detection modes are disabled. The settings are done via the MSC/SPI interface.

Detection mode for Hall sensor signals: For the Hall sensor mode the pin *VRIN2* is forced internally to the switching threshold $V_{VRIN1,th,hall}$. The detection principle is a comparator with hysteresis. Write access to the registers bits of **VRSPT** and **VRSPV** are ignored in the detection mode for Hall sensor signals. The diagnosis is disabled. With this set up the number of external devices is reduced (see [Chapter 17.2](#)).

*Note: Switching between the different configuration must be avoided with active signals at the inputs *VRIN1* and *VRIN2*.*

10.3 Diagnosis for VR Sensor Signal Detection Modes

The TLE8888-1QK integrates three different diagnosis modes for the VR sensor interface:

- **short to GND/short to battery diagnosis mode:** detection of short to GND or short to battery directly at pins *VRIN1* and *VRIN2*
- **open load diagnosis mode:** detection of open load directly at pins *VRIN1* and *VRIN2*
- **ADC measurement mode:** measurement of the voltage between the pins *VRIN1* and *VRIN2*

The modes are defined in the configuration register **VRSCfg1** with the bits **VRSDIAGM**.

The diagnosis of the VR sensor is done by activating the diagnosis mode with the bits **VRSDIAGM** in the configuration register **VRSCfg1** and starting diagnosis measurement with the bit **VDIAGS** in the command register **Cmd0**. With the activation of the VRS diagnosis mode at *VRIN1* a pull up current source to the internal supply and at *VRIN2* a pull down current source is applied (current configuration with bits **VRSI_SC** for short to GND/short to battery diagnosis mode, **VRSI_OL** for open load diagnosis mode and **VRSI_ADC** for ADC measurement mode in the configuration registers **VRSCfg1** and **VRSCfg2**). To avoid bad influence of the time constants of the external circuitry the timing of the measurement is controlled by the micro controller. The sequence is shown in [Figure 44](#).

The end of the diagnosis procedure triggered by the start command is signaled by the correspondent data valid bits **VRSDV_SC** (short to GND and short to battery diagnosis mode), **VRSDV_OL** (open load diagnosis mode) in diagnosis register **VRSDiag0** and **VRSDV_ADC** (ADC measurement mode) in the diagnosis register **VRSDiag1**. For the detection thresholds see parameter **Short to GND detection threshold**, **Short to battery detection**

threshold and **Open load detection threshold**. The output of the ADC measurement is defined by the parameter **ADC measurement gain** and **ADC measurement offset**.

The result of the diagnosis is available in the diagnosis register **VRSDiag0** with the bits **VRSG** (short to GND detection), **VRSB** (short to battery detection) and **VR SOL** (open load detection directly at the pins). The digital value of the ADC measurement is available in the register **VRSDiag1** with the bits **VRSD**. This ADC value can be used by the micro controller to define additional error detection conditions different to the defined short to GND, short to battery and open load thresholds.

The data valid bits are reset with start of the corresponding diagnosis or with the readout of the register.

*Note: In detection mode for Hall sensor signals the diagnosis is deactivated and the values of **VRSDIAGM** and **VR SI_SC** in the register **VR SConfig1**, **VR SI_ADC** and **VR SI_OL** in register **VR SConfig2** and the start command **VDIAGS** in the register **Cmd0** are ignored.*

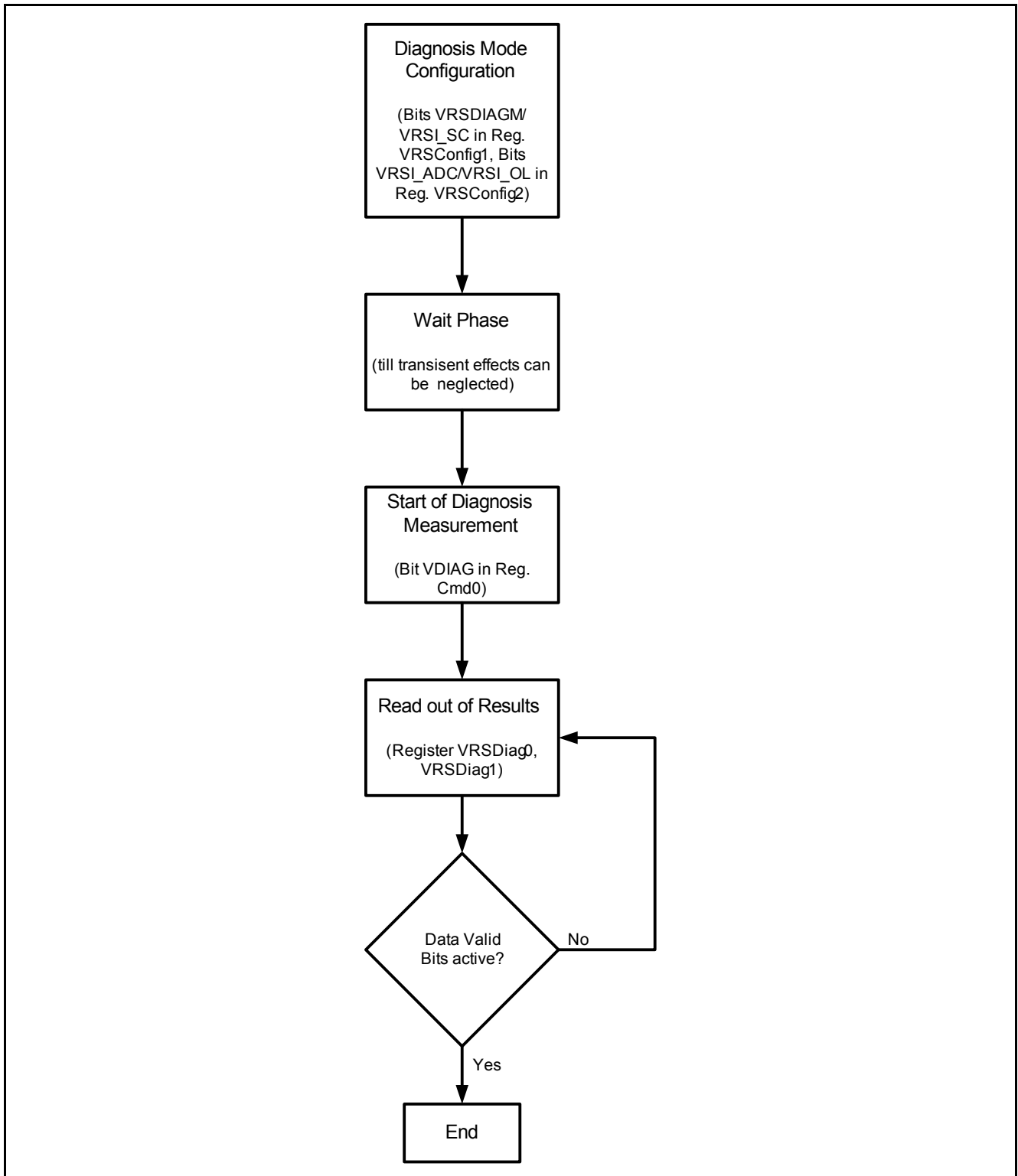


Figure 44 VRS Flow Chart

For the measurement the internal circuits are changed. In [Figure 45](#), [Figure 46](#) and [Figure 47](#) the block diagram of the different setups are shown.

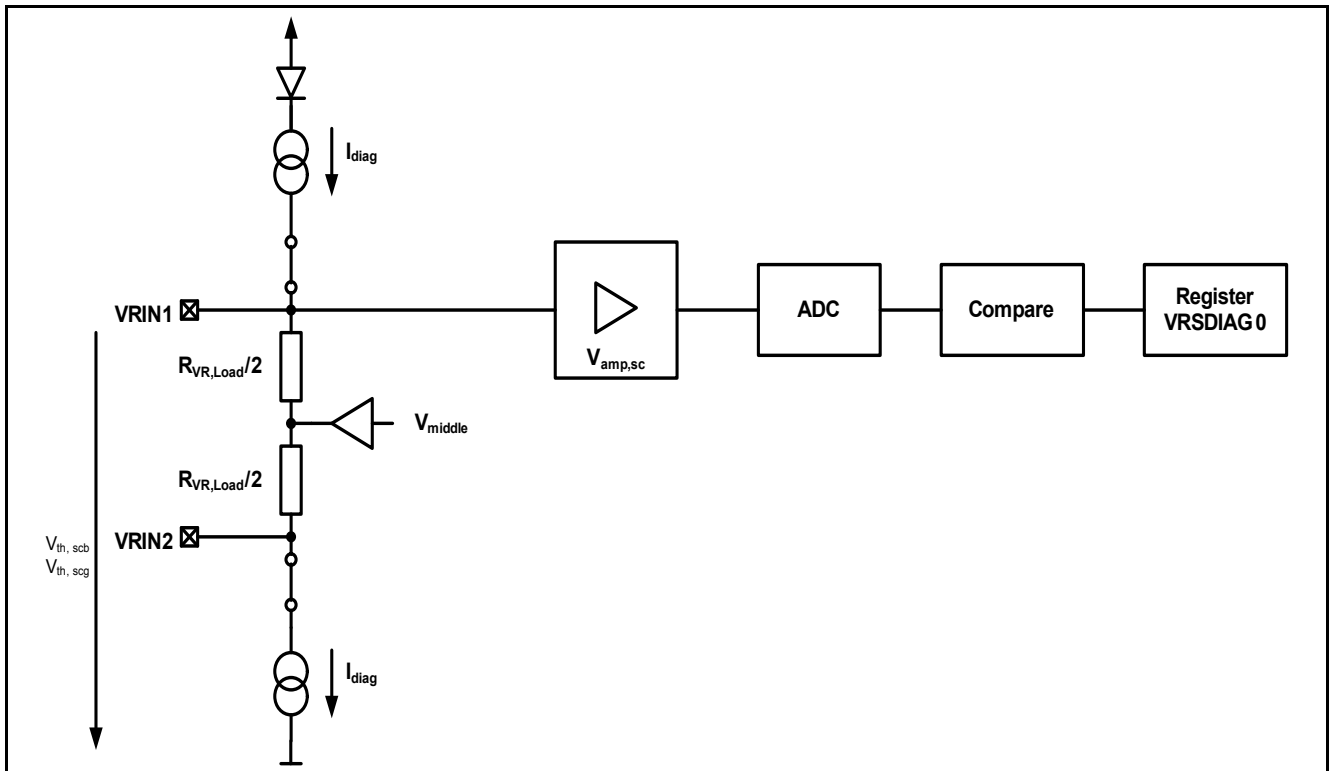


Figure 45 VRS Diagnosis Block Diagram for Short to GND and Short to Battery Measurement

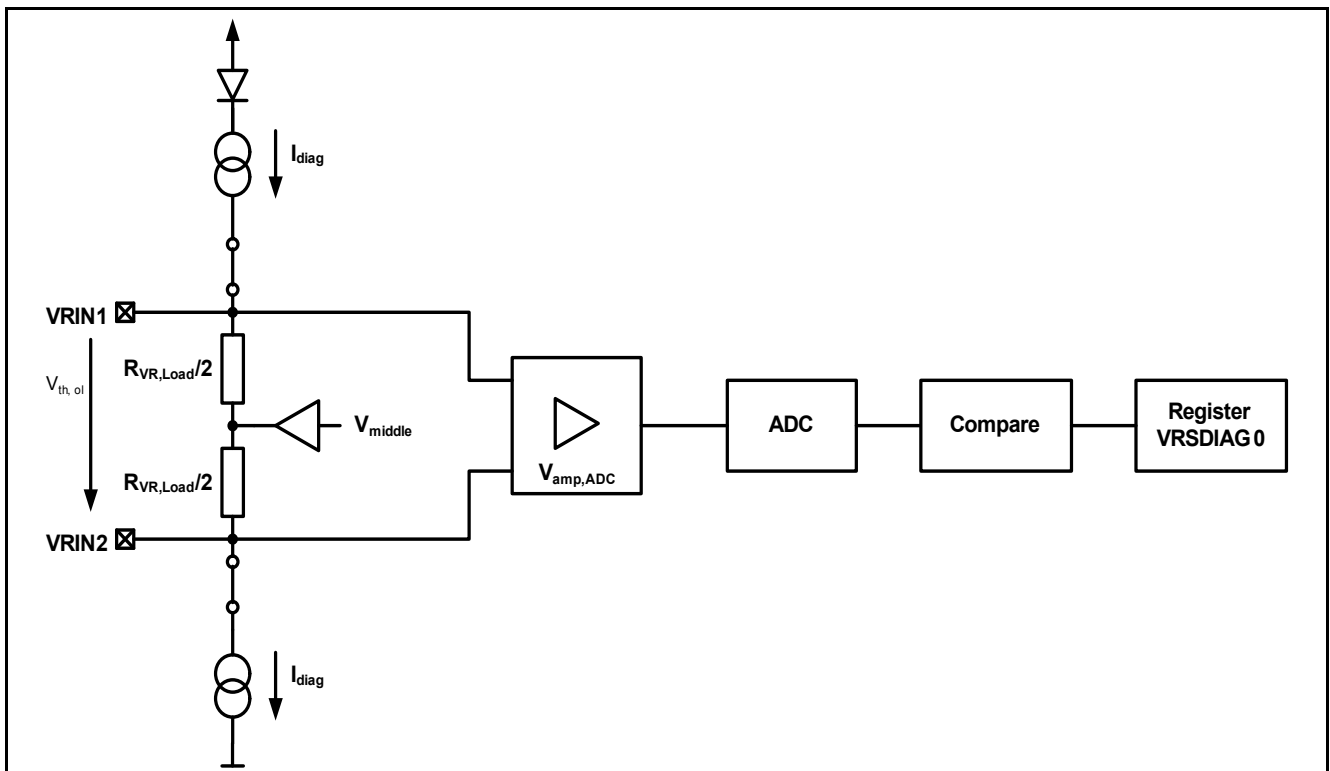


Figure 46 VRS Diagnosis Block Diagram for Open Load Measurement

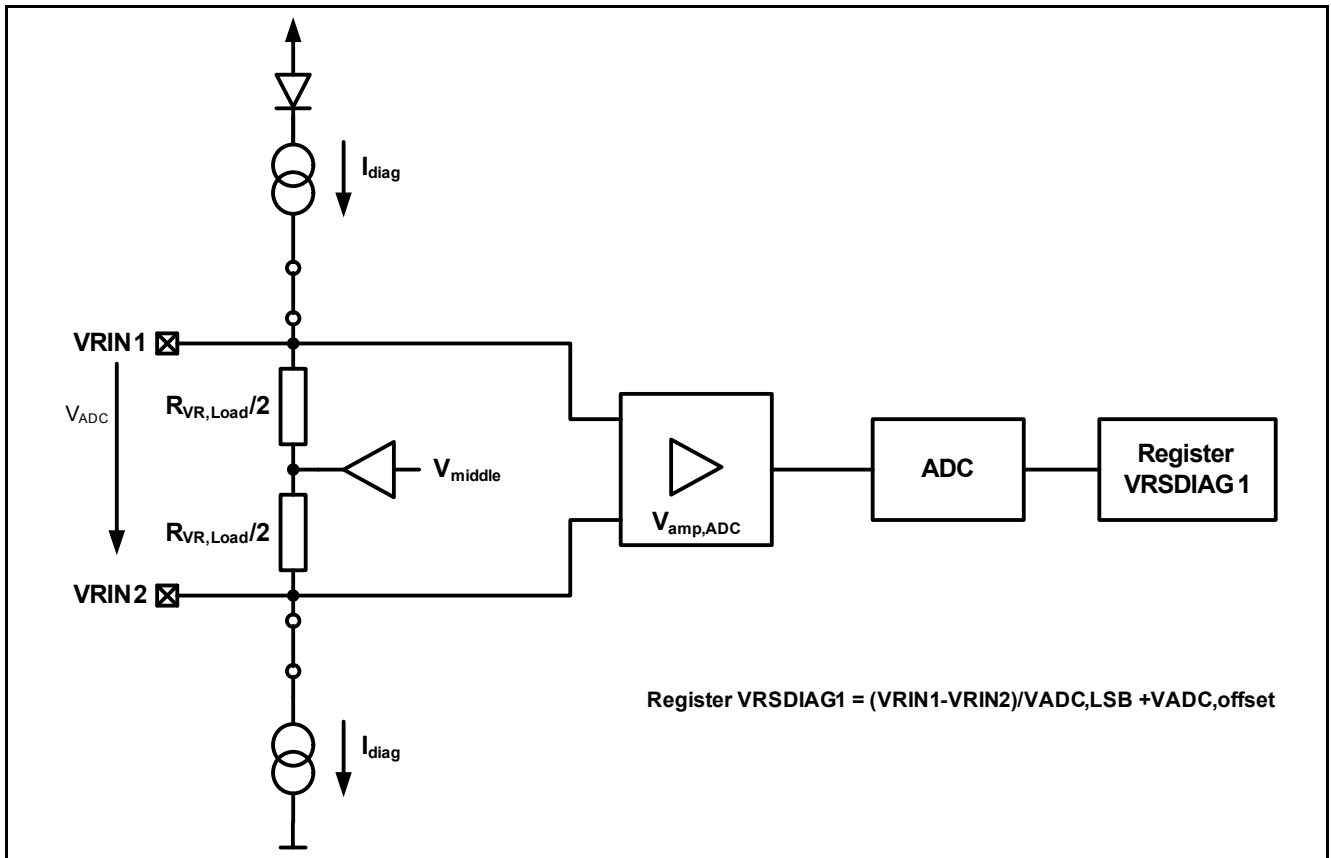


Figure 47 VRS Diagnosis Block Diagram for ADC Measurement

10.4 Electrical Characteristics VR Sensor Interface

Table 38 Electrical Characteristics: VR Sensor Interface

$V_S=13.5V$, $V_{VS}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics:							
VR Sensor Interface Detection Threshold	$V_{VR,th}$	-30	0	30	mV		P_10.4.1
minimum amplitude for peak detection 1	$V_{VR,peak,min,1}$	–	50	–	mV	reset value	P_10.4.2
minimum amplitude for peak detection 2	$V_{VR,peak,min,2}$	–	150	–	mV		P_10.4.3
minimum amplitude for peak detection 3	$V_{VR,peak,min,3}$	–	350	–	mV		P_10.4.4
minimum amplitude for peak detection 4	$V_{VR,peak,min,4}$	–	550	–	mV		P_10.4.5
minimum time for peak detection 1	$t_{VR,peak,min,1}$	–	10	–	μs	reset value 1kHz sinusoidal signal	P_10.4.6
minimum time for peak detection 2	$t_{VR,peak,min,2}$	–	250	–	μs	1kHz sinusoidal signal	P_10.4.7
VR Sensor Interface Load Resistance	$R_{VR,Load}$	50	75	110	$k\Omega$		P_10.4.9
VR Sensor Interface Input Clamping Current	$\Delta I_{VR,clamp}$	–	–	50	mA	$\Delta I_{VR,clamp} = (I_{VRIN1} - I_{VRIN2})/2$	P_10.4.18
VR Sensor Interface Input Clamping Voltage	$\Delta V_{VR,clamp}$	2	–	3	V	$\Delta V_{VR,clamp} = V_{VRIN1} - V_{VRIN2} $, $I_{VR,clamp} = 50mA$	P_10.4.19
Switching threshold voltage at pin <i>VRIN1</i> for Hall Sensor Mode	$V_{VRIN1,th, hall}$	0.9	–	2	V	no load at pin <i>VRIN2</i> ¹⁾	P_10.4.20
Switching hysteresis pin <i>VRIN1</i> for Hall Sensor Mode	$V_{VRIN1,hys, hall}$	0.35	0.5	–	V	no load at pin <i>VRIN2</i>	P_10.4.10
Middle voltage level normal mode	V_{middle}	1.9	2.25	2.5	V		P_10.4.11
VRS Diagnosis:							
Middle voltage level diagnosis mode	V_{middle}	0.9	1.3	1.65	V		P_10.4.12
Diagnosis measurement time	t_{conv}	–	7	8	μs		P_10.4.13

Table 38 Electrical Characteristics: VR Sensor Interface (cont'd)

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^{\circ}C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Diagnosis current accuracy	$I_{diag, acc}$	-30%	–	+30%		$VRIN1 = VRIN2 = V_{middle}$; typ. values see register VRConfig1 and VRConfig2	P_10.4.14
Short to GND detection threshold	$V_{th,scg}$	0.8	–	1.1	V		P_10.4.15
Short to battery detection threshold	$V_{th,scb}$	2.8	–	3.3	V		P_10.4.16
Open load detection threshold	$V_{th,ol}$	0.9	–	1.2	V		P_10.4.17
ADC measurement input range	$V_{ADC,r}$	-1.5	–	1.5	V		P_10.4.8
ADC measurement gain	$V_{ADC,LSB}$	–	49	–	mV	valid from 6_d to 70_d	P_10.4.31
ADC measurement offset	$V_{ADC,offset}$	–	37_d	–			P_10.4.32
Output Characteristics:							
Low Level Output Voltage - Low Output Current	$V_{VR_OUT,L,l}$	–	–	0.4	V	$I_{VR_OUT} = 100\mu A$	P_10.4.21
Low Level Output Voltage - High Output Current	$V_{VR_OUT,L,h}$	–	–	1.5	V	$I_{VR_OUT} = 1mA$	P_10.4.22
High Level Output Voltage - Low Output Current	$V_{VR_OUT,H,l}$	VDDIO -0.4	–	–	V	$I_{VR_OUT} = -100\mu A$	P_10.4.23
High Level Output Voltage - High Output Current	$V_{VR_OUT,H,h}$	VDDIO -1.5	–	–	V	$I_{VR_OUT} = -1mA$	P_10.4.24
Transfer Characteristics:							
Output Filter Time 1	$t_{of,1}$	1	2	3	μs	reset value	P_10.4.25
Output Filter Time 2	$t_{of,2}$	5	6	7.5	μs		P_10.4.26
Output Filter Time 3	$t_{of,3}$	9.5	11	13	μs		P_10.4.27
Output Filter Time 4	$t_{of,4}$	19	21	23	μs		P_10.4.28

1) external circuitry for hall mode see [Chapter 17.2](#)

11 Local Interconnect Network (LIN)

The LIN interface is designed for in-vehicle networks using data transmission up to 20kbit/s. The implementation of the physical layer is according to LIN specification revision 2.1 for slave nodes and is compatible with lower versions like revision 2.0 and 1.3¹⁾. *LINTX* is the transmit-data input from the micro controller, *LINIO* is the bidirectional LIN bus signal and *LINRX* is the receive-data output to the micro controller. The transmitted data stream at *LINTX* is converted to the LIN bus signal at *LINIO*. *LINRX* reflects the received data at *LINIO* with a logic signal suited for 3.3V and 5V micro controller interfaces.

The detection thresholds at *LINIO* are related to the power supply *BATPA*²⁾.

The LIN interface of the TLE8888-1QK is compatible to the physical layer definition of the K-Line (ISO 9141) standard. For K-Line operation no additional settings are necessary.

A flash mode for high speed operation can be selected with the communication interface (MSC or SPI). There is no bus wake up function implemented.

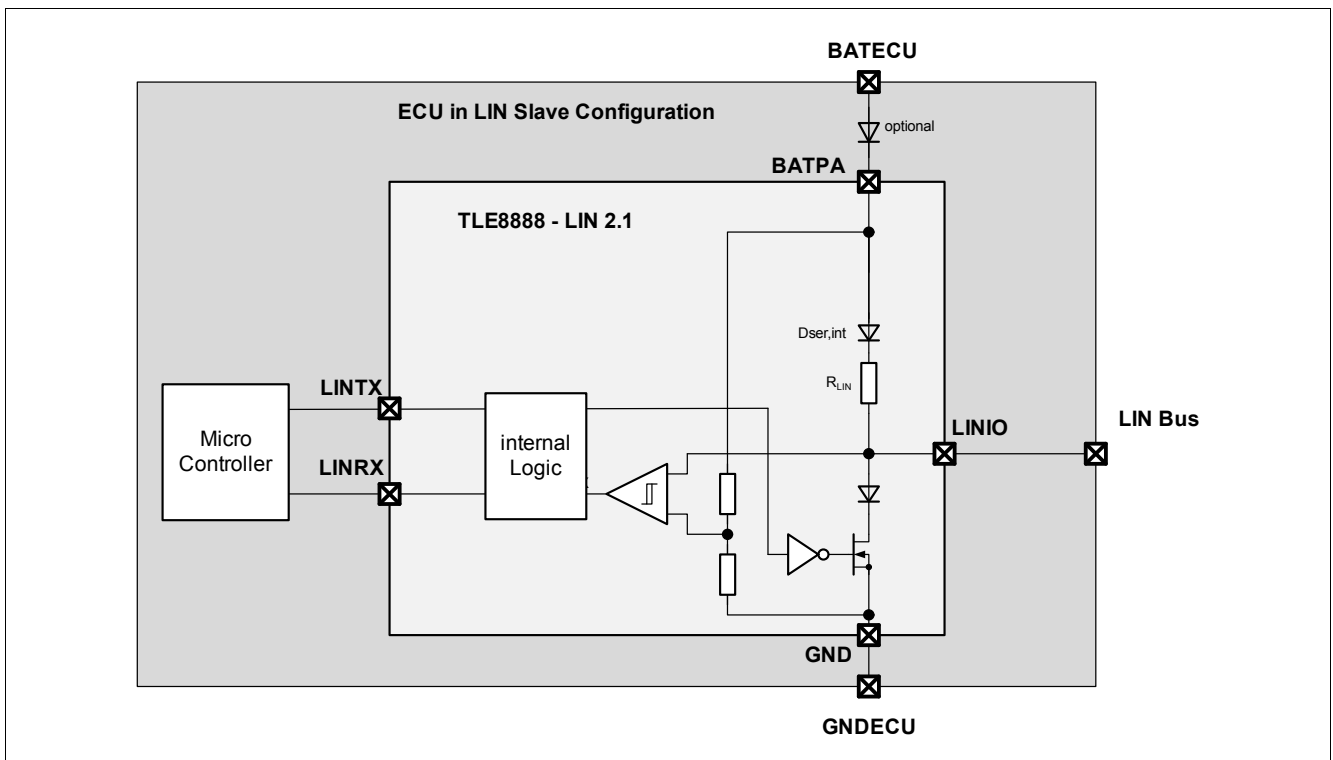


Figure 48 Local Interconnect Network (LIN) Slave Node

The LIN interface in the TLE8888-1QK is implemented according the requirements of the standard for slave nodes. For master setup an external pull up resistor (typ. 1kΩ, see definition in LIN specification) and a diode must be connected to *LINIO* and *BATPA* on the ECU (see [Figure 49](#)).

1) see LIN specification revision 2.1 chapter 6.2

2) *BATPA* is identical to the internal supply voltage V_{SUP} defined in LIN specification revision 2.1

11.2.3 Bus Wiring Short to Battery or GND

The LIN interface is protected against short to battery or short to GND. Upon remove of the fault, normal operation shall resume without any intervention on the LIN bus line (pin *LINIO*).

11.2.4 TX Time Out

The TX time out function is implemented to prevent the bus line from being blocked by a permanent 'low' at the pin *LINTX* caused by an error at the ECU or the micro controller. If the *LINTX* signal is 'low' (dominant) for $t > t_{\text{timeout}}$ the transmission of the *LINTX* signal to the bus is deactivated and the LIN output stage is disabled.

The transmission is reactivated, after a rising edge at *LINTX* was detected. The implemented time out feature requires a minimum data rate of 1600 bit/s.

The time out function can be disabled with the configuration bit **LINTOE** in the configuration register **ComConfig1**.

11.2.5 Over Temperature Protection

The LIN bus output *LINIO* is protected against overload with an over temperature protection. In case of over temperature the output transistor is switched off and the diagnosis bit **LINOT** in the diagnosis register **ComDiag** is set. The configuration register is not changed.

11.3 Electrical Characteristics LIN

Table 39 Electrical Characteristics: LIN

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{BATPA,LIN}$	7	–	18	V	acc. Param 10 LIN Spec. Rev. 2.1	P_11.3.1
Limitation Current at LINIO for driver dominant state	$I_{LINIO,lim}$	40	–	200	mA	acc. Param 12 LIN Spec. Rev. 2.1	P_11.3.2
Leakage Current at LINIO for bus dominant state and driver off	$I_{LINIO,leak,dom}$	-1	–	–	mA	acc. Param 13 LIN Spec. Rev. 2.1 $V_{LINIO}=0V$ $V_{BAT}=12V$	P_11.3.3
Leakage Current at LINIO for bus recessive state	$I_{LINIO,leak,rec}$	–	–	20	μA	acc. Param 14 LIN Spec. Rev. 2.1 $V_{LINIO}>V_{BAT}$	P_11.3.4
Current at LINIO during GND loss	I_{LINIO,no_GND}	-1	–	1	mA	acc. Param 15 LIN Spec. Rev. 2.1 $GND=V_S$ $0V<V_{LINIO}<18V$ $V_{BAT}=12V$	P_11.3.5
Current at LINIO during power supply loss	I_{LINIO,no_Sup}	–	–	20	μA	acc. Param 16 LIN Spec. Rev. 2.1 $GND=V_S=0V$ $0V<V_{LINIO}<18V$	P_11.3.6
Receiver Dominant State	$V_{LINIO,dom}$	–	–	$0.4 \cdot V_{BA_TPA}$	V	acc. Param 17 LIN Spec. Rev. 2.1	P_11.3.7
Receiver Recessive State	$V_{LINIO,rec}$	$0.6 \cdot V_{BA_TPA}$	–	–	V	acc. Param 18 LIN Spec. Rev. 2.1	P_11.3.8
Receiver switching threshold center voltage	$V_{LINIO,cont}$	$0.475 \cdot V_{BATPA}$	–	$0.525 \cdot V_{BATPA}$	V	acc. Param 19 LIN Spec. Rev. 2.1 $V_{LINIO,cont}=(V_{th,dom}+V_{th,rec})/2$	P_11.3.9

Table 39 Electrical Characteristics: LIN (cont'd)

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Hysteresis of switching threshold	V_{Hys}	–	–	0.175* V_{BATPA}	V	acc. Param 20 LIN Spec. Rev. 2.1 $V_{Hys}=V_{th,rec}-V_{th,dom}$	P_11.3.10
voltage drop at internal serial diode $D_{ser,int}$	V_D	0.4	–	1	V	acc. Param 21 LIN Spec. Rev. 2.1	P_11.3.11
Resistance of internal slave resistor R_{slave}	$R_{LIN,Slave}$	20	–	60	k Ω	acc. Param 26 LIN Spec. Rev. 2.1	P_11.3.12
Duty cycle 1	D_1	0.396	–	–	–	acc. Param 27 LIN Spec. Rev. 2.1	P_11.3.13
Duty cycle 2	D_2	–	–	0.581	–	acc. Param 28 LIN Spec. Rev. 2.1	P_11.3.14
Duty cycle 3	D_3	0.417	–	–	–	acc. Param 29 LIN Spec. Rev. 2.1	P_11.3.15
Duty cycle 4	D_4	–	–	0.59	–	acc. Param 30 LIN Spec. Rev. 2.1	P_11.3.16
propagation delay of receiver rising edge	$t_{rx,pd,r}$	–	–	6	μs	acc. Param 31 LIN Spec. Rev. 2.1	P_11.3.17
propagation delay of receiver falling edge	$t_{rx,pd,f}$	–	–	6	μs	acc. Param 31 LIN Spec. Rev. 2.1	P_11.3.18
propagation delay symmetry of receiver	$t_{rx,pd,sym}$	-2	–	2	μs	acc. Param 32 LIN Spec. Rev. 2.1	P_11.3.19
TX Dominant Time Out Time	$t_{timeout}$	6	12	20	ms	min. data rate of 1600bit/s required	P_11.3.20
Bus Recessive Output Voltage	$V_{BUS,rec}$	$0.8*V_{BA}$ TPA	–	–	V		P_11.3.21
Bus Dominant Output Voltage	$V_{BUS,do}$	–	–	1.4	V	$V_{BATPA}=7V$ $R_{pu}=500\Omega$	P_11.3.22
Bus Dominant Output Voltage	$V_{BUS,do}$	–	–	2.2	V	$V_{BATPA}=18V$ $R_{pu}=500\Omega$	P_11.3.23
<i>LINIO</i> Input Capacitance	C_{LINIO}	–	15	25	pF	1)	P_11.3.24

Table 39 Electrical Characteristics: LIN (cont'd)

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over Temperature Switch Off Threshold	$T_{LIN,ot}$	150	–	200		1)	P_11.3.25
Over Temperature Hysteresis	$T_{LIN,ot,hys}$	–	10	–		1)	P_11.3.26

LINRX Output Characteristics

Low Level Output Voltage - Low Output Current	$V_{LINRX,L,l}$	–	–	0.4	V	$I_{LINRX} = 100\mu A$	P_11.3.27
Low Level Output Voltage - High Output Current	$V_{LINRX,L,h}$	–	–	1.5	V	$I_{VR_OUT} = 1mA$	P_11.3.28
High Level Output Voltage - Low Output Current	$V_{LINRX,H,l}$	VDDIO -0.4	–	–	V	$I_{LINRX} = -100\mu A$	P_11.3.29
High Level Output Voltage - High Output Current	$V_{LINRX,H,h}$	VDDIO -1.5	–	–	V	$I_{LINRX} = -1mA$	P_11.3.30

LINTX Input Characteristics

Low Level Input Voltage	$V_{LINTX,l}$	-0.3	–	0.9	V		P_11.3.31
High Level Input Voltage	$V_{LINTX,h}$	2	–	V_{VDDIO}	V		P_11.3.32
Input Voltage Hysteresis	$V_{IN,hys}$	50	200	–	mV		P_11.3.33
Pull Up Current	$I_{LINTX,pu}$	-100	–	-25	μA	$V_{LINTX}=0V$	P_11.3.34
Pull Up Current	$I_{LINTX,pu}$	–	–	-2.4	μA	$V_{LINTX}=V_{VDDIO}-0.6V$	P_11.3.35

1) Not subject to production test, specified by design

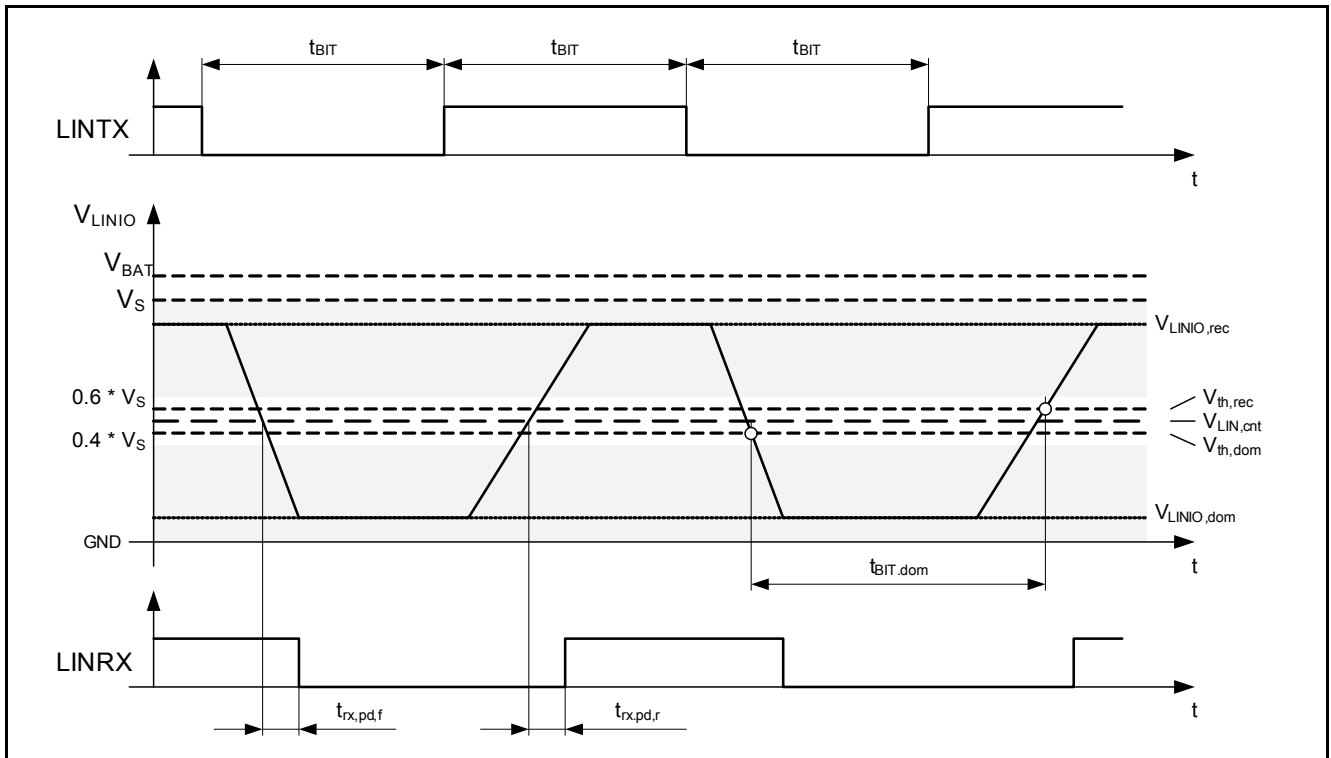


Figure 50 Timing Diagram of the LIN Interface

12 High Speed Controller Area Network (CAN) Transceiver

The Controller Area Network (CAN) is a serial bus system that connects micro controller, sensors and actuators for real-time control applications.

The integrated CAN interface provides the physical layer of the CAN according to ISO 11898. It is suitable for high speed differential data transmission and reception. It works as an interface between the CAN protocol controller and the physical bus lines.

Remote wake up function with a dominant signal at the bus lines is implemented.

12.1 Functional Description

The high speed CAN is a two wire differential network which allows data transmission rates up to 1Mbit/s. The input *CANTX* and the output *CANRX* are connected to the micro controller of the ECU. As shown in **Figure 51**, the CAN has a receive unit and a output driver stage, allowing the transceiver to send data to the bus line and monitor data from the bus lines at the same time. It converts the serial data stream available at the transmit data input *CANTX* into a differential output signal at *CANH* and *CANL*. The receiver stage monitors *CANH* and *CANL* and converts the differential voltage to a serial data stream at *CANRX*.

The supply of the CAN transceiver is done out of *V5VCAN*, the wake receiver is supplied out of *V5VSTBY*. The pin *V5VCAN* must be connected directly to the 5V supply pin *V5V*. In order to optimize EMC performance a ceramic capacitor *C_{V5VCAN}* should be connected to the pins *V5VCAN* and *PGND* (pin 50).

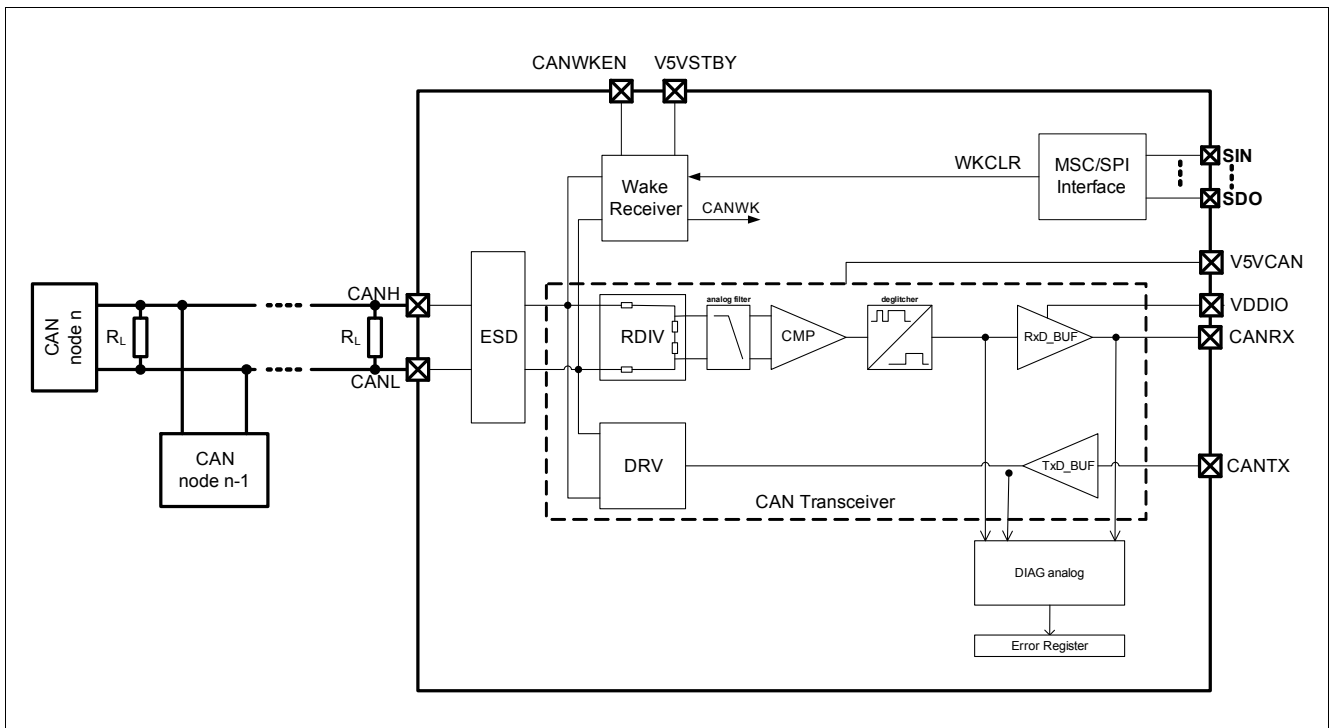


Figure 51 High speed CAN topology

12.2 Operation Modes

Four different operation modes are available. Regardless of the supply status the CAN interface does not disturb the communication on the bus line.

12.2.1 Normal Operation Mode

In normal operation mode the CAN transceiver sends the serial data stream available at the pin *CANTX* to the CAN bus while at the same time the data available at the CAN bus is monitored at the *CANRX* pin. In normal operation mode all functions are active:

- The driver output is active and drives data from the *CANTX* pin to the CAN bus.
- The receiver unit is active and provides the data from the CAN bus to the *CANRX* pin.
- The failure detection is active.

12.2.2 Receive Only Mode

In the receive only mode the CAN transceiver can still receive data from the bus, but the driver output stage is disabled and therefore no data can be sent to the CAN bus. All other functions are active:

- The driver output is disabled and data which is available at the *CANTX* pin will be blocked and not communicated to the CAN bus.
- The receiver unit is active and provides the data from the CAN bus to the *CANRX* pin.
- The failure detection is active.

12.2.3 Power Down Mode

If the TLE8888-1QK is not supplied the bus communication is not allowed to be disturbed. Therefore the resistors of the receiver unit are switched off and the bus input pins *CANH* and *CANL* are high resistive.

12.2.4 Remote Wake Up

The wake receiver is internally supplied from the standby supply pin *V5VSTBY*. The wake up function is enabled by an external connection of the pin *CANWKEN* to the standby supply pin *V5VSTBY*. The wake function is disabled by an external connection to *AGND* and the current consumption of the wake up circuit is reduced to leakage currents only.

In “ECU Sleep” state a dominant signal at *CANH* and *CANL* for longer than the **CAN Wake up filter time** preceded by a recessive signal causes an internal wake up and the internal wake signal **CANWK** is set. With a wake clear command (set bit **WKCLR** to “1” in command register **Cmd0**) **CANWK** is reset (status see bit **CANWK** in the status register **OpStat0**). The next wake up is only detected with a transition from recessive to dominant. With this implementation of the wake up procedure, bus line dominant clamping does not lead to permanent wake up.

In **Figure 52**, **Figure 53** and **Figure 54** the behavior is shown.

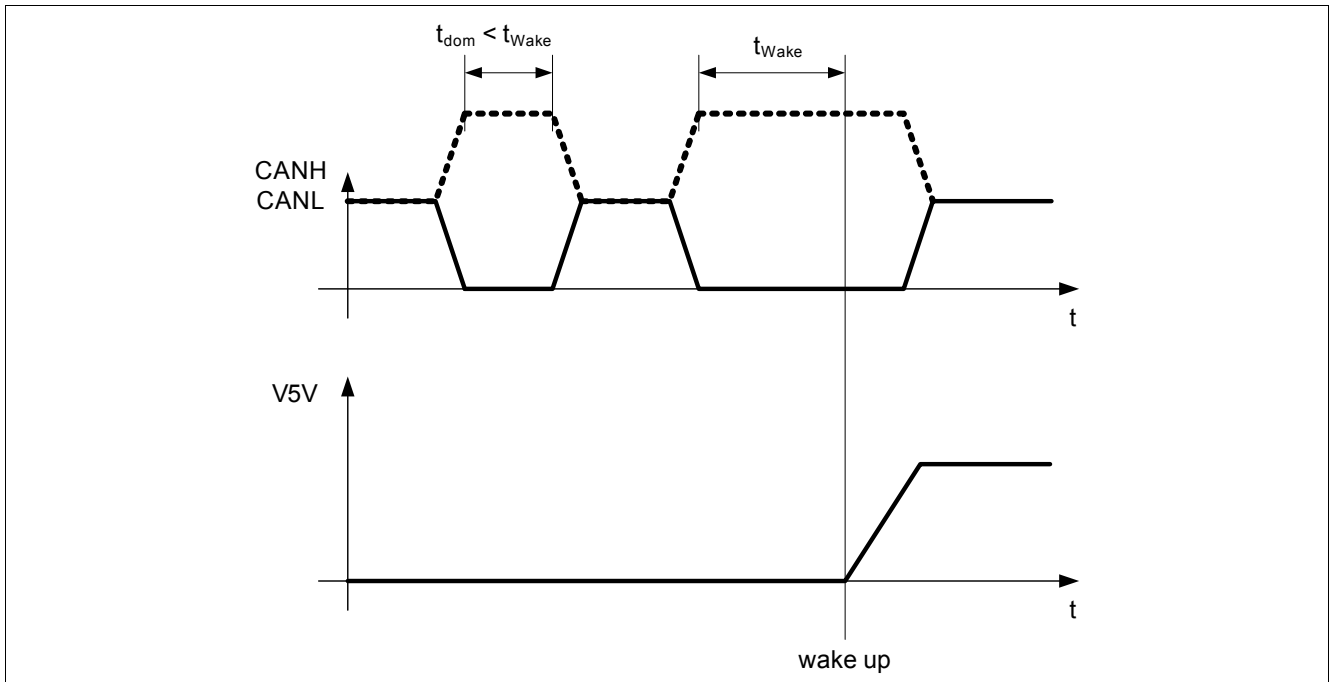


Figure 52 CAN Remote Wake Up

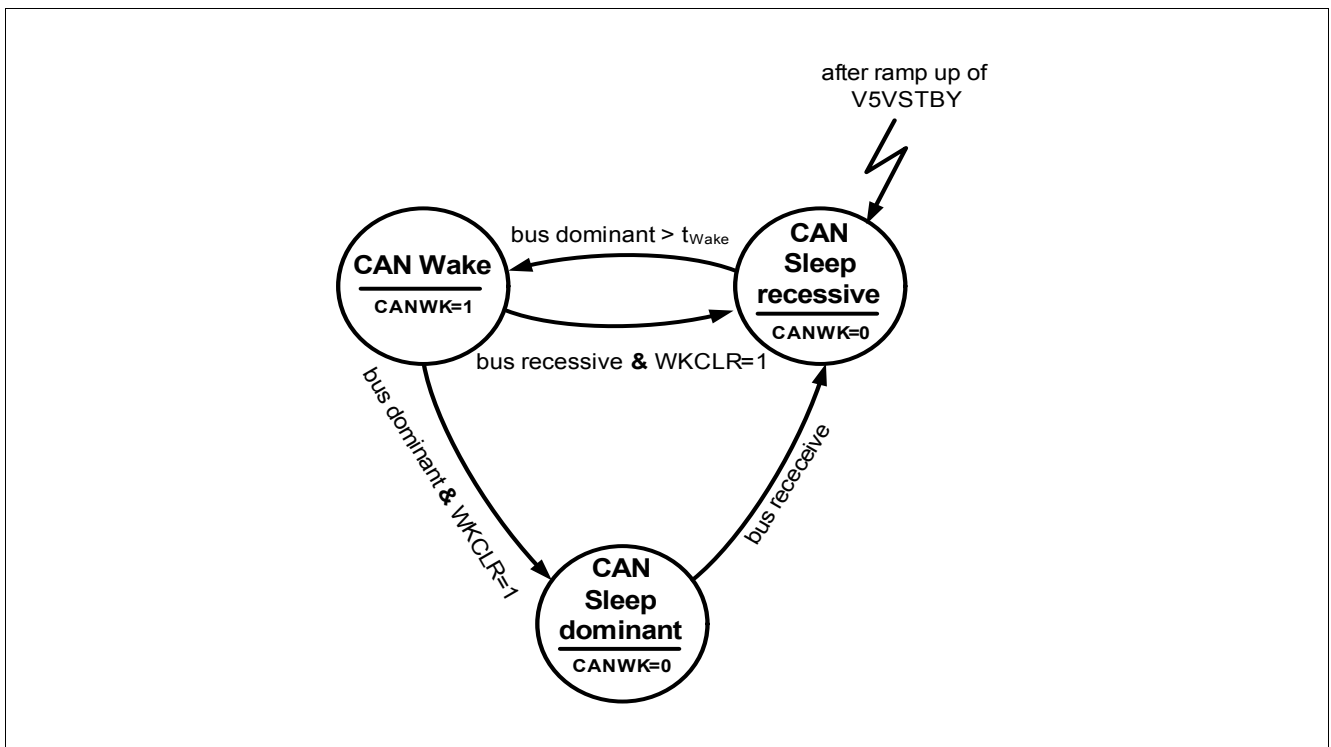


Figure 53 CAN Wake Up State machine

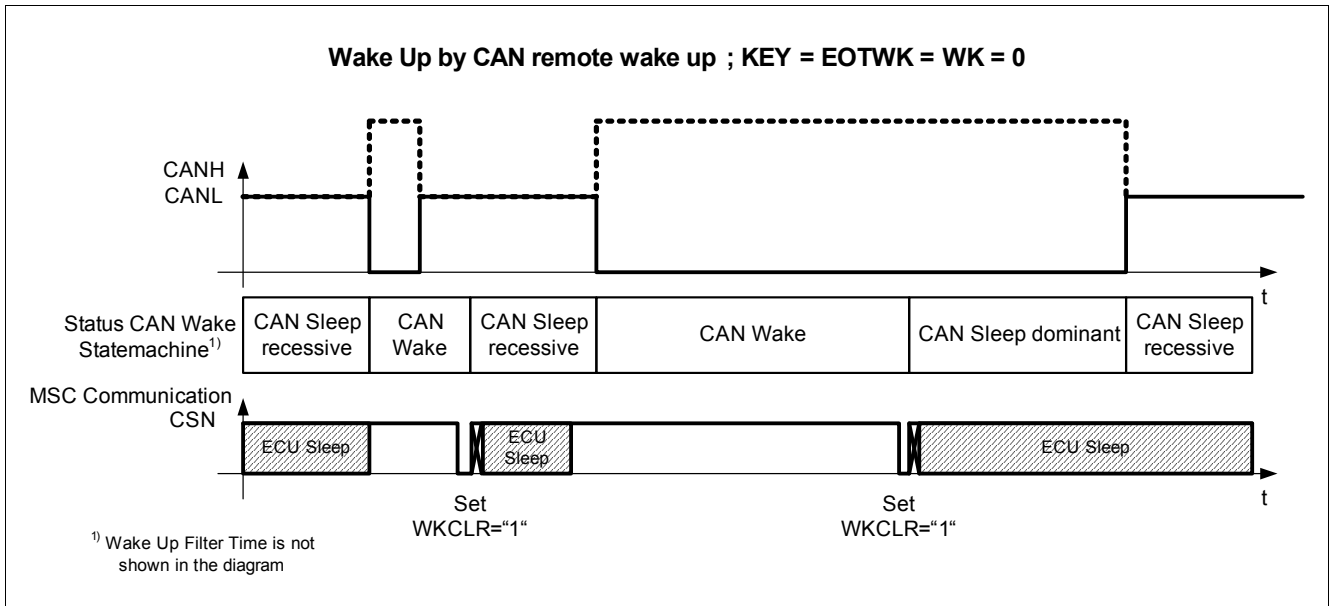


Figure 54 State Transitions at CAN Remote Wake Up

12.3 Diagnostic Functions

The CAN transceiver has an implemented diagnostic unit. Bus failures and local failures can be detected.

12.3.1 CAN Bus Failure Detection

In normal operation the CAN transceiver can detect following bus failure:

- Bus line dominant clamping (bit **CANBDC** in diagnosis register **ComDiag**)

Following bus failures can't be detected (outputs are protected):

- CANH shorted to GND
- CANL shorted to GND
- CANH shorted to low voltage supply
- CANL shorted to low voltage supply
- CANH shorted to V_{Bat}
- CANL shorted to V_{Bat}
- CANH open
- CANL open
- CANH shorted to CANL

12.3.2 Local Failure Detection

In normal operation the CAN transceiver can detect following local failures:

- CAN TX dominant time-out (bit **CANTXTO** in diagnosis register **ComDiag**)
- Over temperature (bit **CANOT** in diagnosis register **ComDiag**)

In case of failure detection only the corresponding diagnosis register bits are changed. No change in the configuration occurs.

12.4 Electrical Characteristics CAN Transceiver

Table 40 Electrical Characteristics: CAN Transceiver
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<i>CANH</i> voltage, recessive state	$V_{CANH,rec}$	2	2.5	3	V	no load	P_12.4.1
<i>CANL</i> voltage, recessive state	$V_{CANL,rec}$	2	2.5	3	V	no load	P_12.4.2
<i>CANH</i> voltage, dominant state	$V_{CANH,dom}$	2.75	3.5	4.5	V		P_12.4.3
<i>CANL</i> voltage, dominant state	$V_{CANL,dom}$	0.5	1.5	2.25	V		P_12.4.4
Differential output bus voltage, dominant state	$V_{diff,out,dom}$	1.5	2	3	V	$4.75V < V_{V5VCAN} < 5.25V$	P_12.4.5
Common mode bus voltage, dominant and recessive state	V_{CM}	-12	–	12	V	$4.75V < V_{V5VCAN} < 5.25V$	P_12.4.6
External Termination resistor	R_L	100	120	130	Ω		P_12.4.7
Differential input voltage, recessive state	$V_{diff,n,rec}$	-1	–	0.5	V		P_12.4.8
Differential input voltage, dominant state	$V_{diff,in,dom}$	0.9	–	5	V		P_12.4.9
Differential receiver hysteresis	$V_{diff,hys}$	20	100	–	mV		P_12.4.10
Common mode input resistance	R_{in}	5	–	50	k Ω		P_12.4.11
Bit time	t_B	1	–	–	μs		P_12.4.12
Propagation delay time <i>CANTX</i> to <i>CANRX</i> recessive to dominant	$t_{pd,rec,dom}$	–	–	255	ns		P_12.4.13
Propagation delay time <i>CANTX</i> to <i>CANRX</i> dominant to recessive	$t_{pd,dom,rec}$	–	–	255	ns		P_12.4.14
Propagation delay time <i>CANTX</i> to <i>CANH/CANL</i> recessive to dominant	$t_{pd,out,dom}$	–	–	140	ns	$T_j=25^\circ\text{C}^{1)}$ $C_{CANH/CANL} < 10\text{pF}$	P_12.4.15
Propagation delay time <i>CANTX</i> to <i>CANH/CANL</i> dominant to recessive	$t_{pd,out,rec}$	–	–	140	ns	$T_j=25^\circ\text{C}^{1)}$ $C_{CANH/CANL} < 10\text{pF}$	P_12.4.16
Bus line dominant clamping detection time	$t_{bus,cl,dom}$	4	–	7	ms		P_12.4.17
<i>CANTX</i> dominant detection time	$t_{CANTX,cl,dom}$	4	–	7	ms		P_12.4.18

High Speed Controller Area Network (CAN) Transceiver
Table 40 Electrical Characteristics: CAN Transceiver (cont'd)
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
$V_{5V}CAN$ buffer capacitance ¹⁾	C_{V5VCAN}		2	–	μF	recommended for optimized EMC performance	P_12.4.19
Over Temperature Switch Off Threshold	$T_{CAN,ot}$	150	–	200	$^\circ C$	¹⁾	P_12.4.20
Over Temperature Hysteresis	$T_{CAN,ot,hys}$	–	10	–	$^\circ C$	¹⁾	P_12.4.21
CANRX Output Characteristics							
Low Level Output Voltage - Low Output Current	$V_{CANRX,L,l}$	–	–	0.4	V	$I_{CANRX} = 100\mu A$	P_12.4.22
Low Level Output Voltage - High Output Current	$V_{CANRX,L,h}$	–	–	1.5	V	$I_{CANRX} = 1mA$	P_12.4.23
High Level Output Voltage - Low Output Current	$V_{CANRX,H,l}$	VDDIO -0.4	–	–	V	$I_{CANRX} = -100\mu A$	P_12.4.24
High Level Output Voltage - High Output Current	$V_{CANRX,H,h}$	VDDIO -1.5	–	–	V	$I_{CANRX} = -1mA$	P_12.4.25
CANTX Input Characteristics							
Low level input voltage	$V_{CANTX,l}$	-0.3	–	1	V		P_12.4.26
High level input voltage	$V_{CANTX,h}$	2	–	V_{V5VCAN}	V		P_12.4.27
Input voltage hysteresis	$V_{CANTX,hys}$	50	200	–	mV		P_12.4.28
Pull up current	$I_{CANTX,pu}$	-100	–	-25	μA	$V_{CANTX}=0V$	P_12.4.29
Wake Receiver							
Differential input voltage, recessive state, low power mode	$V_{diff,rec,lp}$	-1	–	0.4	V	$4.75V < V_{V5VSTBY} < 5.25V$	P_12.4.30
Differential input voltage, dominant state, low power mode	$V_{diff,dom,lp}$	1.15	–	5	V	$4.75V < V_{V5VSTBY} < 5.25V$	P_12.4.31
Common mode bus voltage, low power mode	$V_{CM,lp}$	-12	–	12	V	$4.75V < V_{V5VSTBY} < 5.25V$	P_12.4.32
CAN Wake up filter time	$t_{wake,CAN}$	0.75	–	5	μs	$4.75V < V_{V5VSTBY} < 5.25V$	P_12.4.33
Additional current consumption in low power mode at pin <i>BATSTBY</i>	I_{CANWK}	–	–	35	μA	$0V \leq V_{CANH} \leq 5V$, $0V \leq V_{CANL} \leq 5V$	P_12.4.34

¹⁾ Not subject to production test, specified by design

13 Micro Second Channel MSC

The bidirectional micro second channel (MSC) is a serial interface which is especially optimized to connect peripheral devices via serial link to micro controller. The serial communication link is built up by a fast synchronous downstream channel from micro controller to the device and an asynchronous upstream channel (referenced to downstream clock). The downstream interface can be “low voltage differential” (*FCLN*, *FCLP*, *SIN*, *SIP*, *CSN*) or “single ended” (*FCLP*, *SIP*, *CSN*).

Via MSC, the micro controller controls the outputs and logic of the device including the diagnosis and monitoring module. Read data is requested by micro controller via downstream communication and returned by the device via MSC upstream channel.

Multiple “power devices” with MSC for downstream operation are possible. The device is selected by *CSN*. The MSC logic is internally supplied and referenced to *AGND*.

The behavior of the MSC interface during reset is described in [Table 6](#) and [Table 7](#) in [Chapter 5.2](#).

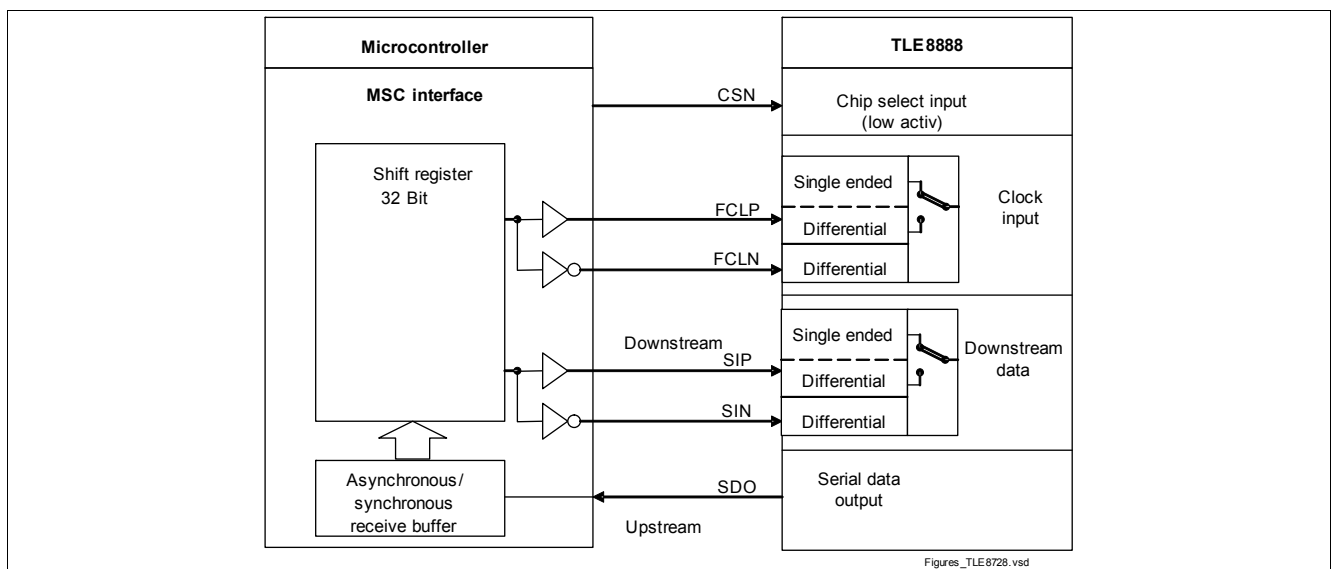


Figure 55 MSC Interface (not tested, overview only)

13.1 Downstream Communication

Downstream frames are synchronous serial frames with clock and data line.

The physical interface for downstream communication can be “low voltage differential” or “single ended” type. Both interface types are using individual pins (*FCLN*, *FCLP*, *SIN* and *SIP*) and common pins (*CSN* and *SDO*). For single ended interface *FCLN* and *SIN* have to be connected to *VDDIO*. For low voltage differential interface both input voltage levels must be within the defined input voltage range.

The frames and the behavior of the communication are the same in differential and single ended mode. Differential inputs for downstream data are *SIP* and *SIN*; the differential input signal *SIP* – *SIN* is the same logical signal as *SIP* alone in single ended mode and SI will be used in the description for both types of communication. The clock pins are *FCLP* and *FCLN*, the differential clock *FCLP* – *FCLN* is the same logical signal as *FCLP* in single ended mode and CLK will be used in the description for both types of communication.

There is one input *CSN* for chip select, and one output *SDO* for upstream data. The device is always the slave in this communication link.

The *CSN* signal enables receiver circuits automatically during a downstream frame transmission.

Two types of downstream frames are defined:

- Command frames (selection bit =“1”)
- Data frames (selection bit =“0”)

The device MSC uses non inverting polarity for SI and CLK: SI changes its state with the rising edge of CLK and is sampled with the falling edge; a logic ‘1’ is a ‘high level’ on SI, and a logic ‘0’ is a ‘low level’ on SI. Data at SI is latched by the device on the falling edge of CLK.

The *CSN* input is active low during the active phases of command or data frames. An active enable signal validates the SI input signal. Outside the active phase (*CSN* line is at high level) data at SI is ignored.

It is possible to drive multiple “power devices” with shared CLK and SI lines and individual *CSN* signal.

Command frames and data frames may be sent in any sequence (with a passive phase of at least 2 CLK-cycles after each frame).

Table 41 Execution of commands

Event on MSC downstream	upstream busy	upstream idle
valid read command frame	ignored	executed
valid write command frame	executed ¹⁾	executed
valid data frame	accepted	accepted
invalid command	ignored	ignored
invalid data frame	ignored	ignored

1) only after $t_{prep,sr}$ or $t_{prep,mr}$, see also [Chapter 13.2](#)

The serial clock CLK must be active (toggling) during upstream communication even when no command frame or data frame is transmitted.

The clock period of CLK is defined as t_{FCL} , maximum downstream clock rate is f_{FCLmax} .

The active phase of a downstream frame starts with the falling edge of the signal on *CSN* and ends with the rising edge. *CSN* changes its state with the rising edge of clock CLK.

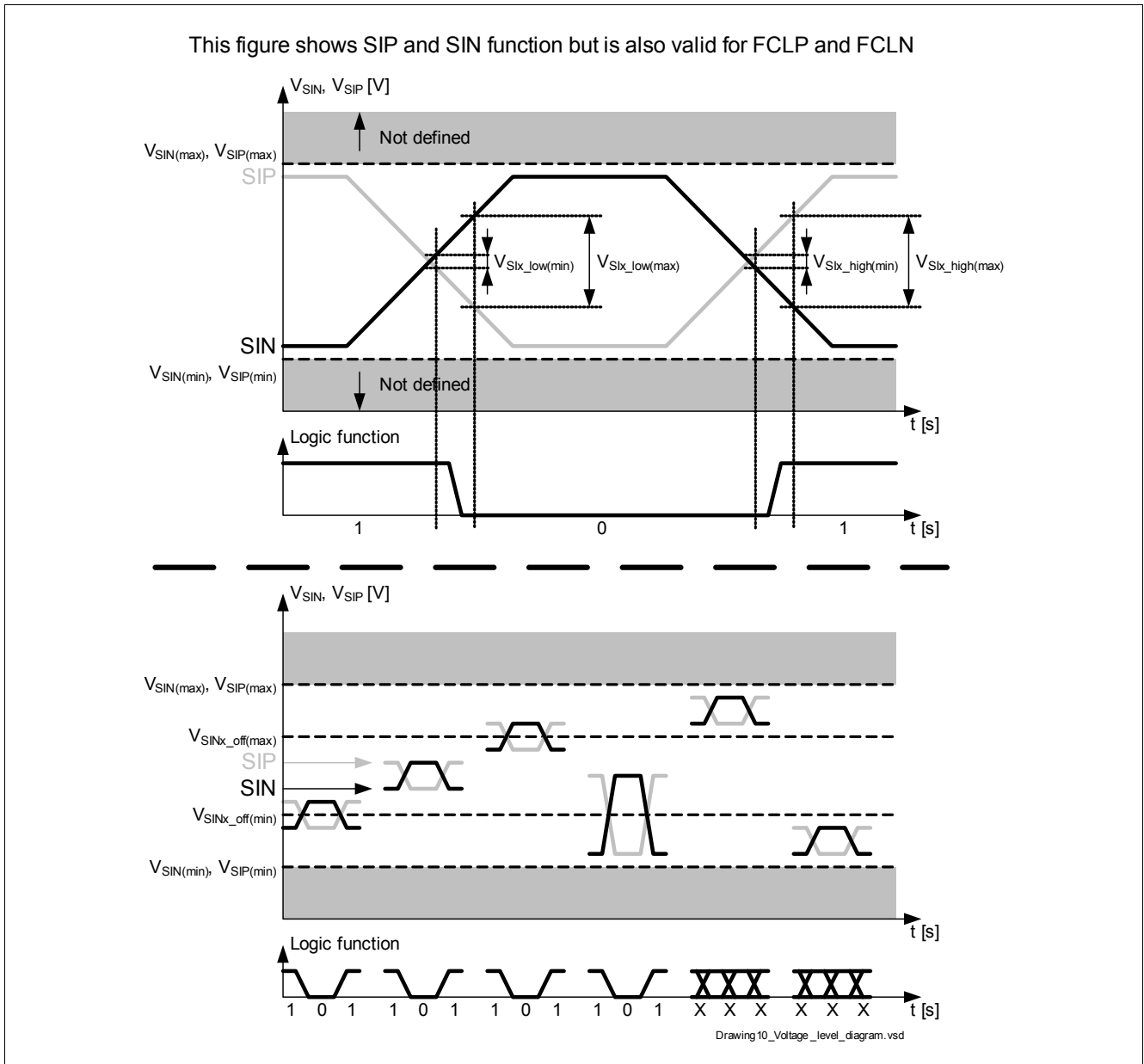


Figure 56 Voltage level diagram

13.1.1 Downstream Supervisory Functions

A command- or data frame is interpreted as valid, if it has the correct number of CLK pulses (a frame has a length of 17 clock pulses). Clock pulses are counted at the falling edge of the signal.

There is no parity check.

If TLE8888-1QK receives no valid data frame for $t > t_{MSC_mon}$, the device switches off the output stages (all output stage control bits are set to "0"), the bits **01E** to **024E** in the configuration registers **OEConfig0** to **OEConfig3** are set to "0" and the MSC time out failure bit in the register **ComDiag** is set to "1". The MSC time out failure bit is reset by a readout of the register **ComDiag** and all output stages remain off. For switching on the stages the bits **01E** to **024E** in the configuration registers **OEConfig0** to **OEConfig3** must be set to "1" and the control bits must be set. Outputs which are configured to be driven directly with the direct drive inputs are switched according the input level of the pins **INI** to **INI2** after set of the bits **01E** to **024E**.

13.1.2 Command Frame

A command frame always starts with a high level bit (command selection bit). The number of command bits of the active phase of a command frame is fixed to 16. A command is executed only if the number of transmitted bits of an active command frame is equal to 17.

The length of the command frame's passive phase t_{CPP} must be a minimum of $2 * t_{FCL}$ (2 clock pulses).

Alternatively the passive phase can consist in $t_{CPP} = t_{FCL}$ (1 clock pulse) followed by a frame of wrong length (4...8 bits, with or without *CSN* active low) and a second $t_{CPP} = t_{FCL}$ (1 clock pulse).

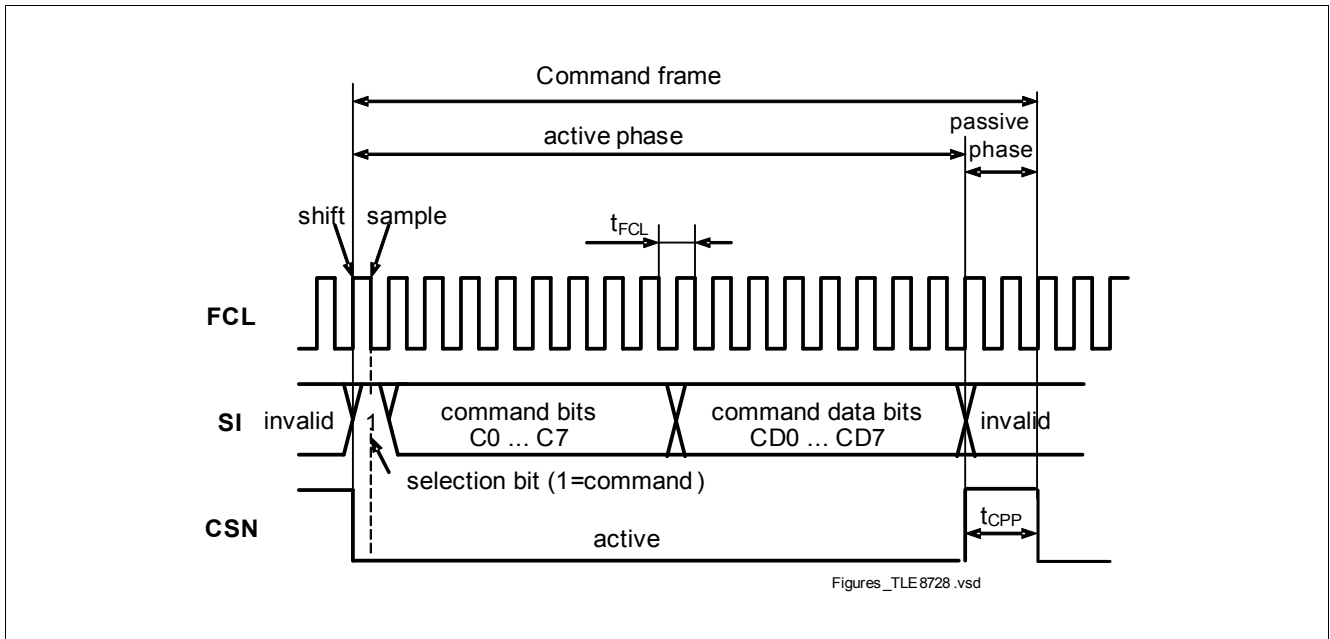


Figure 57 MSC command frame

Content of a command frame (LSB transmitted first)

Table 42 Command frame

Bit #	Description
0 (first bit)	= '1': command selection bit
1...8	Command [C0 ... C7]
9...16	Data for the command [CD0 ... CD7]

The least significant (LSB) bit of a command is transmitted first

13.1.3 Data Frame

A data frame always starts with a low level bit (data selection bit). The number of the data bits of the active phase of a data frame is fixed to 28 bit.

A data frame is accepted if the actual length is the expected length 29.

MSC Monitoring t_{MSC_mon} is re triggered by any data frame with correct length (no other error detection mechanism is implemented).

The length of the data frame's passive phase t_{DPP} must be a minimum of $2 * t_{FCL}$ (2 clock pulses).

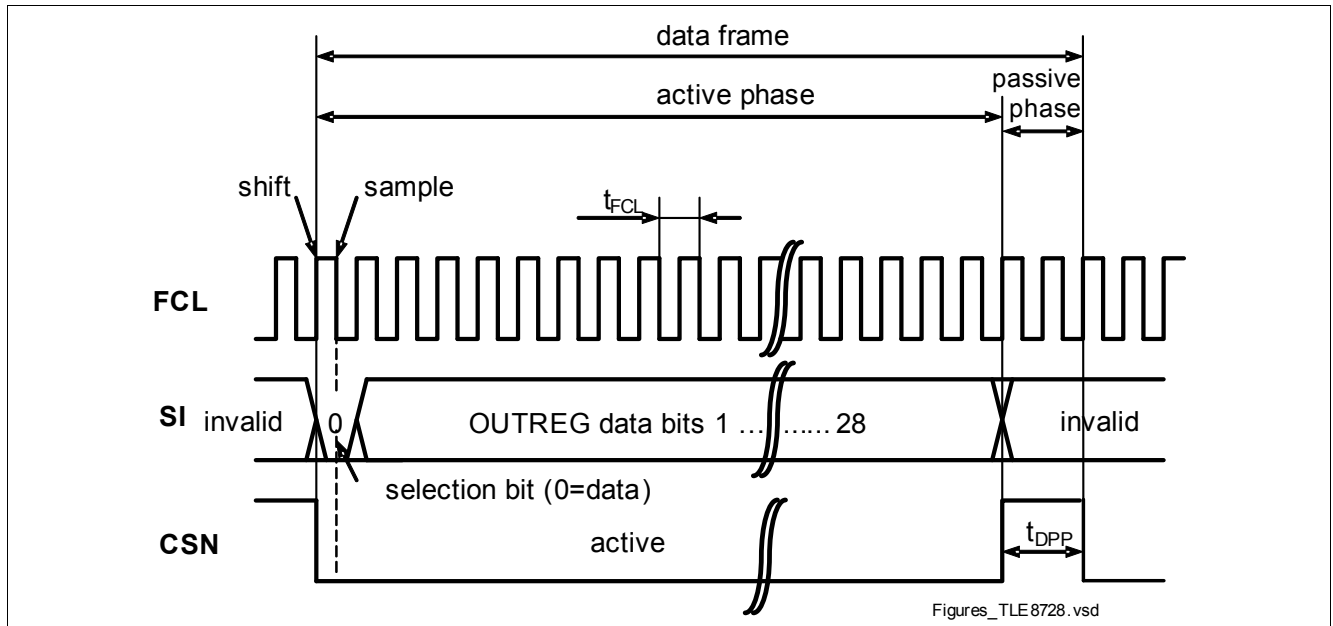


Figure 58 MSC data frame

Table 43 Data frame

OUTREG Bit	Description
0 (first bit)	= '0': data selection bit
1	O14ON¹⁾
2	O11ON¹⁾
3	O24ON¹⁾
4	O13ON¹⁾
5	IGN1ON¹⁾
6	IGN2ON¹⁾
7	O5ON¹⁾
8	O1ON¹⁾
9	O15ON¹⁾
10	IGN3ON¹⁾
11	O2ON¹⁾
12	O22ON¹⁾
13	O9ON¹⁾
14	O23ON¹⁾
15	O19ON¹⁾
16	O16ON¹⁾
17	O18ON¹⁾
18	O20ON¹⁾
19	O8ON¹⁾
20	O4ON¹⁾
21	O17ON¹⁾
22	O10ON¹⁾
23	O21ON¹⁾

Table 43 Data frame (cont'd)

OUTREG Bit	Description
24	O7ON ¹⁾
25	O6ON ¹⁾
26	O3ON ¹⁾
27	IGN4ON ¹⁾
28	O12ON ¹⁾

1) Definition see [Chapter 14.6](#).

There is no parity bit in the data frame.

The data is stored in the control register [Cont0](#) to [Cont3](#).

13.2 Upstream Communication

The serial data output *SDO* is the synchronous serial data signal of the upstream channel and is always single ended. The polarity is ‘non inverting polarity’– i.e. a low level bit at *SDO* is stored in the micro controller as a logic ‘0’, and a high level bit at *SDO* is stored in the micro controller as a logic ‘1’. The frequency for *SDO* is derived from CLK by an internal divider and can be configured via MSC.

The output of *SDO* can be configured as an open drain or an push pull output. The set is done with the bit [MSCO](#) in the configuration register [ComConfig0](#). The full range of up stream frequency divider settings in the configuration register [ComConfig0](#) bits [MSCF](#) is valid for the push pull output configuration.

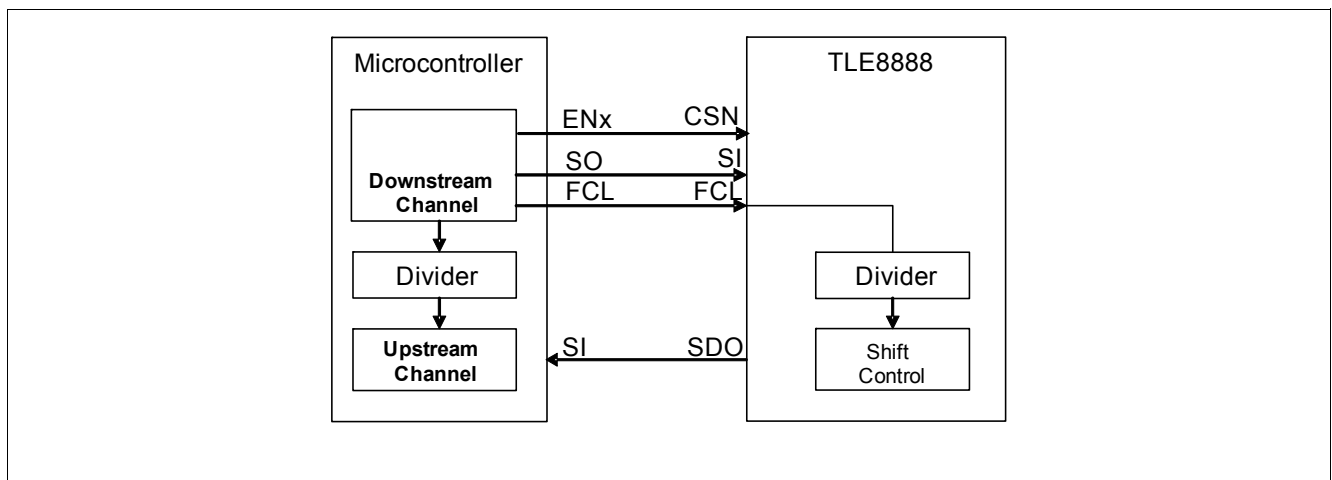


Figure 59 MSC upstream communication (not tested, overview only, Single Ended)

The data frame could be defined with 12 and 16 bit according the setting of [MSCUF](#) in the configuration register [ComConfig0](#). In [Figure 60](#) the formats are shown. The address bits A2 and A3 are used for the selection of the upstream data register in the micro controller.

Definition of Address Bits A0 to A3 in 16 Bit Upstream Mode:

- **Fixed A0 to A3 Value:**
The value of the address bits A0 to A3 is fixed according the definition of [MSCA](#) in the configuration register [ComConfig1](#) at the rising edge of *CSN* of the read command. For read out with multiple read out commands the value of A0 to A3 does not change.
- **Multiple Read Command Mode:**
This mode is especially for the multiple read commands and the configuration of the micro controller in UD3 interrupt mode. A2 and A3 are used in this mode to define the upstream data register (UD0 -UD3) and a number of n times 4 of upstream frames. A0 is defined as read overflow and A1 is defined as read busy.

Table 44 Definition of A0 in Multiple Read Command Mode for 16 Bit Upstream Format

A0	Description
0	No read command is ignored
1	A read command was sent during upstream communication. This read command was ignored and this is signaled with A0=1

Table 45 Definition of A1 in Multiple Read Command Mode for 16 Bit Upstream Format

A1	Description
0	last upstream frame; after finish of this frame next transmitted read command will be executed
1	Upstream activities required by an multiple read commands are ongoing

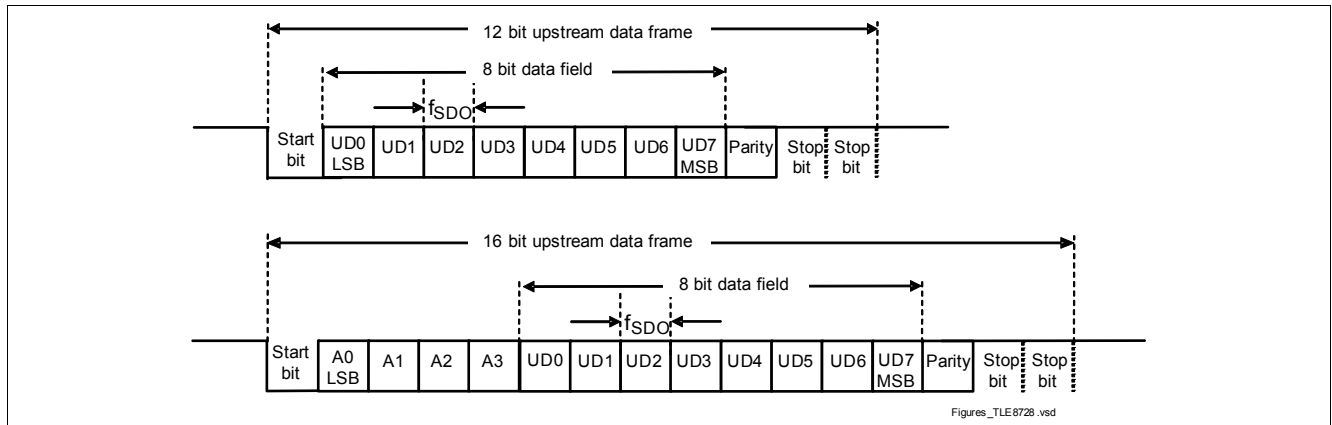


Figure 60 MSC upstream frame

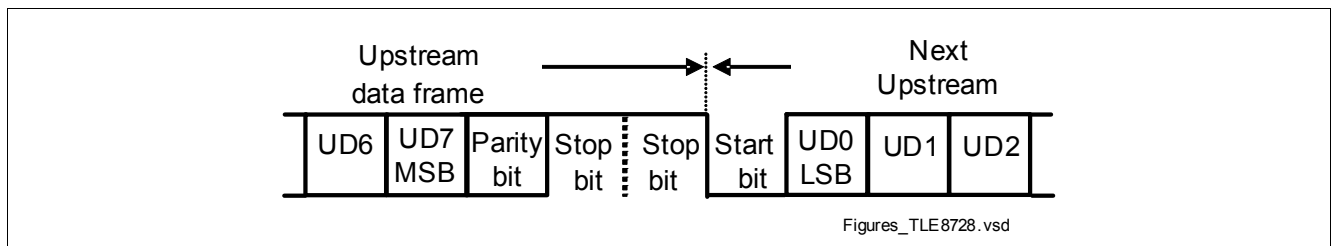


Figure 61 MSC upstream communication flow

Table 46 12 Bit Upstream Frame

Bit	description
0	start bit, always '0'
1-8	upstream data bits UD0..7
9	parity bit (The parity bit is set in order to achieve an even number of '1' in Bits UD0..7+Parity)
10, 11	stop bits, always '1'

Table 47 16 Bit Upstream Frame

Bit	description
0	start bit, always '0'
1-4	address bits A0..3

Table 47 16 Bit Upstream Frame (cont'd)

Bit	description
5-12	upstream data bits UD0..7
9	parity bit (The parity bit is set in order to achieve an even number of '1' in Bits UD0..7+Parity)
10, 11	stop bits, always '1'

Transmission of the registers via upstream starts within t_{MSC_RSP} after read command has been received. During an ongoing upstream communication the device will ignore further read commands until the upstream data transfer is finished. A new read command is accepted if the rising edge CSN arrives after the last stop bit has been sent. Data frames are executed independently of ongoing read requests. Write commands are ignored during **MSC upstream preparation time for single read command $t_{prep,sr}$** or **MSC upstream preparation time for multi read command $t_{prep,mr}$** (see Figure 62). After that time the write commands are executed also during ongoing upstream communication. If the write command is changing the register which is in transmission, the old register content will be sent. With setting the command bit **MSCUPS** in the command register **Cmd0** the running upstream transmission is stopped and all remaining read request of a multiple read command are cleared.

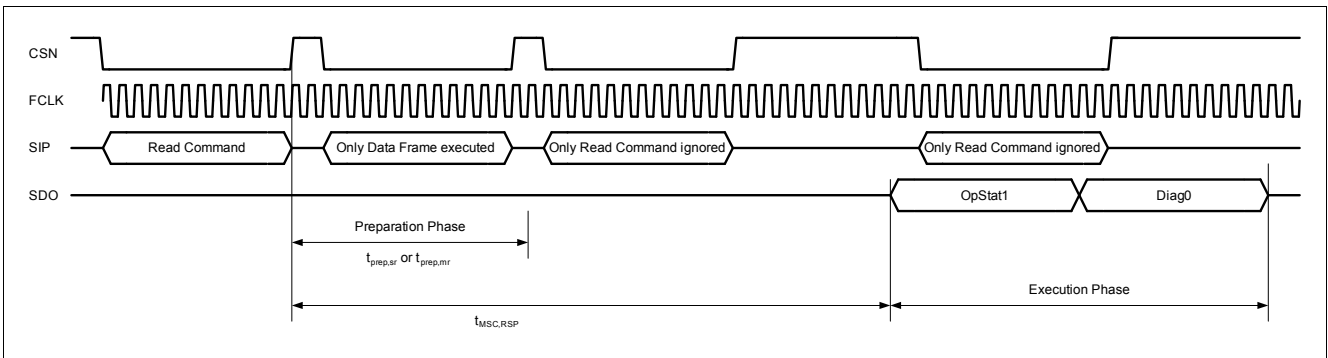


Figure 62 Example MSC upstream and active downstream communication

13.3 Timing Characteristics

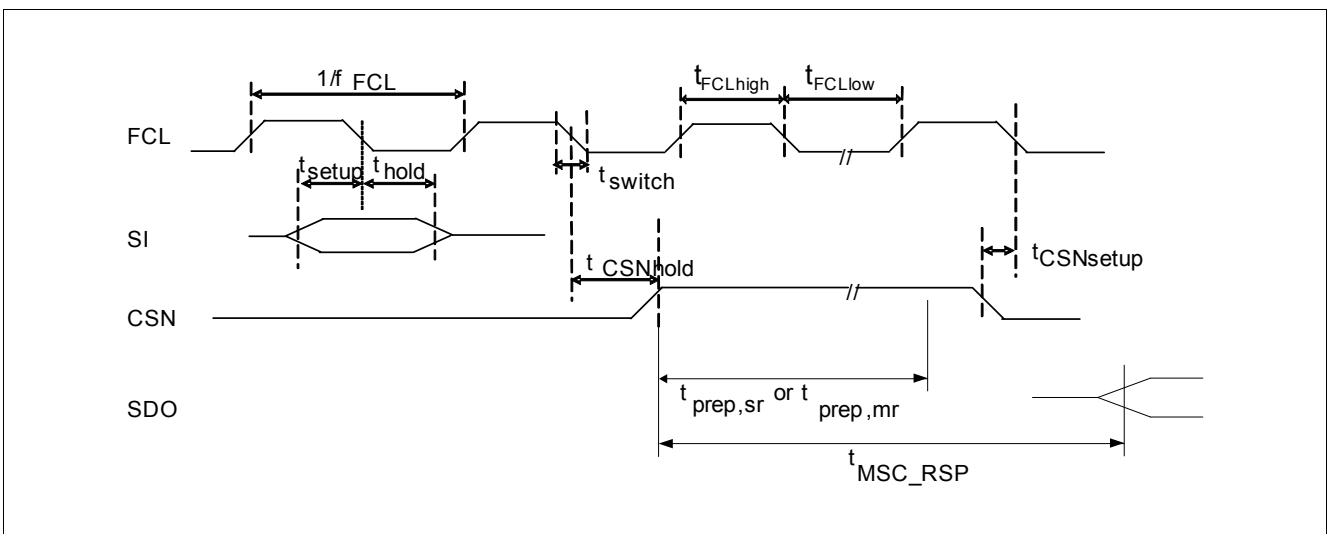


Figure 63 MSC timing

The downstream clock within the device must be active during an upstream data frame transmission (i.e. each answer to a READ command).

The upstream response time t_{MSC_RSP} describes the time between end of read command (rising edge of CSN) to beginning of up-stream communication (falling edge of start bit).

13.4 Electrical Characteristics

Table 48 Electrical Characteristics: Micro Second Channel

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pin CSN							
Input comparator low level	V_{CSN_low}	-0.3	–	0.8			P_13.4.1
Input comparator high level	V_{CSN_high}	1.6	–	5.5	V	–	P_13.4.2
Input comparator hysteresis	V_{CSN_hys}	0.1	–	0.5	V	–	P_13.4.3
Input capacitance ¹⁾	C_{CSN}			12	pF	–	P_13.4.4
Input current Internal pull up current source to $VDDIO$	I_{CSN}	-25	–	-3	μA	$0V < V_{CSN} < 2V$	P_13.4.5
Pins $FCLP$, $FCLN$ MSC Differential Mode							
Input voltage range	V_{FCLP} , V_{FCLN}	0.8	–	1.6	V	–	P_13.4.6
Differential input high detection level, $V_{FCLx_high} = V_{FCLP} - V_{FCLN}$	V_{FCLx_high}	–	–	125	mV	–	P_13.4.7
Differential input low detection level, $V_{FCLx_low} = V_{FCLP} - V_{FCLN}$	V_{FCLx_low}	-125	–	–	mV	–	P_13.4.8
Differential input hysteresis	V_{FCLx_hys}	50		200	mV		P_13.4.53
Input voltage offset, $V_{FCLx_off} = 0.5 * (V_{FCLP} + V_{FCLN})$	V_{FCLx_off}	1.05	–	1.4	V	–	P_13.4.9
Differential capacitance between; $FCLP$ and $FCLN$	C_{FCLx}	–	–	8	pF	¹⁾	P_13.4.10
Input pull down current	I_{FCLN}	3	–	25	μA	$1V < V_{FCLx} < V_{VDDIO}$	P_13.4.12
Pins $FCLP$ Single Ended Mode							
Input comparator low level	V_{FLCP_low}	-0.3	–	0.8			P_13.4.13
Input comparator high level	V_{FLCP_high}	1.6	–	5.5	V	–	P_13.4.14
Input comparator hysteresis	V_{FLCP_hys}	0.1	–	0.5	V	–	P_13.4.15
Input capacitance	C_{FLCP}			12	pF	¹⁾	P_13.4.16
Input pull down current	I_{FLCP}	3	–	25	μA	$1V < V_{FLCP} < V_{VDDIO}$	P_13.4.17
Clock Frequency							
$FCLP$, $FCLN$ frequency	f_{FCLx}	–	–	23	MHz		P_13.4.18

Table 48 Electrical Characteristics: Micro Second Channel (cont'd)
 $V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
FCL frequency single ended mode	f_{FCL}	–	–	12.5	MHz		P_13.4.19
Pins <i>SIP</i>, <i>SIN</i> MSC Differential Mode							
Input voltage range	V_{SIP}, V_{SIN}	0.8	–	1.6	V	–	P_13.4.20
Differential input high detection level, $V_{SIX_high} = V_{SIP} - V_{NSI}$	V_{SIX_high}	–	–	125	mV	–	P_13.4.21
Differential input low detection level, $V_{SIX_low} = V_{SIP} - V_{SIN}$	V_{SIX_low}	-125	–	–	mV	–	P_13.4.22
Differential input hysteresis	V_{SIX_hys}	50	–	200	mV		P_13.4.54
Input voltage offset, $V_{SIX_Off} = 0.5 * (V_{SIP} + V_{SIN})$	V_{SIX_Off}	1.05	–	1.4	V	–	P_13.4.23
Differential capacitance between SIP and SIN	C_{SIX}	–	–	8	pF	1)	P_13.4.24
Input pull down current	I_{SIN}	3	–	25	μA	$1V < V_{SIX} < V_{VDDIO}$	P_13.4.26
Pin <i>SIP</i> Single Ended Mode							
Input comparator low level	V_{SIP_low}	-0.3	–	0.8			P_13.4.27
Input comparator high level	V_{SIP_high}	1.6	–	5.5	V	–	P_13.4.28
Input comparator hysteresis	V_{SIP_hys}	0.1	–	0.5	V	–	P_13.4.29
Input capacitance	C_{SIP}			12	pF	1)	P_13.4.30
Input pull down current	I_{SIP}	3	–	25	μA	$1V < V_{SIP} < V_{VDDIO}$	P_13.4.31
Pin <i>SDO</i> open drain set up							
SDO output low level	$V_{SDO_low}; V_{SDO_low}$	–	–	0.8	V	$I_{SDO} < 4mA;$	P_13.4.32
		–	–	0.4	V	$I_{SDO} < 1mA$	P_13.4.33
SDO passive output high voltage	$V_{SDO_high,p}$	$V_{DDIO} - 1.5$	V_{DDIO}	–	V	no load	P_13.4.34
Output current capability	I_{SDO_max}	15 ²⁾	–	–	mA	$V_{SDO}=5V$ and $V_{VDDIO}=5V$	P_13.4.35
SDO pull-up current source	I_{SDO_high}	-50	–	-10	μA	$0V < V_{SDO} < 2V$, SDO in tristate, pull up to <i>VDDIO</i>	P_13.4.36
SDO (high level = inactive) pin capacity	C_{SDO}	–	–	10	pF	measured with bias voltage of 1V ¹⁾	P_13.4.37
SDO frequency; maximum upstream frequency with external pull-up	f_{SDO}	500	–	–	kHz	2.2k Ω and $C_L = 15pF$ ¹⁾	P_13.4.38
Pin <i>SDO</i> push pull set up							

Table 48 Electrical Characteristics: Micro Second Channel (cont'd)

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SDO output low level	$V_{SDO_low};$	–	–	0.8	V	$I_{SDO}<4mA;$	P_13.4.39
	V_{SDO_low}	–	–	0.4	V	$I_{SDO}<1mA$	P_13.4.40
SDO active output high voltage	$V_{SDO_high,a}$	$V_{DDIO} - 0.4$	–	–	V	$I_{SDO}=100\mu A$	P_13.4.41

Timing Characteristics³⁾

Data hold time	t_{hold}	10	–	–	ns	–	P_13.4.42
Data Setup time	t_{setup}	10	–	–	ns	–	P_13.4.43
Switching time	t_{switch}	–	–	3	ns	1)	P_13.4.44
FCL low time	t_{FCLlow}	13	–	–	ns	–	P_13.4.45
FCL high time	$t_{FCLhigh}$	13	–	–	ns	–	P_13.4.46
CSN setup time	$t_{CSNsetup}$	10	–	–	ns	–	P_13.4.47
CSN hold time	$t_{CSNhold}$	10	–	–	ns	–	P_13.4.48
MSC data time-out monitoring	t_{MSC_mon}	60	–	135	μs	–	P_13.4.49
MSC upstream preparation time for single read command	$t_{prep,sr}$	–	–	$0.9 + 4 * t_{FCL}$	μs	–	P_13.4.11
MSC upstream preparation time for multi read command	$t_{prep,mr}$	–	–	$1.8 + 4 * t_{FCL}$	μs	–	P_13.4.25
MSC upstream response time; up-stream divider independent	t_{MSC_RSP}	–	–	100	μs	–	P_13.4.50
Required idle time after command	t_{CPP}	$2/f_{FCL}$ (2 clock pulses)	–	–	s	–	P_13.4.51
Required idle time after data frame	t_{DPP}	$2/f_{FCL}$ (2 clock pulses)	–	–	s	–	P_13.4.52

1) not subject to production test, specified by design

2) Application must ensure that current into this pin does not exceed this value.

3) See [Figure 57](#), [Figure 58](#) and [Figure 63](#)

14 Register and Commands

In [Chapter 14.1](#) to [Chapter 14.6](#) detailed descriptions and definitions of the registers and commands are shown. General definition for all registers and commands are described below.

Offset Address

The offset address used for the register address is mapped to the command bits from C1 to C7. In [Figure 64](#) an example is shown. Maximum allowed address is $7F_H$.

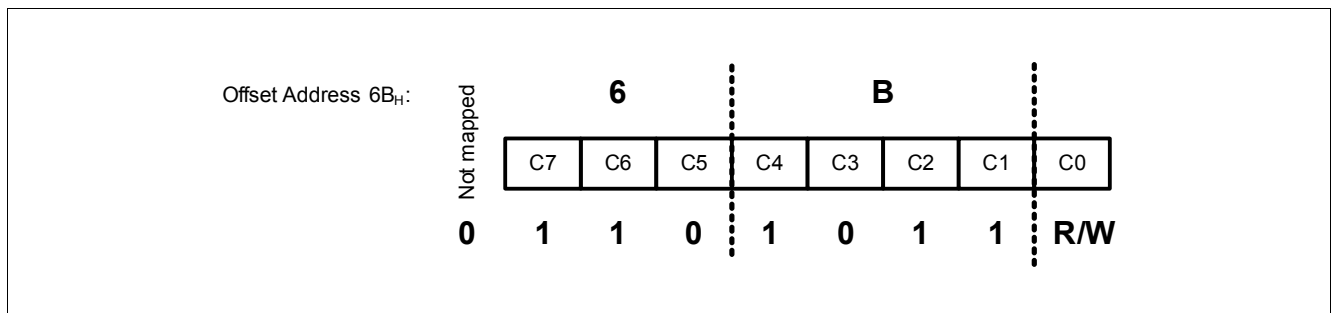


Figure 64 Mapping Offset Address to the Command Bits

Read Access

A read access to a register is done by sending a “0” for the bit C0 of the command frame of the MSC or the SPI frame. All register bits are updated constantly. With the positive edge of *CSN* of a valid read command the internal register information is loaded into the output shift register. The communication via *SDO* to the micro controller is according to the serial interface mode MSC or SPI. Therefore the read information is related to the time of the positive edge of *CSN*.

Write Access

A write access to a register is done by sending a “1” for the bit C0 of the command frame of the MSC or the SPI frame or with the data frame of the MSC communication. With the positive edge of *CSN* of a valid write access for read/write register the bits are set and for command registers the defined function is executed (e.g. multiple read command).

Command Register

These registers are write only registers. Following functions are executed:

- **Main relay switching with bits *MRON* and *MRSE* in command register *Cmd0***: In all states where a serial communication with the TLE8888-1QK is allowed the main relay can be switched. This is done by enabling the command with a “1” for *MRSE* and a “0” for switch off or a “1” for switch on for *MRON*. Switch off of the main relay leads for an application with supply of the ECU over the main relay path to a power down.
- **VRS diagnosis start with bit *VDIAGS* in command register *Cmd0***: With a “1” the VRS diagnosis is started. A “0” leads to no action.
- **Stop of a MSC upstream communication with bit *MSCUPS* in command register *Cmd0***: With a “1” the upstream communication is stopped immediately. This leads during an upstream to invalid communication. This command is implemented to stop especially multiple read communication. A “0” leads to no action. For SPI mode this command has no effect.
- **Start of the engine off timer with bit *EOTS* in command register *Cmd0***: With a “1” the engine off timer is started if the configuration is set accordingly. A “0” leads to no action.
- **Restart of the delayed off timer with bit *RDOT* in command register *Cmd0***: With a “1” the delayed off timer is reset and started again. A “0” leads to no action.

- **Wake up signal clear with bit WKCLR in command register Cmd0:** With a “1” all internal wake up signals (WKINT, CANWK, EOTWK) are reset. A “0” leads to no action.
- **Response write command FWDRspCmd and FWDRspSyncCmd:** With the write access to these registers the 8 bit response byte is sent to the TLE8888-1QK. The interpretation of the sent response byte is done according the description in [Chapter 6](#).
- **Multiple read command MSCReadWd0 to MSCReadWd1:** Multiple read commands are only allowed for MSC setup of the serial interface. The number of read register is defined by a “1” in the data bits of the command. The chosen register is sent in the order MSB down to LSB (see [Figure 65](#)). In SPI setup a multiple read command is an invalid communication. During a multi read upstream read commands are ignored, write commands are allowed. To stop an upstream operation use the command **MSCUPS**.
- **Software reset command CmdSR:** With the execution of this command the software reset of the TLE8888-1QK is performed according [Table 7](#) in [Chapter 5](#).
- **Central output enable command CmdOE:** With the execution of this command the central output enable bit is set or reset. For the description of the functionality see [Chapter 9.2](#). The status of the central enable bit is available in register **OpStat1**.
- **Lock command CmdLOCK:** With the execution of this command the lock bit is set or reset. This bit is used to lock some configuration registers (see [Table 50](#)) to avoid a change of these register e.g. during operation. The status of the lock bit is available in register **OpStat1**.

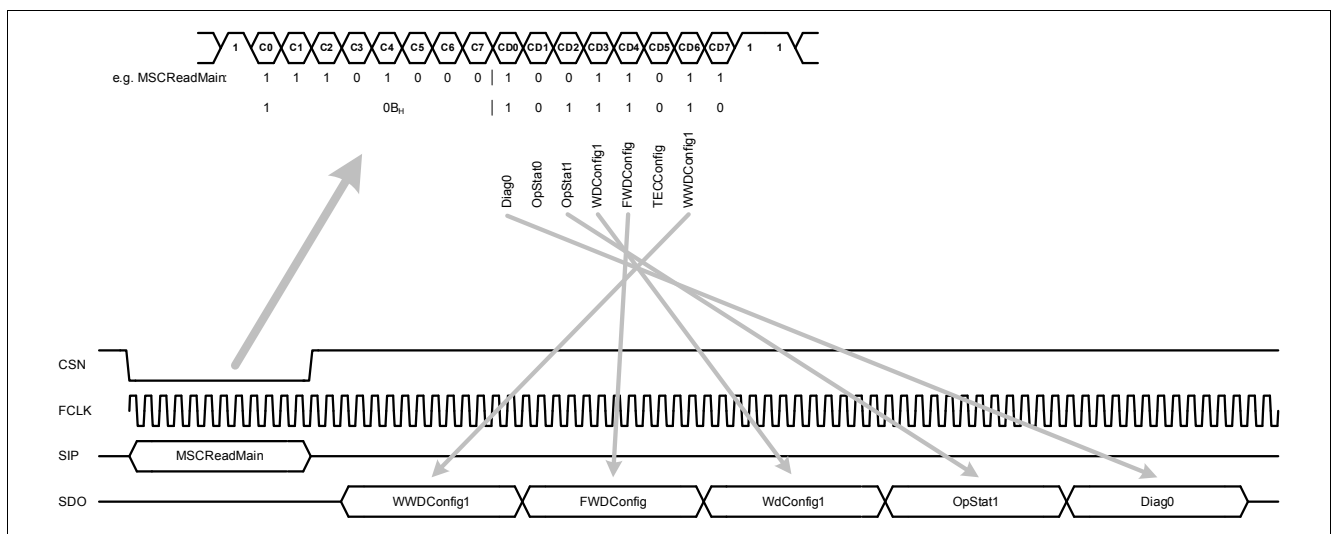


Figure 65 Example of a Multi read Command

Diagnosis Register

The diagnosis register bits are set according the asynchronous detection circuits. The reset of the diagnosis bits is done with the read out of the registers if the failure condition is not detected anymore.

Central Over-temperature Bit COT in Diagnosis Register Diag0

The central over temperature bit is an OR combination of all over temperature detection signals which leads to active diagnosis bits. With at least one active over-temperature diagnosis the central over-temperature bit is “1”, with no active over-temperature diagnosis this bit is “0”. All other diagnosis signals doesn’t change the status of the central over-temperature bit.

Central Failure Bit **CF** in Diagnosis Register **Diag0**

The central failure bit is an OR combination of diagnosis bits (see [Table 49](#)). If one or more of these diagnosis bits are active then the central failure bit is “1”. If all are inactive the central failure bit is “0”. The over-temperature diagnosis doesn’t change the status of the central failure bit.

Table 49 Overview of Diagnosis Registers and Bits affecting the Central Failure Bit

Register	Offset	Bit(s)	Note
ComDiag	024_H	MSCTO, COMFE, CANBDC, CANTXTO	
OutDiag0 to OutDiag4	026_H to 029_H	all bits	central failure bit not set if only over-temperature is detected
PPOVDiag	02A_H	all bits	
BriDiag0	02B_H	all bits	
BriDiag1	02C_H	only over-current bits	
IgnDiag	02D_H	all bits	
WdDiag	02E_H	WWDTO, WWDSCE, FWDREL, FWDREA	

Engine Off Timer Register **EOTStat0** to **EOTStat2**, **EOTConfig0** and **EOTConfig1**

These registers are located in the standby block and are supplied by the standby supply. They are not reset with the power on reset of the digital block.

Registers affected by the Lock Bit

Table 50 Overview of Register affected by the Lock Bit

Register	Offset
OutConfig0	040_H
OutConfig1	041_H
OutConfig2	042_H
OutConfig3	043_H
OutConfig4	044_H
OutConfig5	045_H
BriConfig0	046_H
BriConfig1	047_H
IGNConfig	048_H
VRSCConfig1	04A_H
VRSCConfig2	04B_H
OpConfig0	04E_H
ComConfig0	04F_H
ComConfig1	050_H
EOTConfig0	051_H
EOTConfig1	052_H

Table 50 Overview of Register affected by the Lock Bit (cont'd)

Register	Offset
InConfig0	053 _H
InConfig1	054 _H
InConfig2	055 _H
InConfig3	056 _H
DDConfig0	057 _H
DDConfig1	058 _H
DDConfig2	059 _H
DDConfig3	05A _H
WDConfig1	064 _H

14.1 Register Table

Table 14-1 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
Cmd0		001 _H	00 _H
MSCReadWd0		003 _H	00 _H
MSCReadDiag0EOT		004 _H	00 _H
MSCReadDiag1		005 _H	00 _H
MSCReadCont		006 _H	00 _H
MSCReadConfig0		007 _H	00 _H
MSCReadConfig1		008 _H	00 _H
MSCReadConfig2		009 _H	00 _H
MSCReadOEConfig		00A _H	00 _H
MSCReadMain		00B _H	00 _H
MSCReadWd1		00C _H	00 _H
WWDServiceCmd		015 _H	00 _H
FWDRespCmd		016 _H	00 _H
FWDRespSyncCmd		017 _H	00 _H
WDHBTPSyncCmd		018 _H	00 _H
CmdSR		01A _H	00 _H
CmdOE		01C _H	00 _H
CmdLOCK		01E _H	00 _H
Diag0		020 _H	00 _H
Diag1		021 _H	00 _H
VRSDiag0		022 _H	00 _H
VRSDiag1		023 _H	00 _H
ComDiag		024 _H	00 _H
OutDiag0		025 _H	00 _H
OutDiag1		026 _H	00 _H
OutDiag2		027 _H	00 _H
OutDiag3		028 _H	00 _H
OutDiag4		029 _H	00 _H
PPOVDiag		02A _H	00 _H
BriDiag0		02B _H	00 _H
BriDiag1		02C _H	00 _H
IgnDiag		02D _H	00 _H
WdDiag		02E _H	00 _H
EOTStat0		031 _H	00 _H
EOTStat1		032 _H	00 _H

Table 14-1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
EOTStat2		033 _H	00 _H
OpStat0		034 _H	00 _H
OpStat1		035 _H	00 _H
WWDStat		036 _H	30 _H
FWDDStat0		037 _H	30 _H
FWDDStat1		038 _H	30 _H
TECStat		039 _H	30 _H
WdStat0		03A _H	00 _H
WdStat1		03B _H	00 _H
WDHBT0		03C _H	00 _H
WDHBT1		03D _H	00 _H
OutConfig0		040 _H	FF _H
OutConfig1		041 _H	3F _H
OutConfig2		042 _H	3F _H
OutConfig3		043 _H	30 _H
OutConfig4		044 _H	3F _H
OutConfig5		045 _H	3F _H
BriConfig0		046 _H	00 _H
BriConfig1		047 _H	00 _H
IGNConfig		048 _H	00 _H
VRSCConfig0		049 _H	00 _H
VRSCConfig1		04A _H	00 _H
VRSCConfig2		04B _H	00 _H
OpConfig0		04E _H	09 _H
ComConfig0		04F _H	A4 _H
ComConfig1		050 _H	0D _H
EOTConfig0		051 _H	00 _H
EOTConfig1		052 _H	00 _H
InConfig0		053 _H	00 _H
InConfig1		054 _H	00 _H
InConfig2		055 _H	00 _H
InConfig3		056 _H	00 _H
DDConfig0		057 _H	00 _H
DDConfig1		058 _H	00 _H
DDConfig2		059 _H	00 _H
DDConfig3		05A _H	00 _H
OEConfig0		05B _H	00 _H
OEConfig1		05C _H	00 _H

Table 14-1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
OEConfig2		05D _H	00 _H
OEConfig3		05E _H	00 _H
WWDConfig0		05F _H	FF _H
WWDConfig1		060 _H	77 _H
FWDConfig		061 _H	F7 _H
TECConfig		062 _H	77 _H
WDConfig0		063 _H	47 _H
WDConfig1		064 _H	03 _H
Cont0		07B _H	00 _H
Cont1		07C _H	00 _H
Cont2		07D _H	00 _H
Cont3		07E _H	00 _H

The registers are addressed wordwise.

14.2 Command Register

Cmd0 Offset Reset Value
001_H 00_H

7	6	5	4	3	2	1	0
WKCLR	RDOT	EOTS	MSCUPS	WDHBTS	VDIAGS	MRON	MRSE
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
WKCLR	7	w	Wake Up Signal Clear Command: 0 _B no action 1 _B initiated clear of internal wake signals Reset: 0 _B

Field	Bits	Type	Description
RDOT	6	w	Restart Delayed off Timer Command: 0_B no action 1_B delayed off timer is restarted Reset: 0_B
EOTS	5	w	Engine Off Timer Start Command: 0_B no action 1_B start counter Reset: 0_B
MSCUPS	4	w	MSC Upstream Stop Bit Command: 0_B no influence to upstream transmission 1_B upstream communication is stopped Reset: 0_B
WDHBT5	3	w	Watchdog Heartbeat Timer Sample Command: 0_B no action 1_B Watchdog Heartbeat Timer sampled (WDHBT0 and WDHBT1) Reset: 0_B
VDIAGS	2	w	VRS Diagnosis Measurement Start Command: 0_B no measurement 1_B start of VRS diagnosis measurement Reset: 0_B
MRON	1	w	Main Relay On Command (active if MRSE=1): 0_B initiated main relay is switched off 1_B initiated main relay is switched on Reset: 0_B
MRSE	0	w	Main Relay Switching Enable: 0_B main relay switching by bit MRON not enabled 1_B main relay switching enabled: value of MRON executed Reset: 0_B

MSCReadWd0

Offset

Reset Value

003_H

00_H

7	6	5	4	3	2	1	0
WWDCONF IG0	WDCONFI G0	WWDSTAT	WDDIAG	FWDSTAT 1	FWDSTAT 0	TECSTAT	WDSTAT0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
WWDCONFIG0	7	w	Read Status Register WWDConfig0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
WDCONFIG0	6	w	Read Status Register WDConfig0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
WWDSTAT	5	w	Read Status Register WWDStat 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
WDDIAG	4	w	Read Configuration Register WdDiag 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
FWDSTAT1	3	w	Read Configuration Register FWDStat1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
FWDSTAT0	2	w	Read Diagnosis Register FWDStat0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
TECSTAT	1	w	Read Diagnosis Register TECStat 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
WDSTAT0	0	w	Read Status Register WdStat0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B

MSCReadDiag0EOT

Offset

004_H

Reset Value

00_H

7	6	5	4	3	2	1	0
PPOVDIAG	DIAG1	EOTSTAT 2	EOTSTAT 1	EOTSTAT 0	COMDIAG	VRSDIAG 1	VRSDIAG 0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PPOVDIAG	7	w	Read Diagnosis Register PPOVDIag 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
DIAG1	6	w	Read Diagnosis Register Diag1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
EOTSTAT2	5	w	Read Status Register EOTStat2 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
EOTSTAT1	4	w	Read Status Register EOTStat1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
EOTSTAT0	3	w	Read Status Register EOTStat0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
COMDIAG	2	w	Read Diagnosis Register ComDiag 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
VRSDIAG1	1	w	Read Diagnosis Register VRSDIag1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
VRSDIAG0	0	w	Read Diagnosis Register VRSDIag0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B

MSCReadDiag1

Offset

Reset Value

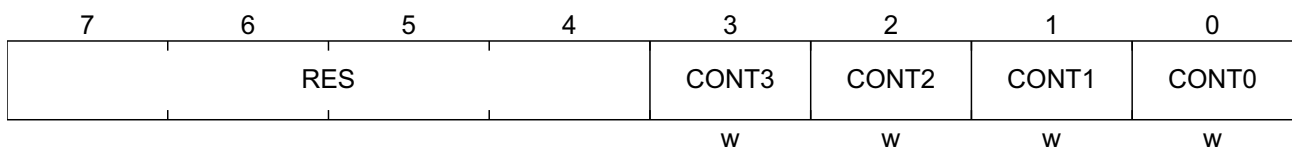
005_H

00_H

7	6	5	4	3	2	1	0
IGNDIAG	BRIDIAG 1	BRIDIAG 0	OUTDIAG 4	OUTDIAG 3	OUTDIAG 2	OUTDIAG 1	OUTDIAG 0
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
IGNDIAG	7	w	Read Diagnosis Register IgnDiag 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
BRIDIAG1	6	w	Read Diagnosis Register BriDiag1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
BRIDIAG0	5	w	Read Diagnosis Register BriDiag0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OUTDIAG4	4	w	Read Diagnosis Register OutDiag4 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OUTDIAG3	3	w	Read Diagnosis Register OutDiag3 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OUTDIAG2	2	w	Read Diagnosis Register OutDiag2 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OUTDIAG1	1	w	Read Diagnosis Register OutDiag1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OUTDIAG0	0	w	Read Diagnosis Register OutDiag0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B

MSCReadCont **Offset** **Reset Value**
006_H **00_H**

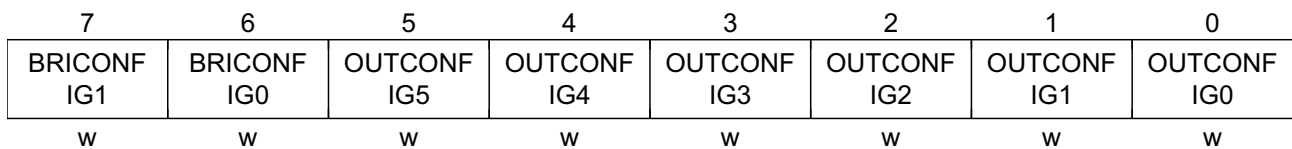


Field	Bits	Type	Description
CONT3	3	w	Read Control Register Cont3 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
CONT2	2	w	Read Control Register Cont2 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
CONT1	1	w	Read Control Register Cont1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
CONT0	0	w	Read Control Register Cont0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B

MSCReadConfig0

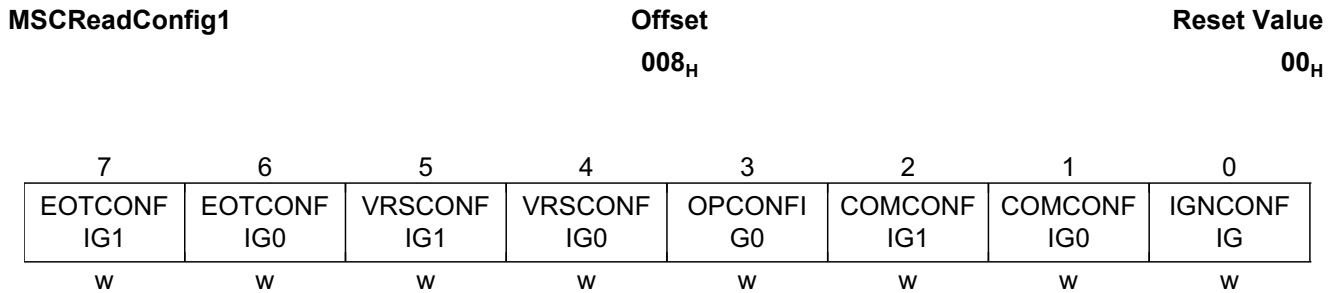
Offset
007_H

Reset Value
00_H



Field	Bits	Type	Description
BRICONFIG1	7	w	Read Configuration Register BriConfig1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
BRICONFIG0	6	w	Read Configuration Register BriConfig0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OUTCONFIG5	5	w	Read Configuration Register OutConfig5 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B

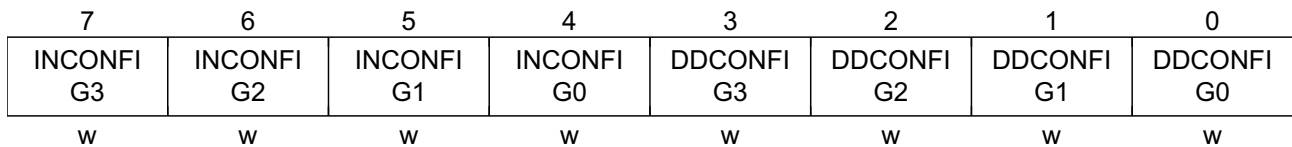
Field	Bits	Type	Description
OUTCONFIG4	4	w	Read Configuration Register OutConfig4 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OUTCONFIG3	3	w	Read Configuration Register OutConfig3 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OUTCONFIG2	2	w	Read Configuration Register OutConfig2 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OUTCONFIG1	1	w	Read Configuration Register OutConfig1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OUTCONFIG0	0	w	Read Configuration Register OutConfig0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B



Field	Bits	Type	Description
EOTCONFIG1	7	w	Read Configuration Register EOTConfig1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
EOTCONFIG0	6	w	Read Configuration Register EOTConfig0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B

Field	Bits	Type	Description
VRSCONFIG1	5	w	Read Configuration Register VRSConfig1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
VRSCONFIG0	4	w	Read Configuration Register VRSConfig0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OPCONFIG0	3	w	Read Configuration Register OpConfig0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
COMCONFIG 1	2	w	Read Configuration Register ComConfig1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
COMCONFIG 0	1	w	Read Configuration Register ComConfig0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
IGNCONFIG	0	w	Read Configuration Register IGNConfig 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B

MSCReadConfig2 **Offset** **Reset Value**
009_H **00_H**



Field	Bits	Type	Description
INCONFIG3	7	w	Read Configuration Register InConfig3 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B

Field	Bits	Type	Description
VRSCONFIG2	4	w	Read Configuration Register VRSConfig2 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OECONFIG3	3	w	Read Configuration Register OEConfig3 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OECONFIG2	2	w	Read Configuration Register OEConfig2 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OECONFIG1	1	w	Read Configuration Register OEConfig1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
OECONFIG0	0	w	Read Configuration Register OEConfig0 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B

MSCReadMain

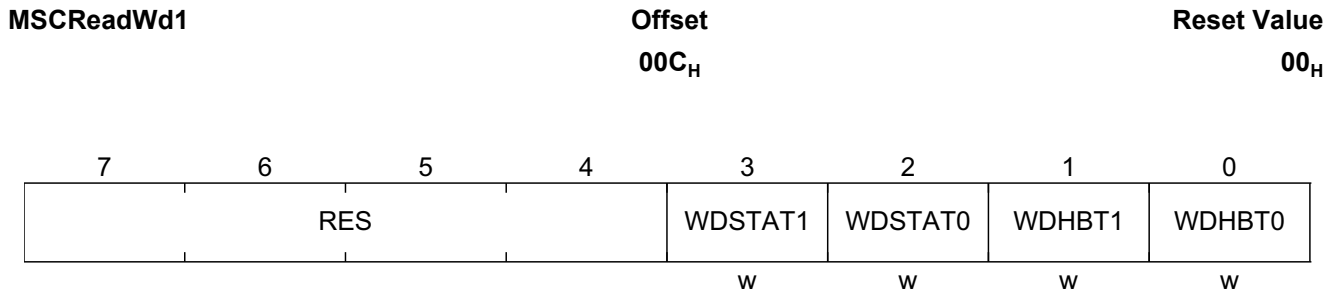
Offset
00B_H

Reset Value
00_H

7	6	5	4	3	2	1	0
RES	WWDCONFIG1	TECCONFIG	FWDCONFIG	WDCONFIGN1	OPSTAT1	OPSTAT0	DIAG0
	w	w	w	w	w	w	w

Field	Bits	Type	Description
WWDCONFIG1	6	w	Read Status Register WWDConfig1 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B
TECCONFIG	5	w	Read Status Register TECConfig 0 _B no action 1 _B multi read operation executed (order MSB to LSB) Reset: 0 _B

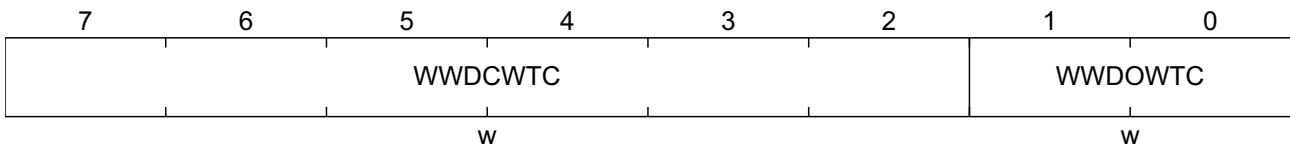
Field	Bits	Type	Description
FWDCONFIG	4	w	Read Status Register FWDConfig 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
WDCONFIG1	3	w	Read Status Register WDConfig1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OPSTAT1	2	w	Read Status Register OpStat1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
OPSTAT0	1	w	Read Status Register OpStat0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
DIAG0	0	w	Read Diagnosis Register Diag0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B



Field	Bits	Type	Description
WDSTAT1	3	w	Read Status Register WdStat1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
WDSTAT0	2	w	Read Status Register WdStat0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B

Field	Bits	Type	Description
WDHBT1	1	w	Read Status Register WDHBT1 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B
WDHBT0	0	w	Read Status Register WDHBT0 0_B no action 1_B multi read operation executed (order MSB to LSB) Reset: 0_B

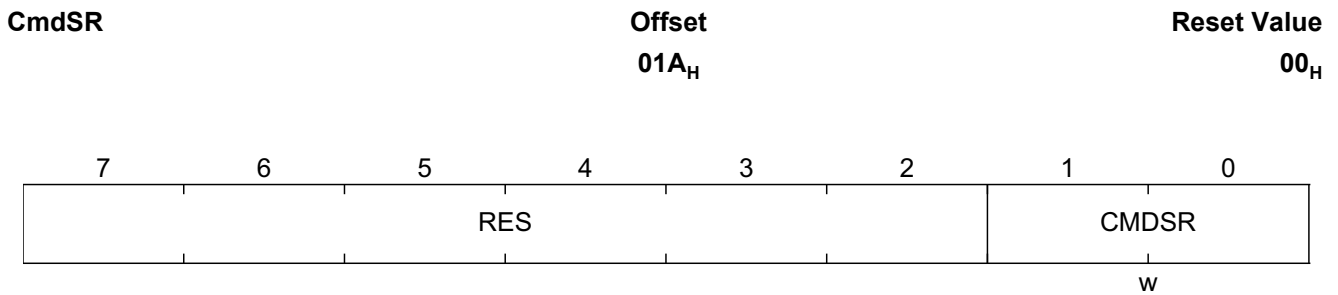
WWDServiceCmd **Offset** **Reset Value**
015_H **00_H**



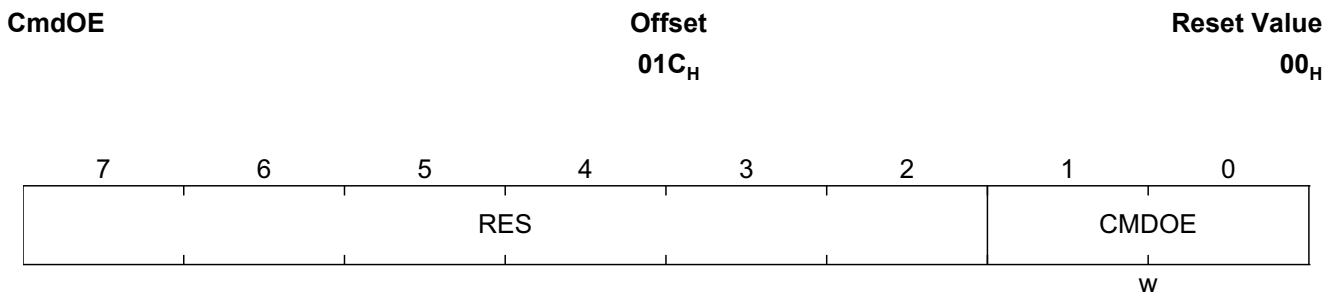
Field	Bits	Type	Description
WWDCWTC	7:2	w	Window Watchdog Closed Window Time Write Command: Set WWDCWT in register WWDCConfig0 000000_B no change - old setting used for open and closed window 000001_B 1,6ms 111111_B 100,8ms Reset: 000000_B
WWDOWTC	1:0	w	Window Watchdog Open Window Time Write Command: Set WWDOWT in register WWDCConfig0 00_B 3,2ms 01_B 6,4ms 10_B 9,6ms 11_B 12,8ms Reset: 00_B

FWDRspCmd **Offset** **Reset Value**
016_H **00_H**

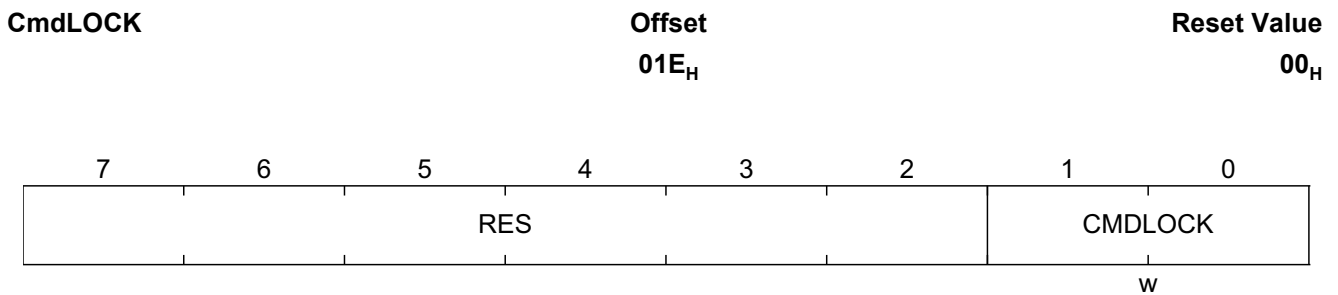
Field	Bits	Type	Description
WDHBTPC	6:0	w	Heartbeat Timer Period Write and Synchronisation Command: Set WDHBTP in register WDConfig0 0000000 _B no change 0000001 _B 1,6ms 0000010 _B 3,2ms 1111111 _B 203,2ms Reset: 0000000 _B



Field	Bits	Type	Description
CMDSR	1:0	w	Software Reset Command 00 _B No action 01 _B No action 10 _B No action 11 _B Initiate software reset Reset: 00 _B

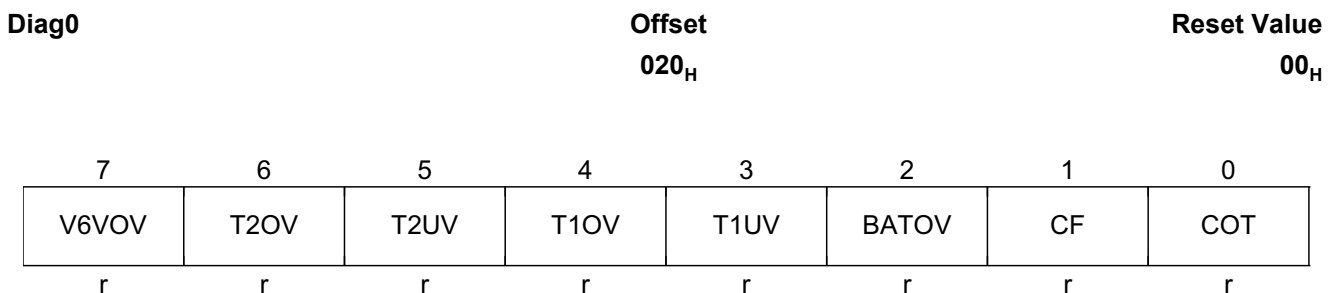


Field	Bits	Type	Description
CMDOE	1:0	w	Global Output Enable Command 00 _B No action 01 _B Set Bit OE to 0 10 _B Set Bit OE to 1 11 _B No action Reset: 00 _B

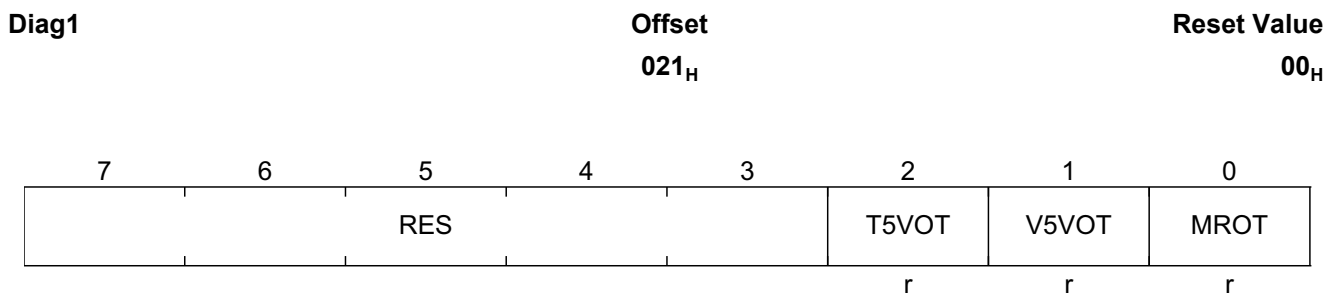


Field	Bits	Type	Description
CMDLOCK	1:0	w	Configuration Lock Command 00 _B No action 01 _B Set Bit LOCK to 0 10 _B Set Bit LOCK to 1 11 _B No action Reset: 00 _B

14.3 Diagnosis Register

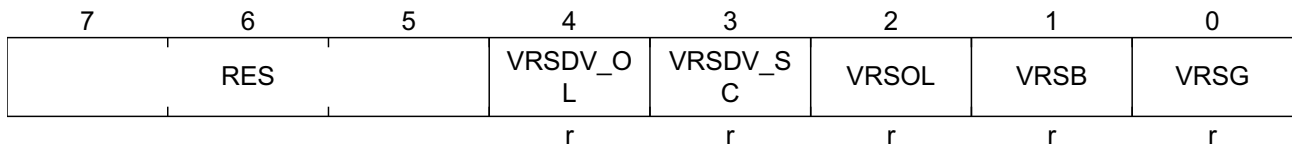


Field	Bits	Type	Description
V6VOV	7	r	Over Voltage Diagnosis Bit of 6V Supply V6V: 0_B no over voltage 1_B over voltage Reset: 0_B
T2OV	6	r	Over Voltage Diagnosis Bit of Tracker Output T5V2: 0_B no over voltage 1_B over voltage Reset: 0_B
T2UV	5	r	Under Voltage Diagnosis Bit of Tracker Output T5V2: 0_B no under voltage 1_B under voltage Reset: 0_B
T1OV	4	r	Over Voltage Diagnosis Bit of Tracker Output T5V1: 0_B no over voltage 1_B over voltage Reset: 0_B
T1UV	3	r	Under Voltage Diagnosis Bit of Tracker Output T5V1: 0_B no under voltage 1_B under voltage Reset: 0_B
BATOV	2	r	Battery Over Voltage Diagnosis Bit: 0_B no battery over voltage 1_B battery over voltage Reset: 0_B
CF	1	r	Central Failure Diagnosis Bit: 0_B no failure 1_B failure of minimum one diagnostic detected Reset: 0_B
COT	0	r	Central Over Temperature Diagnosis Bit: 0_B no over temperature 1_B over temperature of minimum one temperature sensor Reset: 0_B



Field	Bits	Type	Description
T5VOT	2	r	Tracker Overtemperature Diagnosis Bit: 0_B no over temperature 1_B over temperature Reset: 0_B
V5VOT	1	r	V5V Regulator Overtemperature Diagnosis Bit: 0_B no over temperature 1_B over temperature Reset: 0_B
MROT	0	r	Main Relay Overtemperature Diagnosis Bit: 0_B no over temperature 1_B over temperature Reset: 0_B

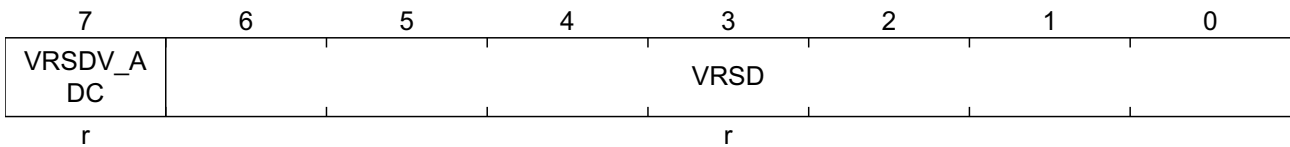
VRSDiag0 **Offset** **Reset Value**
022_H **00_H**



Field	Bits	Type	Description
VRSDV_OL	4	r	Open Load Measurement Data Valid Bit 0_B measurement data not valid 1_B measurement data valid Reset: 0_B
VRSDV_SC	3	r	Short to GND/Bat Measurement Data Valid Bit 0_B measurement data not valid 1_B measurement data valid Reset: 0_B
VRSOL	2	r	VRS Open Load Diagnosis Bit: 0_B no open load 1_B open load Reset: 0_B
VRSB	1	r	VRS Short to Battery Diagnosis Bit: 0_B no short to battery 1_B short to battery Reset: 0_B

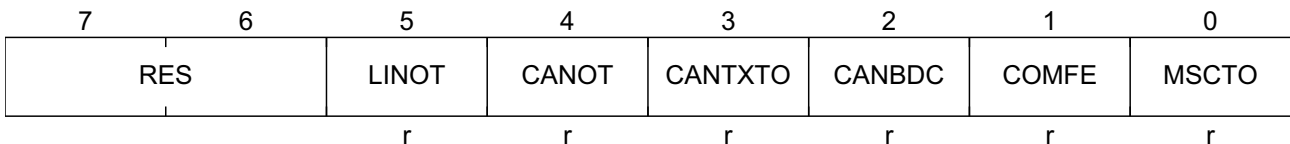
Field	Bits	Type	Description
VRSG	0	r	VRS Short to GND Diagnosis Bit: 0_B no short to GND 1_B short to GND Reset: 0_B

VRSDiag1 **Offset** **Reset Value**
023_H **00_H**



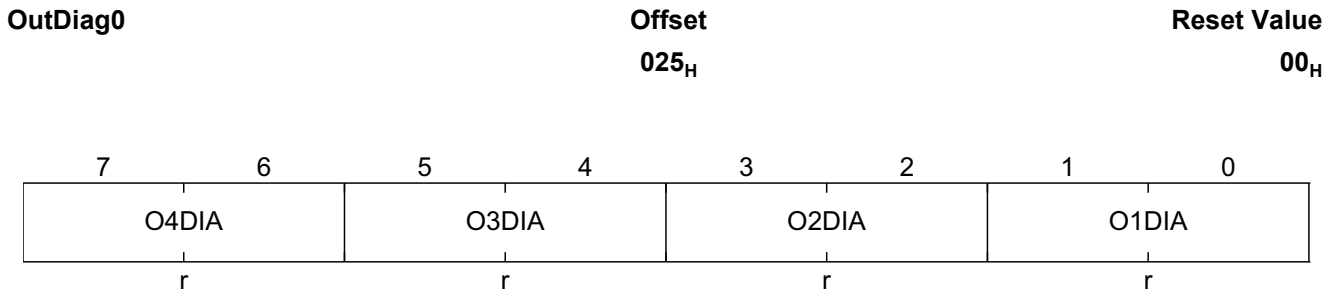
Field	Bits	Type	Description
VRSDV_ADC	7	r	ADC Measurement Data Valid Bit 0_B measurement data not valid 1_B measurement data valid Reset: 0_B
VRSD	6:0	r	VRS Diagnosis Measurement Result Register Reset: 000000 $_B$

ComDiag **Offset** **Reset Value**
024_H **00_H**



Field	Bits	Type	Description
LINOT	5	r	LIN Over Temperature Diagnosis Bit: 0_B no over temperature 1_B over temperature Reset: 0_B

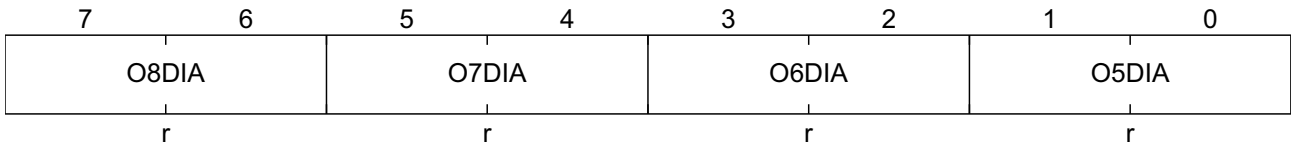
Field	Bits	Type	Description
CANOT	4	r	CAN Over Temperature Diagnosis Bit: 0_B no over temperature 1_B over temperature Reset: 0_B
CANTXTO	3	r	CAN TX Dominant Time Out Error Diagnosis Bit: 0_B no error 1_B TX dominant time out error Reset: 0_B
CANBDC	2	r	CAN Bus Line Dominant Clamp Error Diagnosis Bit: 0_B no error 1_B bus dominant clamp error Reset: 0_B
COMFE	1	r	Communication Frame Error Diagnosis Bit: 0_B no MSC/SPI frame error 1_B MSC/SPI frame error Reset: 0_B
MSCTO	0	r	MSC Time Out Failure Diagnosis Bit: 0_B no failure 1_B MSC time out Reset: 0_B



Field	Bits	Type	Description
O4DIA	7:6	r	Output4 Diagnosis Bits: see below Reset: 00_B
O3DIA	5:4	r	Output3 Diagnosis Bits: see below Reset: 00_B
O2DIA	3:2	r	Output2 Diagnosis Bits: see below Reset: 00_B

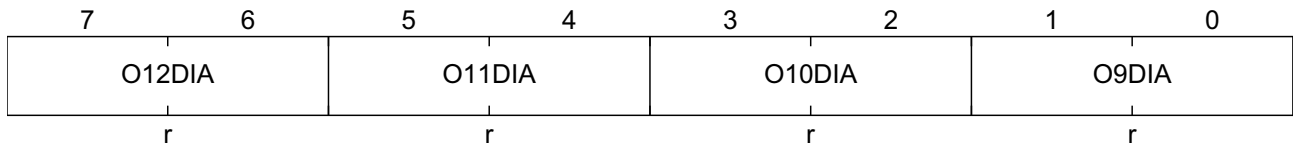
Field	Bits	Type	Description
O1DIA	1:0	r	Output1 Diagnosis Bits: 00 _B no failure 01 _B short circuit to bat (over current) or over temperature 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B

OutDiag1 **Offset** **Reset Value**
026_H **00_H**



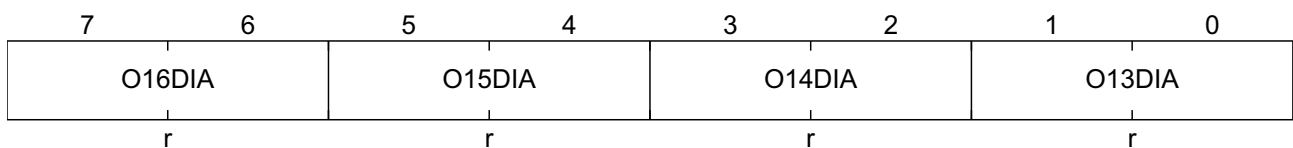
Field	Bits	Type	Description
O8DIA	7:6	r	Output8 (DFB8) Diagnosis Bit: 00 _B no failure 01 _B short circuit to bat 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B
O7DIA	5:4	r	Output7 Diagnosis Bits: see below Reset: 00 _B
O6DIA	3:2	r	Output6 Diagnosis Bits: see below Reset: 00 _B
O5DIA	1:0	r	Output5 Diagnosis Bits: 00 _B no failure 01 _B short circuit to bat (over current) or over temperature 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B

OutDiag2 **Offset** **Reset Value**
027_H **00_H**



Field	Bits	Type	Description
O12DIA	7:6	r	Output12 (DFB12) Diagnosis Bit: see below Reset: 00 _B
O11DIA	5:4	r	Output11 (DFB11) Diagnosis Bit: see below Reset: 00 _B
O10DIA	3:2	r	Output10 (DFB10) Diagnosis Bit: see below Reset: 00 _B
O9DIA	1:0	r	Output9 (DFB9) Diagnosis Bit: 00 _B no failure 01 _B short circuit to bat 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B

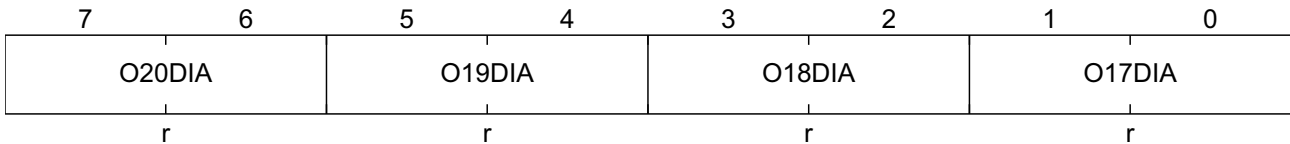
OutDiag3 **Offset** **Reset Value**
028_H **00_H**



Field	Bits	Type	Description
O16DIA	7:6	r	Output16 Diagnosis Bit: see below Reset: 00 _B
O15DIA	5:4	r	Output15 Diagnosis Bit: see below Reset: 00 _B
O14DIA	3:2	r	Output14 Diagnosis Bit: 00 _B no failure 01 _B short circuit to bat (over current) or over temperature 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B

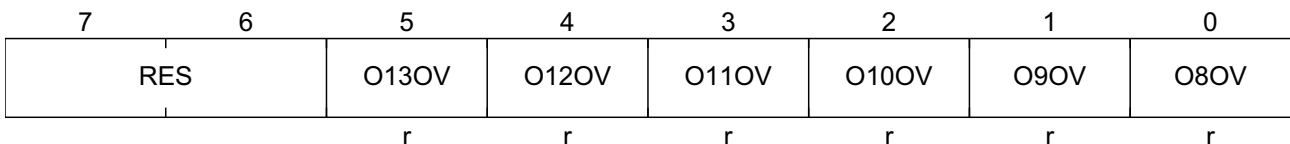
Field	Bits	Type	Description
O13DIA	1:0	r	Output13 (DFB13) Diagnosis Bit: 00 _B no failure 01 _B short circuit to bat 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B

OutDiag4 **Offset** **Reset Value**
029_H **00_H**

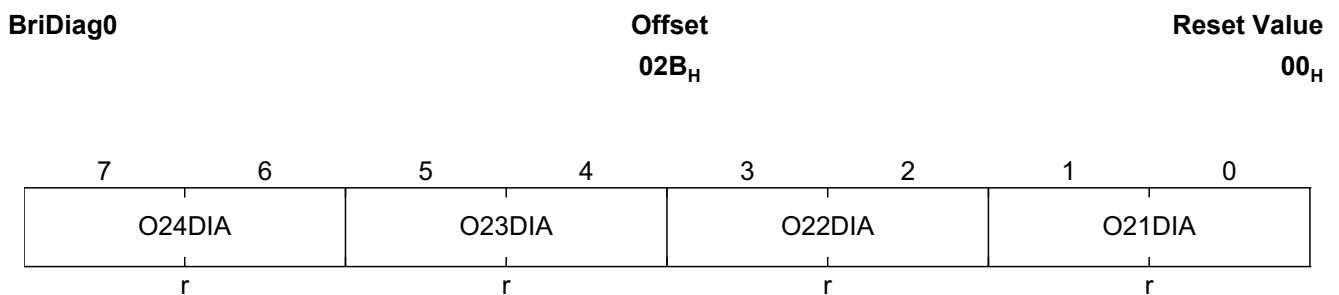


Field	Bits	Type	Description
O20DIA	7:6	r	Output20 Diagnosis Bits: see below Reset: 00 _B
O19DIA	5:4	r	Output19 Diagnosis Bits: see below Reset: 00 _B
O18DIA	3:2	r	Output18 Diagnosis Bits: see below Reset: 00 _B
O17DIA	1:0	r	Output17 Diagnosis Bits: 00 _B no failure 01 _B short circuit to bat (over current) or over temperature 10 _B open load in off 11 _B short circuit to ground in off Reset: 00 _B

PPOVDiag **Offset** **Reset Value**
02A_H **00_H**



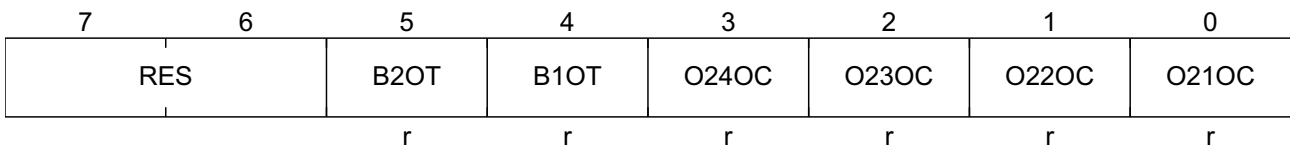
Field	Bits	Type	Description
O13OV	5	r	Output13 Overvoltage Diagnosis Bit: 0 _B no overvoltage 1 _B overvoltage Reset: 0 _B
O12OV	4	r	Output12 Overvoltage Diagnosis Bit: 0 _B no overvoltage 1 _B overvoltage Reset: 0 _B
O11OV	3	r	Output11 Overvoltage Diagnosis Bit: 0 _B no overvoltage 1 _B overvoltage Reset: 0 _B
O10OV	2	r	Output10 Overvoltage Diagnosis Bit: 0 _B no overvoltage 1 _B overvoltage Reset: 0 _B
O9OV	1	r	Output9 Overvoltage Diagnosis Bit: 0 _B no overvoltage 1 _B overvoltage Reset: 0 _B
O8OV	0	r	Output8 Overvoltage Diagnosis Bit: 0 _B no overvoltage 1 _B overvoltage Reset: 0 _B



Field	Bits	Type	Description
O24DIA	7:6	r	Output24 Diagnosis Bits (in off) Reset: 00 _B
O23DIA	5:4	r	Output23 Diagnosis Bits (in off) Reset: 00 _B

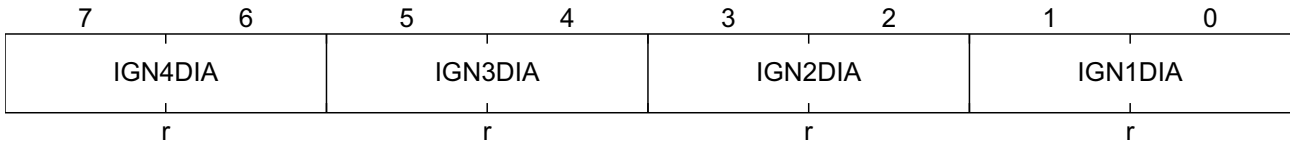
Field	Bits	Type	Description
O22DIA	3:2	r	Output22 Diagnosis Bits (in off) Reset: 00 _B
O21DIA	1:0	r	Output21 Diagnosis Bits (in off) Reset: 00 _B

BriDiag1 **Offset** **Reset Value**
02C_H **00_H**



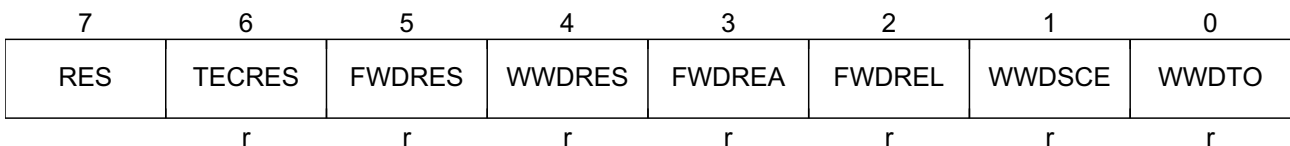
Field	Bits	Type	Description
B2OT	5	r	Output23,24 Overtemperature Diagnosis Bit 0 _B no over temperature 1 _B over temperature Reset: 0 _B
B1OT	4	r	Output21,22 Overtemperature Diagnosis Bit 0 _B no over temperature 1 _B over temperature Reset: 0 _B
O24OC	3	r	Output24 Over Current Diagnosis Bit 0 _B no over current 1 _B over current Reset: 0 _B
O23OC	2	r	Output23 Over Current Diagnosis Bit 0 _B no over current 1 _B over current Reset: 0 _B
O22OC	1	r	Output22 Over Current Diagnosis Bit 0 _B no over current 1 _B over current Reset: 0 _B
O21OC	0	r	Output21 Over Current Diagnosis Bit 0 _B no over current 1 _B over current Reset: 0 _B

IgnDiag **Offset** **Reset Value**
02D_H **00_H**



Field	Bits	Type	Description
IGN4DIA	7:6	r	Ignition 4 Output Diagnosis Bits: see below Reset: 00 _B
IGN3DIA	5:4	r	Ignition 3 Output Diagnosis Bits: see below Reset: 00 _B
IGN2DIA	3:2	r	Ignition 2 Output Diagnosis Bits: see below Reset: 00 _B
IGN1DIA	1:0	r	Ignition 1 Output Diagnosis Bits: 00 _B no failure 01 _B short circuit to bat or over temperature 10 _B open load 11 _B short circuit to ground in on Reset: 00 _B

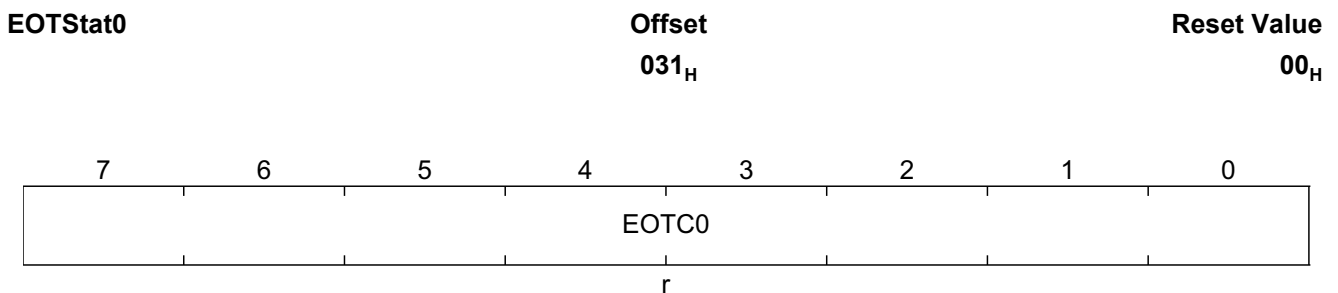
WdDiag **Offset** **Reset Value**
02E_H **00_H**



Field	Bits	Type	Description
TECRES	6	r	Reset caused by TEC: 0 _B no reset (caused by TEC) happened 1 _B reset (caused by TEC) happened Reset: 0 _B

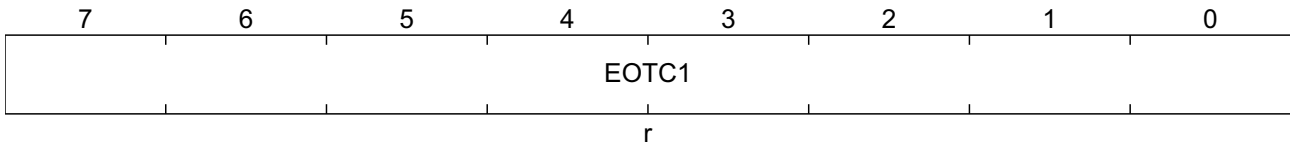
Field	Bits	Type	Description
FWDRES	5	r	Reset caused by Functional Watchdog: 0_B no functional watchdog reset happened 1_B functional watchdog reset happened Reset: 0_B
WWDRES	4	r	Reset caused by Window Watchdog: 0_B no window watchdog reset happened 1_B window watchdog reset happened Reset: 0_B
FWDREA	3	r	Functional Watchdog Response Error of Actual Running Sequence Diagnosis Bit: 0_B no error 1_B error Reset: 0_B
FWDREL	2	r	Functional Watchdog Response Error of Last Sequence Diagnosis Bit: 0_B no error 1_B error Reset: 0_B
WWDSC	1	r	Window Watchdog Service Command too Early Diagnosis Bit: 0_B service command in time 1_B service command too early Reset: 0_B
WWDTO	0	r	Window Watchdog Time Out Diagnosis Bit: 0_B no time out 1_B time out Reset: 0_B

14.4 Status Register



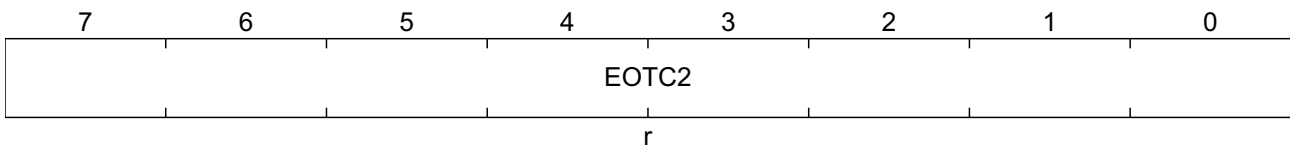
Field	Bits	Type	Description
EOTC0	7:0	r	Engine Off Timer Counter Value Bits: (Bit 7 - 0) Reset: 00 _H

EOTStat1 **Offset**
032_H **Reset Value**
00_H



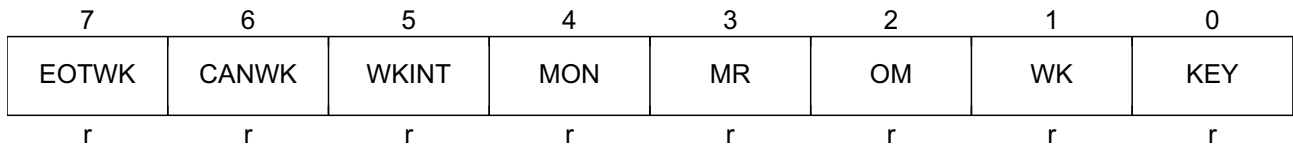
Field	Bits	Type	Description
EOTC1	7:0	r	Engine Off Timer Counter Value Bits: (Bit 15 - 8) Reset: 00 _H

EOTStat2 **Offset**
033_H **Reset Value**
00_H



Field	Bits	Type	Description
EOTC2	7:0	r	Engine Off Timer Counter Value Bits: (Bit 23 - 16) Reset: 00 _H

OpStat0 **Offset**
034_H **Reset Value**
00_H



Field	Bits	Type	Description
EOTWK	7	r	Status of internal EOTWK signal: 0 _B EOTWK is inactive 1 _B EOTWK is active Reset: 0 _B
CANWK	6	r	Status of internal CANWK signal: 0 _B CANWK is inactive 1 _B CANWK is active Reset: 0 _B
WKINT	5	r	Status of internal WKINT signal: 0 _B WKINT is inactive 1 _B WKINT is active Reset: 0 _B
MON	4	r	MON Pin Status Bit: 0 _B active (low) 1 _B inactive (high) Reset: 0 _B
MR	3	r	Main Relay Switch On Status Bit: 0 _B off 1 _B on Reset: 0 _B
OM	2	r	Operation Mode Bit: 0 _B normal operation 1 _B afterrun mode Reset: 0 _B
WK	1	r	WK Status Bit (filtered): 0 _B WK=0 1 _B WK=1 Reset: 0 _B
KEY	0	r	KEY Status Bit (filtered): 0 _B KEY=0 1 _B KEY=1 Reset: 0 _B

OpStat1	Offset	Reset Value
	035_H	00_H

7	6	5	4	3	2	1	0
LOCK	OE	EOTRES	RSTR	V5VOVR	V5VUVR	WDRES	ARES
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
LOCK	7	r	Configuration Lock Status Bit: 0_B Configuration registers unlocked 1_B Configuration registers locked Reset: 0_B
OE	6	r	Global Output Enable Status Bit: 0_B outputs disabled and control register are reset 1_B outputs enabled Reset: 0_B
EOTRES	5	r	Engine Off Timer Reset Status Bit: 0_B no EOT reset happened 1_B EOT reset happened Reset: 0_B
RSTR	4	r	Reset caused by external RST Reset: (only valid if no internal power on reset occurs) 0_B no external RST reset happened 1_B external RST reset happened Reset: 0_B
V5VOVR	3	r	Reset caused by V5V Over Voltage Reset: (only valid if no internal power on reset occurs) 0_B no V5V over voltage reset happened 1_B V5V over voltage reset happened Reset: 0_B
V5VUVR	2	r	Reset caused by V5V Under Voltage Reset: (only valid if no internal power on reset occurs) 0_B no V5V under voltage reset happened 1_B V5V under voltage reset happened Reset: 0_B
WDRES	1	r	Reset caused by Watchdog Reset: (only valid if no internal power on reset occurs) 0_B no watchdog reset happened 1_B watchdog reset happened Reset: 0_B
ARES	0	r	Reset caused by Afterrun Reset: (only valid if no internal power on reset occurs) 0_B no afterrun reset happened 1_B afterrun reset happened Reset: 0_B

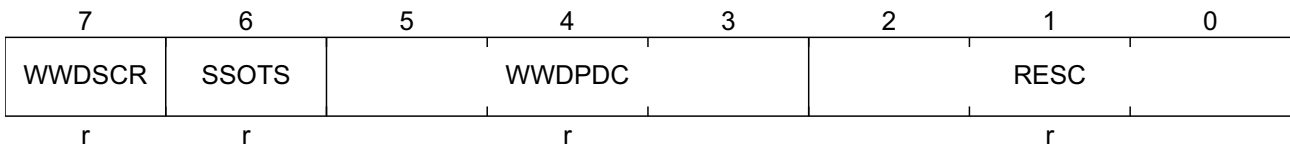
Field	Bits	Type	Description
FWDRESPC	5:4	r	Functional Watchdog Response Counter Value Reset: 11 _B
FWDQUEST	3:0	r	Functional Watchdog Question Reset: 0000 _B

TECStat **Offset** **Reset Value**
039_H 30_H



Field	Bits	Type	Description
TEC	5:0	r	Total Error Counter Value Reset: 110000 _B

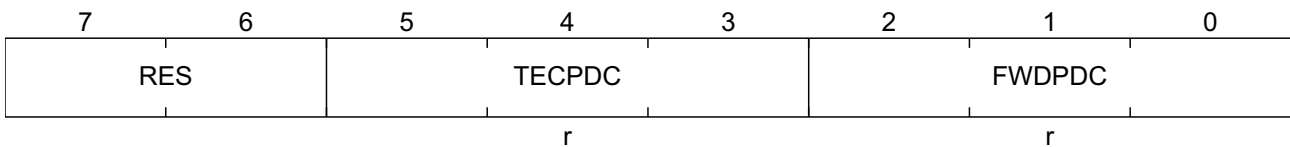
WdStat0 **Offset** **Reset Value**
03A_H 00_H



Field	Bits	Type	Description
WWDCR	7	r	Window Watchdog Service Command received 0 _B No Service Command received 1 _B Service Command received Reset: 0 _B

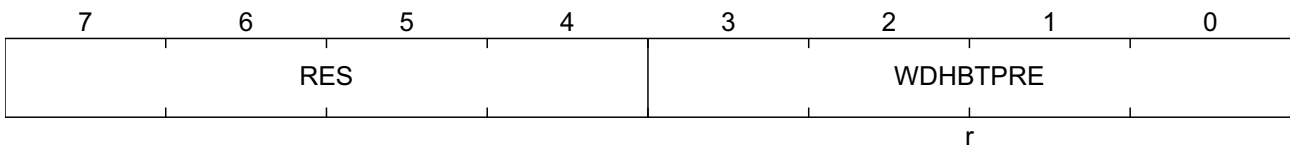
Field	Bits	Type	Description
SSOTS	6	r	Secure Shut Off Timer Start Status Bit: 0 _B timer reset 1 _B timer started Reset: 0 _B
WWDPDC	5:3	r	Window Watchdog Power Down Counter Value Reset: 000 _B
RESC	2:0	r	Reset Counter Value Reset: 000 _B

WdStat1 **Offset**
03B_H **Reset Value**
00_H



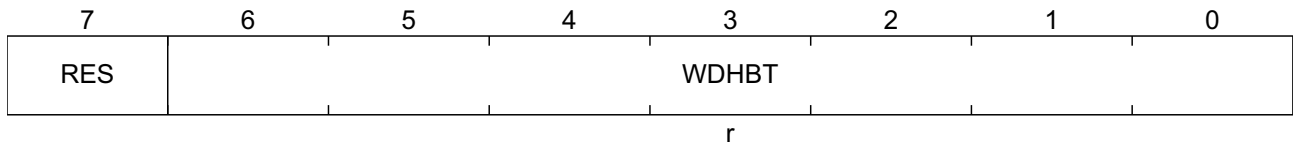
Field	Bits	Type	Description
TECPDC	5:3	r	Total Error Power Down Counter Value Reset: 000 _B
FWDPDC	2:0	r	Functional Watchdog Power Down Counter Value Reset: 000 _B

WDHBT0 **Offset**
03C_H **Reset Value**
00_H



Field	Bits	Type	Description
WDHBTPRE	3:0	r	Sampled Watchdog Heartbeat Timer Predivider Value Reset: 0000 _B

WDHBT1 **Offset** **Reset Value**
03D_H **00_H**

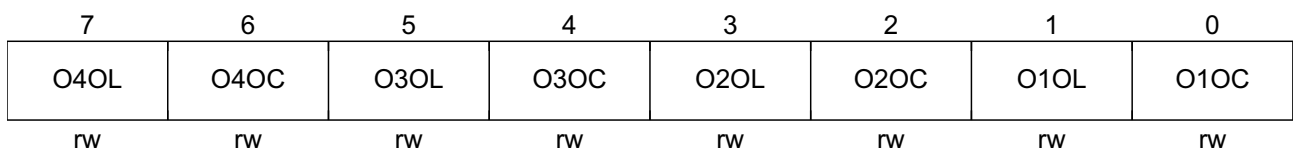


Field	Bits	Type	Description
WDHBT	6:0	r	Sampled Watchdog Heartbeat Timer Value Reset: 0000000 _B

14.5 Configuration Register

OutConfig0 locked with LOCK=1

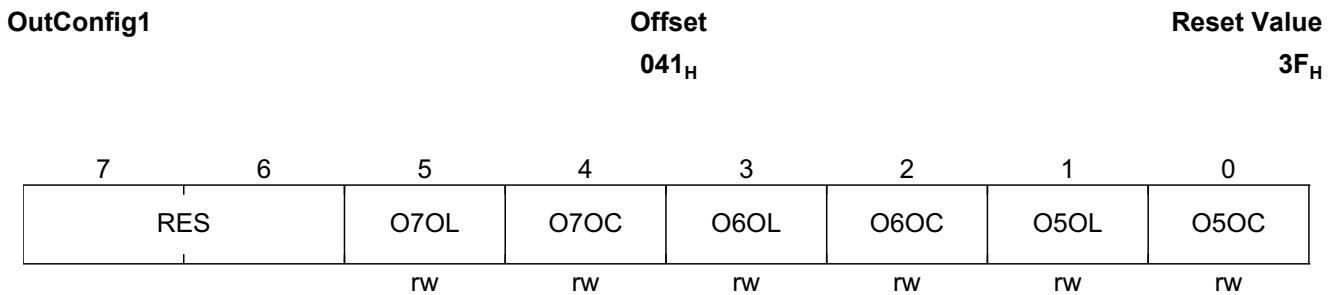
OutConfig0 **Offset** **Reset Value**
040_H **FF_H**



Field	Bits	Type	Description
O4OL	7	rw	Output4 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O4OC	6	rw	Output4 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
O3OL	5	rw	Output3 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B

Field	Bits	Type	Description
O3OC	4	rw	Output3 Over Current Protection Set Up: 0_B current limitation in case of over current 1_B switch off in case of over current Reset: 1_B
O2OL	3	rw	Output2 Open Load Set Up: 0_B pull down current deactivated 1_B fully functional Reset: 1_B
O2OC	2	rw	Output2 Over Current Protection Set Up: 0_B current limitation in case of over current 1_B switch off in case of over current Reset: 1_B
O1OL	1	rw	Output1 Open Load Set Up: 0_B pull down current deactivated 1_B fully functional Reset: 1_B
O1OC	0	rw	Output1 Over Current Protection Set Up: 0_B current limitation in case of over current 1_B switch off in case of over current Reset: 1_B

OutConfig1 locked with LOCK=1

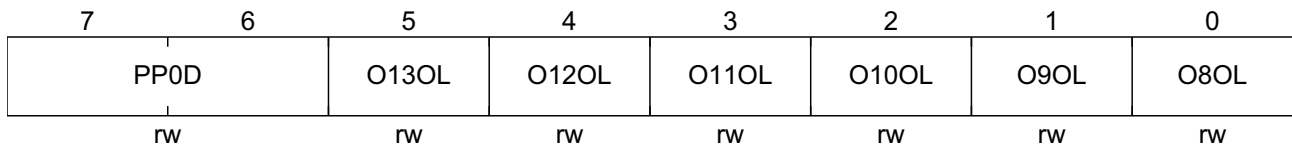


Field	Bits	Type	Description
O7OL	5	rw	Output7 Open Load Set Up: 0_B pull down current deactivated 1_B fully functional Reset: 1_B
O7OC	4	rw	Output7 Over Current Protection Set Up: 0_B current limitation in case of over current 1_B switch off in case of over current Reset: 1_B

Field	Bits	Type	Description
O6OL	3	rw	Output6 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O6OC	2	rw	Output6 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
O5OL	1	rw	Output5 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O5OC	0	rw	Output5 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B

OutConfig2 locked with LOCK=1

OutConfig2 **Offset** **Reset Value**
042_H **3F_H**

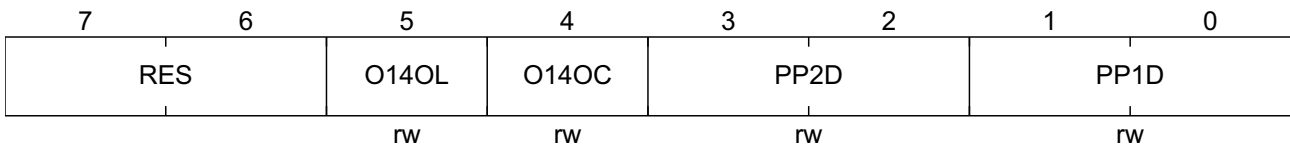


Field	Bits	Type	Description
PP0D	7:6	rw	Diagnosis in On Set Up for OUT8 and OUT9: 00 _B typ. 125mV short to bat in on threshold 01 _B typ. 225mV short to bat in on threshold 10 _B typ. 400mV short to bat in on threshold 11 _B typ. 0.8V short to bat in on threshold Reset: 00 _B
O13OL	5	rw	Output13 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O12OL	4	rw	Output12 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B

Field	Bits	Type	Description
O11OL	3	rw	Output11 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O10OL	2	rw	Output10 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O9OL	1	rw	Output9 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O8OL	0	rw	Output8 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B

OutConfig3 locked with LOCK=1

OutConfig3 **Offset** **Reset Value**
043_H **30_H**



Field	Bits	Type	Description
O14OL	5	rw	Output14 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O14OC	4	rw	Output14 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
PP2D	3:2	rw	Diagnosis in On Set Up for OUT12 and OUT13: 00 _B typ. 125mV short to bat in on threshold 01 _B typ. 225mV short to bat in on threshold 10 _B typ. 400mV short to bat in on threshold 11 _B typ. 0.8V short to bat in on threshold Reset: 00 _B

Field	Bits	Type	Description
PP1D	1:0	rw	Diagnosis in On Set Up for OUT10 and OUT11: 00 _B typ. 125mV short to bat in on threshold 01 _B typ. 225mV short to bat in on threshold 10 _B typ. 400mV short to bat in on threshold 11 _B typ. 0.8V short to bat in on threshold Reset: 00 _B

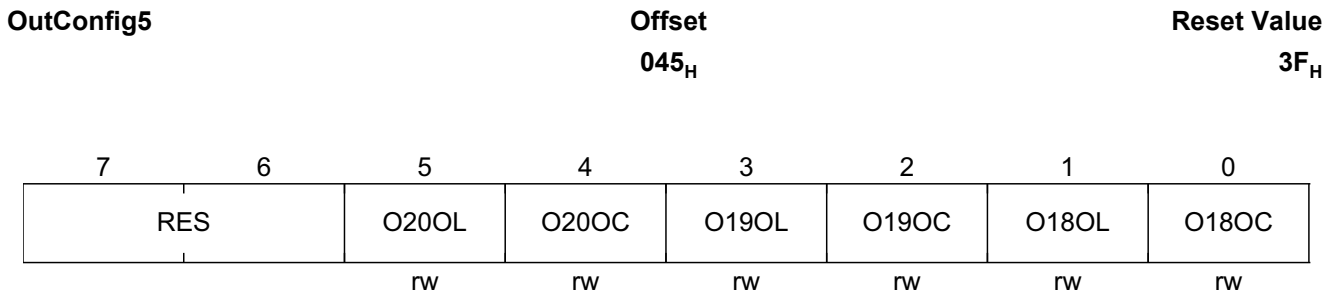
OutConfig4 locked with LOCK=1

OutConfig4								Offset	Reset Value
								044 _H	3F _H
7	6	5	4	3	2	1	0		
RES	O17D	O17OL	O17OC	O16OL	O16OC	O15OL	O15OC		
	rw	rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
O17D	6	rw	Output17 Delayed Off Set Up: 0 _B no delayed off function 1 _B delayed off function activated Reset: 0 _B
O17OL	5	rw	Output17 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O17OC	4	rw	Output17 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
O16OL	3	rw	Output16 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B
O16OC	2	rw	Output16 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
O15OL	1	rw	Output15 Open Load Set Up: 0 _B pull down current deactivated 1 _B fully functional Reset: 1 _B

Field	Bits	Type	Description
O15OC	0	rw	Output15 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B

OutConfig5 locked with LOCK=1



Field	Bits	Type	Description
O20OL	5	rw	Output20 Open Load Set Up: 0 _B pull down and pull up current deactivated 1 _B fully functional Reset: 1 _B
O20OC	4	rw	Output20 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
O19OL	3	rw	Output19 Open Load Set Up: 0 _B pull down and pull up current deactivated 1 _B fully functional Reset: 1 _B
O19OC	2	rw	Output19 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B
O18OL	1	rw	Output18 Open Load Set Up: 0 _B pull down and pull up current deactivated 1 _B fully functional Reset: 1 _B
O18OC	0	rw	Output18 Over Current Protection Set Up: 0 _B current limitation in case of over current 1 _B switch off in case of over current Reset: 1 _B

BriConfig0 locked with LOCK=1

BriConfig0

Offset
046_H

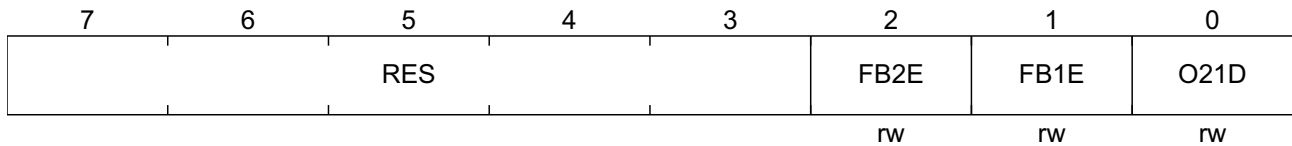
Reset Value
00_H

7	6	5	4	3	2	1	0
O24F	O24M	O23F	O23M	O22F	O22M	O21F	O21M
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
O24F	7	rw	Output24 Freewheeling Mode Set Up: 0 _B passive freewheeling mode 1 _B active freewheeling mode Reset: 0 _B
O24M	6	rw	Output24 Mode Set Up: 0 _B low side switch mode 1 _B high side switch mode Reset: 0 _B
O23F	5	rw	Output23 Freewheeling Mode Set Up: 0 _B passive freewheeling mode 1 _B active freewheeling mode Reset: 0 _B
O23M	4	rw	Output23 Mode Set Up: 0 _B low side switch mode 1 _B high side switch mode Reset: 0 _B
O22F	3	rw	Output22 Freewheeling Mode Set Up: 0 _B passive freewheeling mode 1 _B active freewheeling mode Reset: 0 _B
O22M	2	rw	Output22 Mode Set Up: 0 _B low side switch mode 1 _B high side switch mode Reset: 0 _B
O21F	1	rw	Output21 Freewheeling Mode Set Up: 0 _B passive freewheeling mode 1 _B active freewheeling mode Reset: 0 _B
O21M	0	rw	Output21 Mode Set Up: 0 _B low side switch mode 1 _B high side switch mode Reset: 0 _B

BriConfig1 locked with LOCK=1

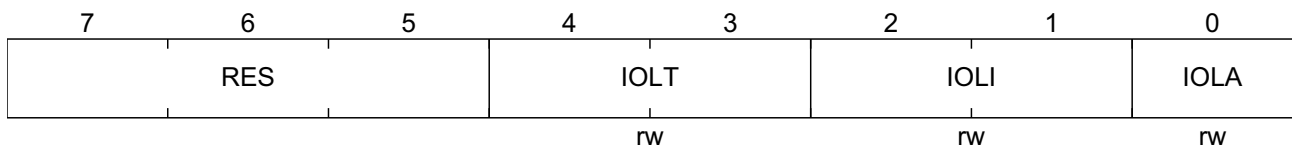
BriConfig1 **Offset** **Reset Value**
047_H **00_H**



Field	Bits	Type	Description
FB2E	2	rw	Full Bridge 2 Enable Bit: 0 _B Output 23 and 24 are not used in full bridge configuration 1 _B Output 23 and 24 are used in full bridge configuration Reset: 0 _B
FB1E	1	rw	Full Bridge 1 Enable Bit: 0 _B Output 21 and 22 are not used in full bridge configuration 1 _B Output 21 and 22 are used in full bridge configuration Reset: 0 _B
O21D	0	rw	Output21 Delayed Off Set Up: 0 _B no delayed off function 1 _B delayed off function activated Reset: 0 _B

IGNConfig locked with LOCK=1

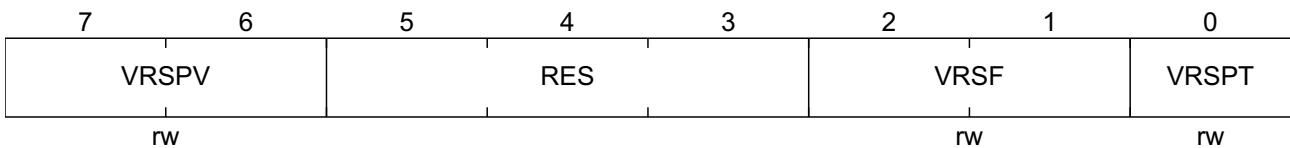
IGNConfig **Offset** **Reset Value**
048_H **00_H**



Field	Bits	Type	Description
IOLT	4:3	rw	Ignition Time Setting for Open Load Detection: 00 _B 64μs 01 _B 256μs 10 _B 512μs 11 _B 768μs Reset: 00 _B

Field	Bits	Type	Description
IOLI	2:1	rw	Ignition Current Setting for Open Load Detection: 00 _B -100μA 01 _B -400μA 10 _B -1 mA 11 _B -4 mA Reset: 00 _B
IOLA	0	rw	Ignition Open Load Detection Activation: 0 _B no open load detection 1 _B open load detection active Reset: 0 _B

VRSConfig0 **Offset** **Reset Value**
049_H **00_H**



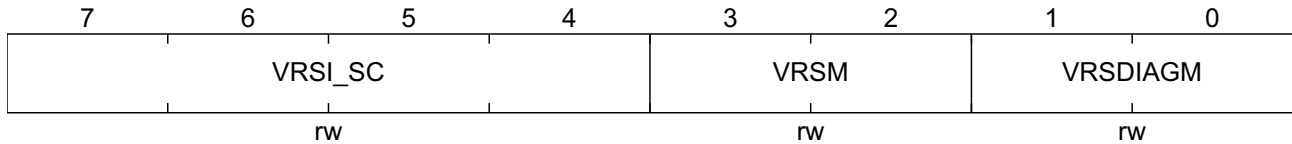
Field	Bits	Type	Description
VRSPV	7:6	rw	VRS Peak Voltage Detection Set Up: 00 _B 50mV 01 _B 150mV 10 _B 350mV 11 _B 550mV Reset: 00 _B
VRSF	2:1	rw	VRS Output Filter Time Set Up: 00 _B 1μs, reset value 01 _B 5μs 10 _B 10μs 11 _B 20μs Reset: 00 _B
VRSPT	0	rw	VRS Peak Time Set Up: 0 _B 10μs, reset value 1 _B 250μs Reset: 0 _B

VRSConfig1 locked with LOCK=1

VRSConfig1

Offset
04A_H

Reset Value
00_H



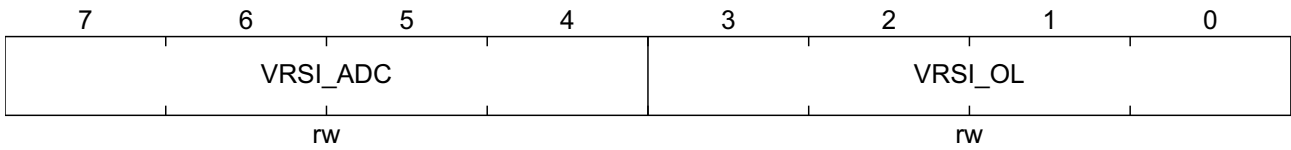
Field	Bits	Type	Description
VRSI_SC	7:4	rw	Current setting for short to GND/Bat measurement 0000 _B 10μA 0001 _B 20μA 0010 _B 30μA 0011 _B 40μA 0100 _B 50μA 0101 _B 60μA 0110 _B 70μA 0111 _B 80μA 1000 _B 100μA 1001 _B 120μA 1010 _B 140μA 1011 _B 160μA 1100 _B to full scale (0b1111) 160μA Reset: 0000 _B
VRSM	3:2	rw	VRS/Hall Sensor Mode Set Up: 00 _B auto detection mode for VR sensor signals (reset value) 01 _B semi auto detection mode for VR sensor signals 10 _B manuel detection mode for VR sensor signals 11 _B Hall sensor mode Reset: 00 _B
VRSDIAGM	1:0	rw	VRS Diagnosis Mode Set Up: 00 _B normal detection mode 01 _B short to GND/Bat diagnosis mode 10 _B open load diagnosis mode 11 _B ADC diagnosis mode Reset: 00 _B

VRSConfig2 locked with LOCK=1

VRSConfig2

Offset
04B_H

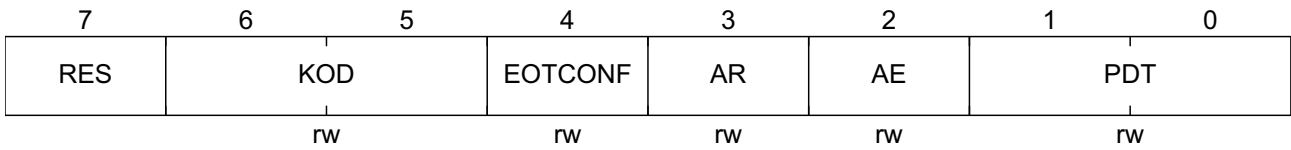
Reset Value
00_H



Field	Bits	Type	Description
VRSI_ADC	7:4	rw	Current setting for ADC measurement 0000 _B 10µA 0001 _B 20µA 0010 _B 30µA 0011 _B 40µA 0100 _B 50µA 0101 _B 60µA 0110 _B 70µA 0111 _B 80µA 1000 _B 100µA 1001 _B 120µA 1010 _B 140µA 1011 _B 160µA 1100 _B to full scale (0b1111) 160µA Reset: 0000 _B
VRSI_OL	3:0	rw	Current setting for open load measurement 0000 _B 10µA 0001 _B 20µA 0010 _B 30µA 0011 _B 40µA 0100 _B 50µA 0101 _B 60µA 0110 _B 70µA 0111 _B 80µA 1000 _B 100µA 1001 _B 120µA 1010 _B 140µA 1011 _B 160µA 1100 _B to full scale (0b1111) 160µA Reset: 0000 _B

OpConfig0 locked with LOCK=1

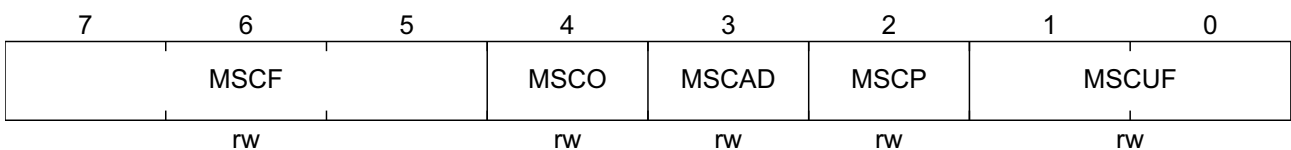
OpConfig0	Offset 04E _H	Reset Value 09 _H
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Field	Bits	Type	Description
KOD	6:5	rw	Key Off Delay Set Up: 00 _B 100ms 01 _B 200ms 10 _B 400ms 11 _B 800ms Reset: 00 _B
EOTCONF	4	rw	Engine Off Timer Configuration: 0 _B timer start with negative edge of KEY signal 1 _B timer start with command EOTS in register Cmd0 Reset: 0 _B
AR	3	rw	Afterrun Reset Behavior Set Up: 0 _B no afterrun reset 1 _B afterrun reset Reset: 1 _B
AE	2	rw	Afterrun Enable: 0 _B no afterrun mode 1 _B afterrun mode Reset: 0 _B
PDT	1:0	rw	Power Down Time Set Up: 00 _B 100ms 01 _B 200ms 10 _B 300ms 11 _B 400ms Reset: 01 _B

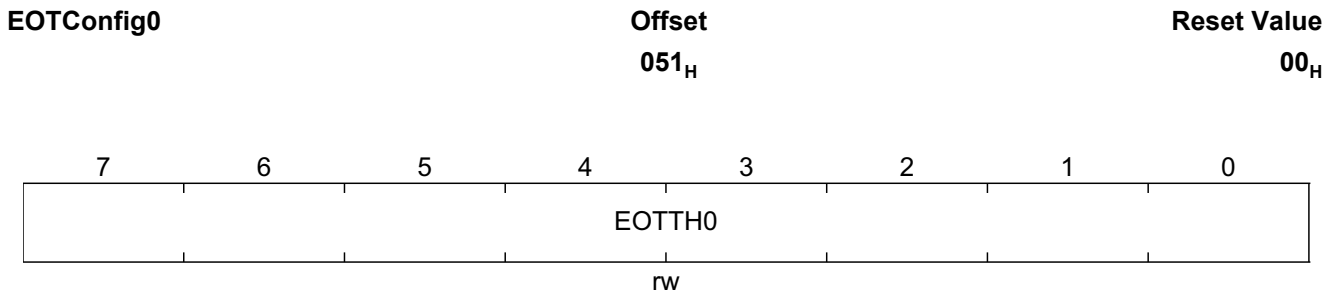
ComConfig0 locked with LOCK=1

ComConfig0 **Offset** **Reset Value**
04F_H **A4_H**



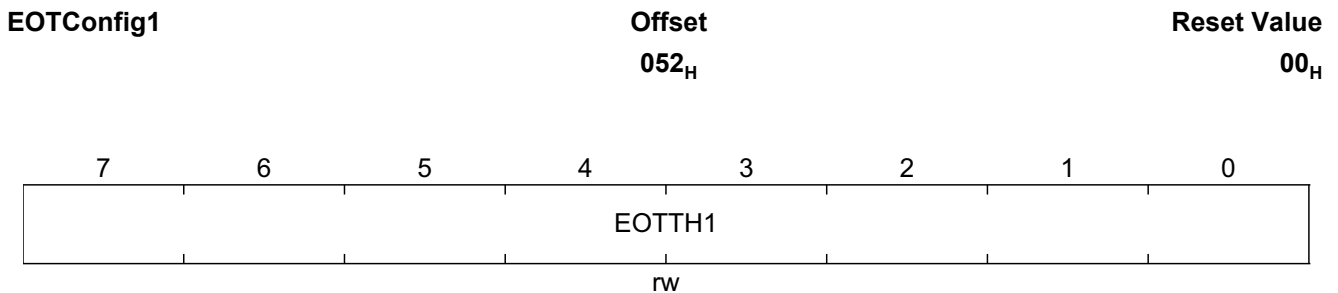
Field	Bits	Type	Description
LINTOE	3	rw	LIN TX Time OUT Function Enable: 0 _B TX time out function disabled 1 _B TX time out function enabled Reset: 1 _B
LIN	2:1	rw	Operation Mode: 00 _B receive only mode 01 _B LIN/K-line operation 10 _B flash mode 11 _B receive only mode Reset: 10 _B
CAN	0	rw	CAN Operation Mode: 0 _B receive only mode 1 _B high speed CAN mode Reset: 1 _B

EOTConfig0 locked with LOCK=1



Field	Bits	Type	Description
EOTTH0	7:0	rw	Engine Off Timer Comparator Threshold: (Bit 7 - 0) Reset: 00 _H

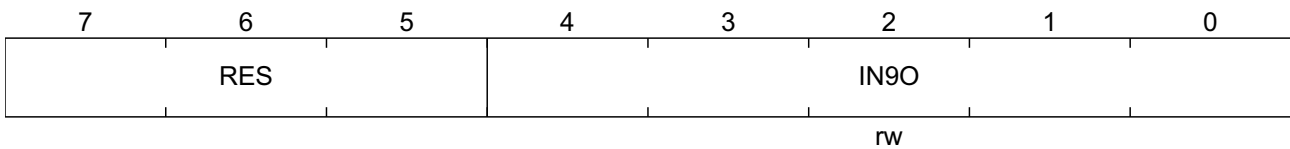
EOTConfig1 locked with LOCK=1



Field	Bits	Type	Description
EOTTH1	7:0	rw	Engine Off Timer Comparator Threshold: (Bit 15 - 8) Reset: 00 _H

InConfig0 locked with LOCK=1

InConfig0 **Offset**
053_H **Reset Value**
00_H



Field	Bits	Type	Description
IN90	4:0	rw	Direct control Input9 Assignment: See Table 14-2 Reset: 00000 _B

Additional Table with Constants

This table describes more than 16 constants.

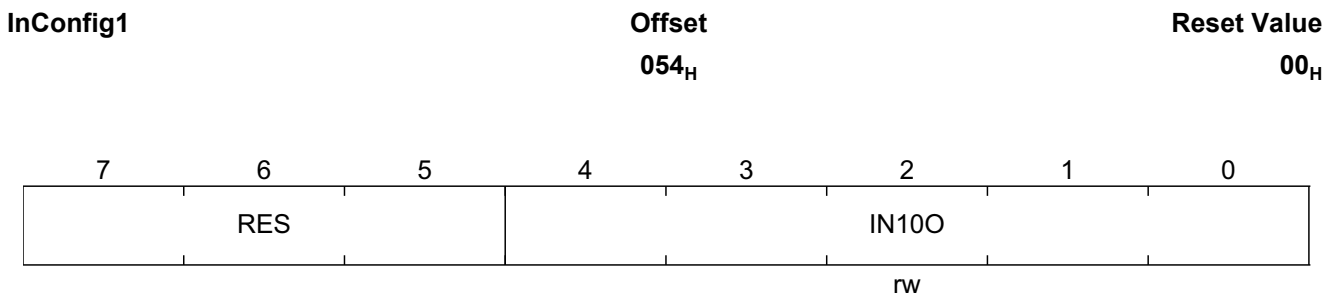
Table 14-2 Constant Values

Name and Description	Value
output5	00000 _B
output6	00001 _B
output7	00010 _B
output8	00011 _B
output9	00100 _B
output10	00101 _B
output11	00110 _B
output12	00111 _B

Table 14-2 Constant Values (cont'd)

Name and Description	Value
output13	01000 _B
output14	01001 _B
output15	01010 _B
output16	01011 _B
output17	01100 _B
output18	01101 _B
output19	01110 _B
output20	01111 _B
output21	10000 _B
output22	10001 _B
output23	10010 _B
output24	10011 _B

InConfig1 locked with LOCK=1



Field	Bits	Type	Description
IN100	4:0	rw	Direct control Input10 Assignment: See Table 14-3 Reset: 00000 _B

Additional Table with Constants

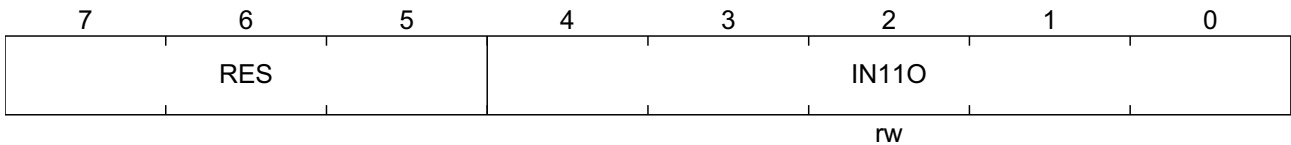
This table describes more than 16 constants.

Table 14-3 Constant Values

Name and Description	Value
output5	00000 _B
output6	00001 _B
output7	00010 _B
output8	00011 _B
output9	00100 _B
output10	00101 _B
output11	00110 _B
output12	00111 _B
output13	01000 _B
output14	01001 _B
output15	01010 _B
output16	01011 _B
output17	01100 _B
output18	01101 _B
output19	01110 _B
output20	01111 _B
output21	10000 _B
output22	10001 _B
output23	10010 _B
output24	10011 _B

InConfig2 locked with LOCK=1

InConfig2 **Offset** **Reset Value**
055_H **00_H**



Field	Bits	Type	Description
IN110	4:0	rw	Direct control Input11 Assignment: See Table 14-4 Reset: 00000 _B

Additional Table with Constants

This table describes more than 16 constants.

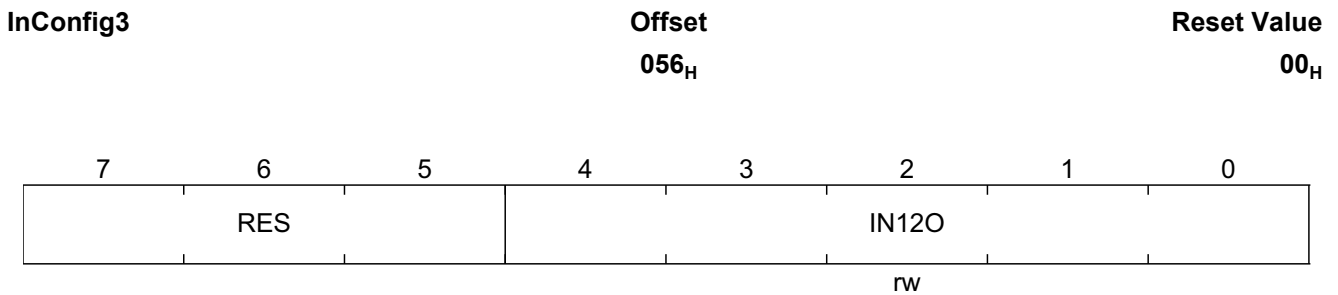
Table 14-4 Constant Values

Name and Description	Value
output5	00000 _B
output6	00001 _B
output7	00010 _B
output8	00011 _B
output9	00100 _B
output10	00101 _B
output11	00110 _B
output12	00111 _B
output13	01000 _B
output14	01001 _B
output15	01010 _B

Table 14-4 Constant Values (cont'd)

Name and Description	Value
output16	01011 _B
output17	01100 _B
output18	01101 _B
output19	01110 _B
output20	01111 _B
output21	10000 _B
output22	10001 _B
output23	10010 _B
output24	10011 _B

InConfig3 locked with LOCK=1



Field	Bits	Type	Description
IN12O	4:0	rw	Direct control Input12 Assignment: See Table 14-5 Reset: 00000 _B

Additional Table with Constants

This table describes more than 16 constants.

Table 14-5 Constant Values

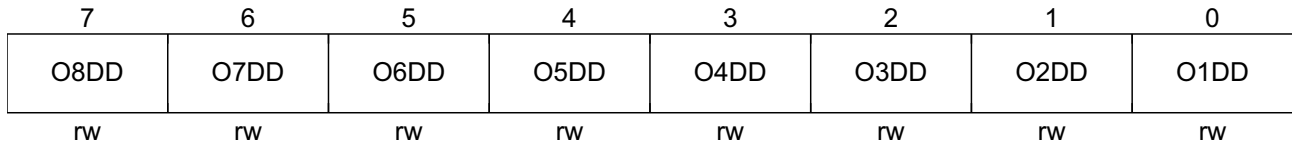
Name and Description	Value
output5	00000 _B
output6	00001 _B
output7	00010 _B
output8	00011 _B
output9	00100 _B
output10	00101 _B
output11	00110 _B
output12	00111 _B
output13	01000 _B
output14	01001 _B
output15	01010 _B
output16	01011 _B
output17	01100 _B
output18	01101 _B
output19	01110 _B
output20	01111 _B
output21	10000 _B
output22	10001 _B
output23	10010 _B
output24	10011 _B

DDConfig0 locked with LOCK=1

DDConfig0

Offset
057_H

Reset Value
00_H



Field	Bits	Type	Description
O8DD	7	rw	Output8 Direct Drive Control: see below Reset: 0 _B
O7DD	6	rw	Output7 Direct Drive Control: see below Reset: 0 _B
O6DD	5	rw	Output6 Direct Drive Control: see below Reset: 0 _B
O5DD	4	rw	Output5 Direct Drive Control: see below Reset: 0 _B
O4DD	3	rw	Output4 Direct Drive Control: see below Reset: 0 _B
O3DD	2	rw	Output3 Direct Drive Control: see below Reset: 0 _B
O2DD	1	rw	Output2 Direct Drive Control: see below Reset: 0 _B
O1DD	0	rw	Output1 Direct Drive Control: 0 _B controlled by MSC/SPI interface 1 _B controlled by Direct Drive Input Reset: 0 _B

DDConfig1 locked with LOCK=1

DDConfig1

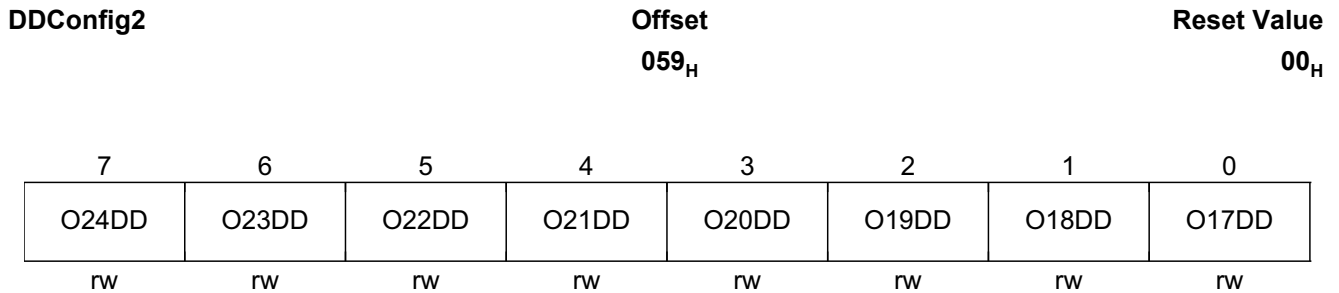
Offset
058_H

Reset Value
00_H



Field	Bits	Type	Description
O16DD	7	rw	Output16 Direct Drive Control: see below Reset: 0 _B
O15DD	6	rw	Output15 Direct Drive Control: see below Reset: 0 _B
O14DD	5	rw	Output14 Direct Drive Control: see below Reset: 0 _B
O13DD	4	rw	Output13 Direct Drive Control: see below Reset: 0 _B
O12DD	3	rw	Output12 Direct Drive Control: see below Reset: 0 _B
O11DD	2	rw	Output11 Direct Drive Control: see below Reset: 0 _B
O10DD	1	rw	Output10 Direct Drive Control: see below Reset: 0 _B
O9DD	0	rw	Output9 Direct Drive Control: 0 _B controlled by MSC/SPI interface 1 _B controlled by Direct Drive Input Reset: 0 _B

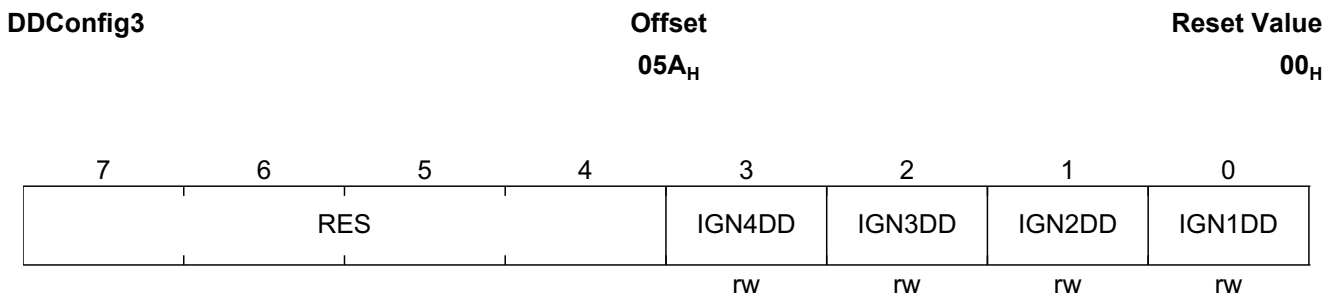
DDConfig2 locked with LOCK=1



Field	Bits	Type	Description
O24DD	7	rw	Output24 Direct Drive Control: see below Reset: 0 _B
O23DD	6	rw	Output23 Direct Drive Control: see below Reset: 0 _B
O22DD	5	rw	Output22 Direct Drive Control: see below Reset: 0 _B
O21DD	4	rw	Output21 Direct Drive Control: see below Reset: 0 _B
O20DD	3	rw	Output20 Direct Drive Control: see below Reset: 0 _B

Field	Bits	Type	Description
O19DD	2	rw	Output19 Direct Drive Control: see below Reset: 0 _B
O18DD	1	rw	Output18 Direct Drive Control: see below Reset: 0 _B
O17DD	0	rw	Output17 Direct Drive Control: 0 _B controlled by MSC/SPI interface 1 _B controlled by Direct Drive Input Reset: 0 _B

DDConfig3 locked with LOCK=1



Field	Bits	Type	Description
IGN4DD	3	rw	Ignition Output4 Direct Drive Control: see below Reset: 0 _B
IGN3DD	2	rw	Ignition Output3 Direct Drive Control: see below Reset: 0 _B
IGN2DD	1	rw	Ignition Output2 Direct Drive Control: see below Reset: 0 _B
IGN1DD	0	rw	Ignition Output1 Direct Drive Control: 0 _B controlled by MSC/SPI interface 1 _B controlled by Direct Drive Input Reset: 0 _B



7	6	5	4	3	2	1	0
O8E	O7E	O6E	O5E	O4E	O3E	O2E	O1E
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
O8E	7	rw	Output8 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O7E	6	rw	Output7 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O6E	5	rw	Output6 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O5E	4	rw	Output5 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O4E	3	rw	Output4 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O3E	2	rw	Output3 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O2E	1	rw	Output2 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O1E	0	rw	Output1 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B

OEConfig1

Offset
05C_H

Reset Value
00_H

7	6	5	4	3	2	1	0
O16E	O15E	O14E	O13E	O12E	O11E	O10E	O9E
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
O16E	7	rw	Output16 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O15E	6	rw	Output15 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O14E	5	rw	Output14 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O13E	4	rw	Output13 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O12E	3	rw	Output12 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O11E	2	rw	Output11 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O10E	1	rw	Output10 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O9E	0	rw	Output9 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B

OEConfig2

Offset

Reset Value

05D_H

00_H

7	6	5	4	3	2	1	0
O24E	O23E	O22E	O21E	O20E	O19E	O18E	O17E
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
O24E	7	rw	Output24 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O23E	6	rw	Output23 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O22E	5	rw	Output22 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O21E	4	rw	Output21 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O20E	3	rw	Output20 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O19E	2	rw	Output19 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O18E	1	rw	Output18 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
O17E	0	rw	Output17 Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B

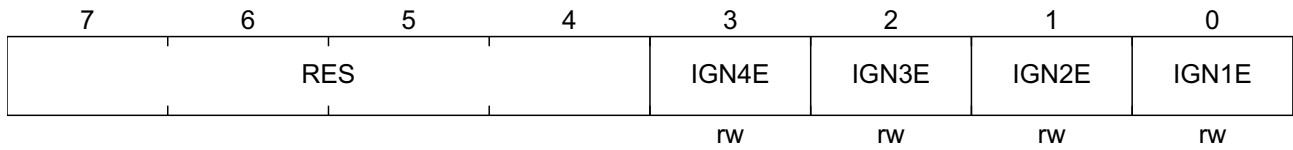
OEConfig3

Offset

Reset Value

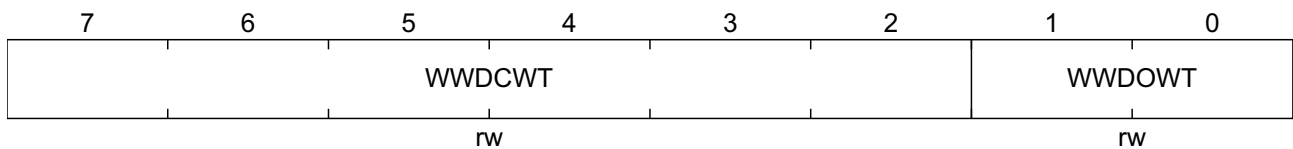
05E_H

00_H



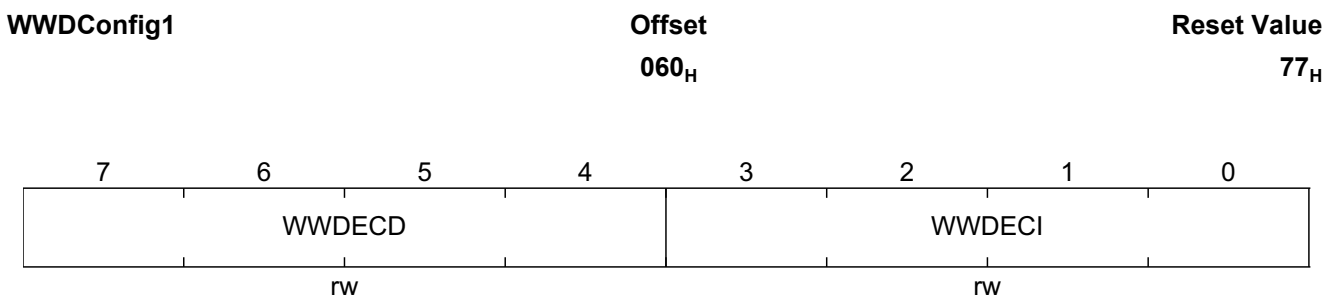
Field	Bits	Type	Description
IGN4E	3	rw	Ignition 4 Output Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
IGN3E	2	rw	Ignition 3 Output Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
IGN2E	1	rw	Ignition 2 Output Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B
IGN1E	0	rw	Ignition 1 Output Enable Bit: 0 _B output disabled 1 _B output enabled Reset: 0 _B

WWDConfig0 **Offset** **Reset Value**
05F_H **FF_H**

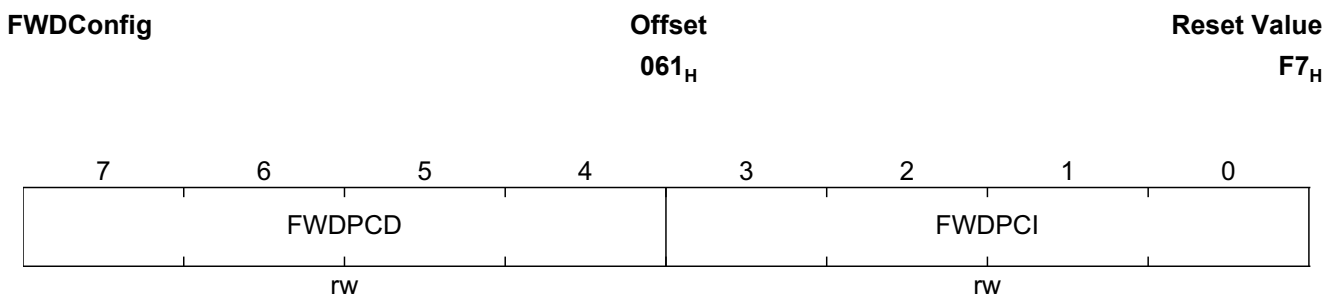


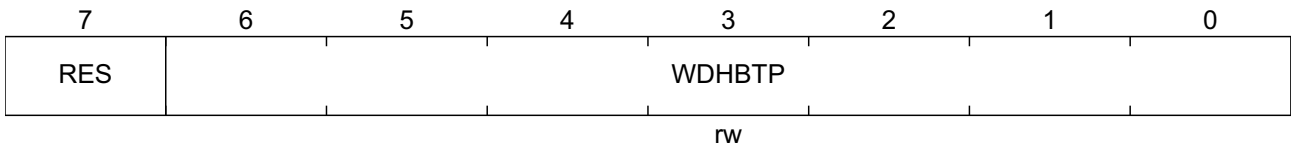
Field	Bits	Type	Description
WWDCWT	7:2	rw	Window Watchdog Closed Window Time: 000000 _B no change - old setting used for open and closed window 000001 _B 1,6ms 111111 _B 100,8ms Reset: 111111 _B

Field	Bits	Type	Description
WWDOWT	1:0	rw	Window Watchdog Open Window Time: 00 _B 3,2ms 01 _B 6,4ms 10 _B 9,6ms 11 _B 12,8ms Reset: 11 _B



Field	Bits	Type	Description
WWDECD	7:4	rw	Window Watchdog Error Counter Decrement: 0000 _B -1 0001 _B -2 1111 _B -16 Reset: 0111 _B
WWDECI	3:0	rw	Window Watchdog Error Counter Increment: 0000 _B +1 0001 _B +2 1111 _B +16 Reset: 0111 _B

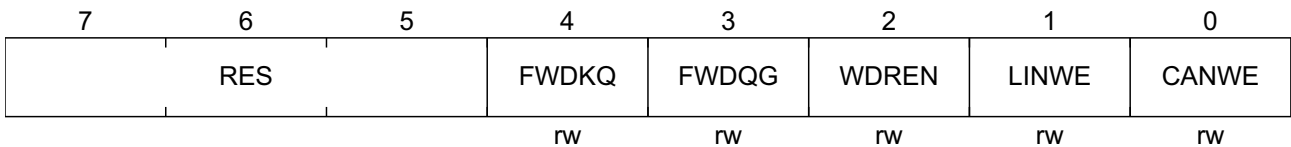




Field	Bits	Type	Description
WDHBTTP	6:0	rw	Watchdog Heartbeat Timer Period: 0000000 _B no change 0000001 _B 1,6ms 0000010 _B 3,2ms 1111111 _B 203,2ms Reset: 1000111 _B

WDConfig1 locked with LOCK=1

WDConfig1 **Offset** **Reset Value**
064_H **03_H**

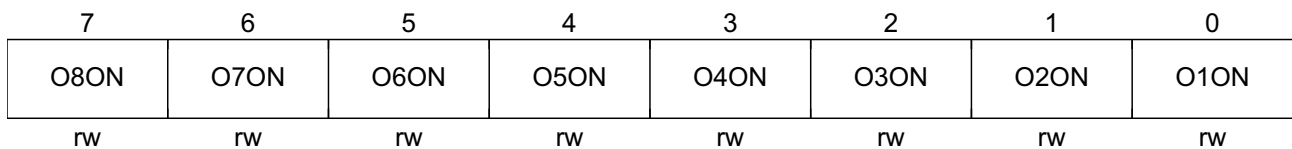


Field	Bits	Type	Description
FWDKQ	4	rw	Functional Watchdog Keep Question Setup: 0 _B No influence to question generation in case of window watchdog error 1 _B Keep question in case of window watchdog error Reset: 0 _B
FWDQG	3	rw	Functional Watchdog Question Generation: 0 _B Question period 16 1 _B Question period 256 Reset: 0 _B
WDREN	2	rw	Watchdog Reset Enable Bit: 0 _B reset disabled 1 _B reset enabled Reset: 0 _B
LINWE	1	rw	LIN Operation Mode during Watchdog Error Setup: 0 _B receive only mode 1 _B according ComConfig1.LIN Reset: 1 _B

Field	Bits	Type	Description
CANWE	0	rw	CAN Operation Mode during Watchdog Error Setup: 0_B receive only mode 1_B according ComConfig1.CAN Reset: 1_B

14.6 Control Register

Cont0 Offset Reset Value
 $07B_H$ 00_H



Field	Bits	Type	Description
O8ON	7	rw	Output8 Switch on Control Bit: 0_B off 1_B on Reset: 0_B
O7ON	6	rw	Output7 Switch on Control Bit: 0_B off 1_B on Reset: 0_B
O6ON	5	rw	Output6 Switch on Control Bit: 0_B off 1_B on Reset: 0_B
O5ON	4	rw	Output5 Switch on Control Bit: 0_B off 1_B on Reset: 0_B
O4ON	3	rw	Output4 Switch on Control Bit: 0_B off 1_B on Reset: 0_B

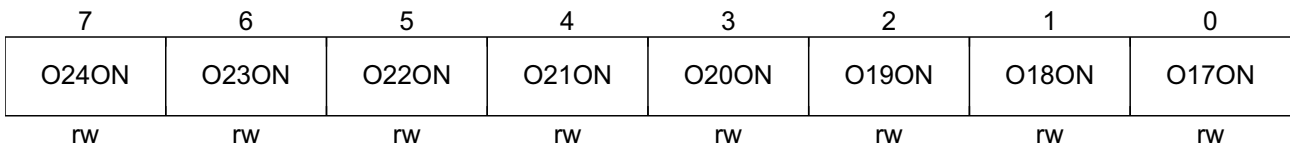
Field	Bits	Type	Description
O3ON	2	rw	Output3 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O2ON	1	rw	Output2 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O1ON	0	rw	Output1 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B

Cont1								Offset	Reset Value
								07C _H	00 _H
7	6	5	4	3	2	1	0		
O16ON	O15ON	O14ON	O13ON	O12ON	O11ON	O10ON	O9ON		
rw	rw	rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
O16ON	7	rw	Output16 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O15ON	6	rw	Output15 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O14ON	5	rw	Output14 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O13ON	4	rw	Output13 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B

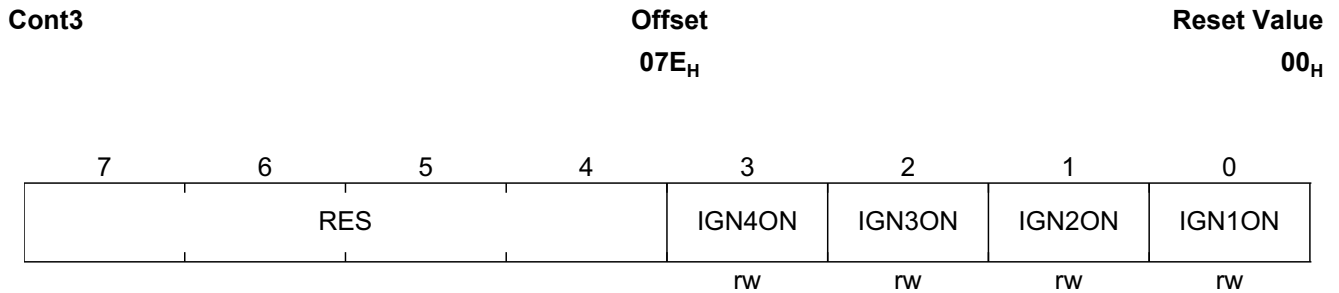
Field	Bits	Type	Description
O12ON	3	rw	Output12 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O11ON	2	rw	Output11 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O10ON	1	rw	Output10 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O9ON	0	rw	Output9 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B

Cont2 Offset Reset Value
07D_H 00_H



Field	Bits	Type	Description
O24ON	7	rw	Output24 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O23ON	6	rw	Output23 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O22ON	5	rw	Output22 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B

Field	Bits	Type	Description
O21ON	4	rw	Output21 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O20ON	3	rw	Output20 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O19ON	2	rw	Output19 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O18ON	1	rw	Output18 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
O17ON	0	rw	Output17 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B



Field	Bits	Type	Description
IGN4ON	3	rw	Ignition Output4 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
IGN3ON	2	rw	Ignition Output3 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B

Field	Bits	Type	Description
IGN2ON	1	rw	Ignition Output2 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B
IGN1ON	0	rw	Ignition Output1 Switch on Control Bit: 0 _B off 1 _B on Reset: 0 _B

15 SPI

Alternatively to the MSC communication interface a SPI interface is available. It uses the pins *SIP*, *SDO*, *CSN* and *FCLP*. The configuration is done via the pins *FCLN* and *SIN*. *FCLN* must be connected to *VDDIO* and *SIN* must be connected to *AGND*. In SPI mode the output stage of the pin *SDO* is set to push pull operation (definition and description see [Chapter 13.2](#) and [Chapter 13.4](#)).

The definition of the registers is the same as for the MSC communication (see [Chapter 14](#)), only the frame is SPI specific (see [Figure 67](#) and [Chapter 15.1](#)). Multiple read commands are not allowed.

There is no monitoring of valid transmissions implemented (like MSC monitoring, see [Chapter 13.1.1](#)).

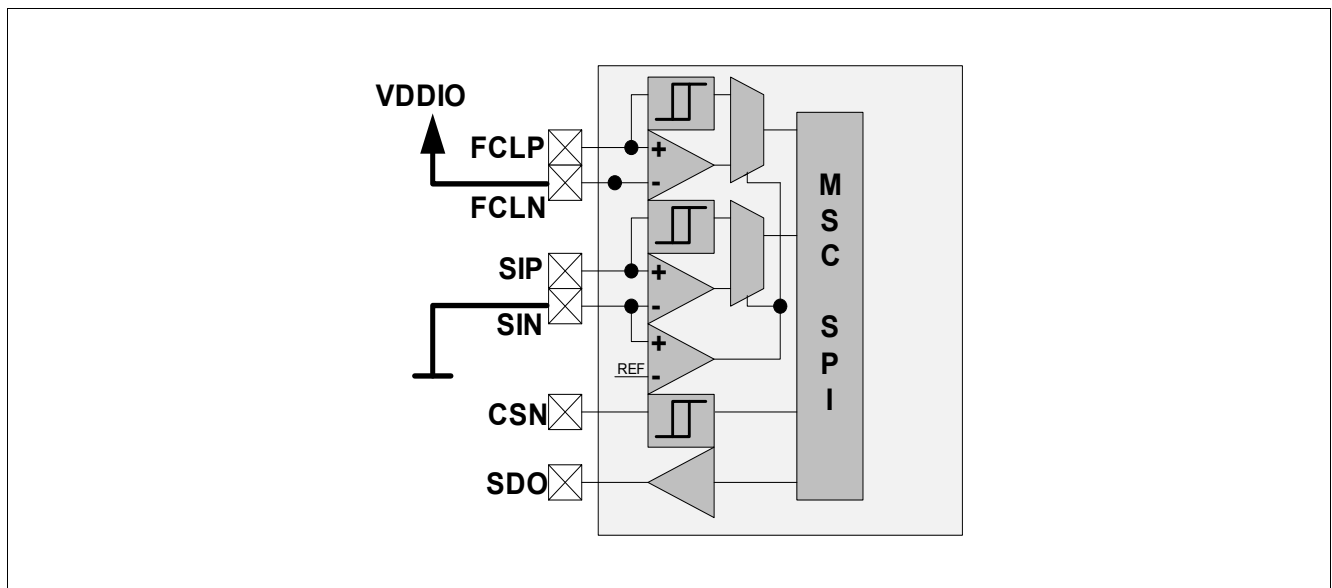


Figure 66 Block diagram of the SPI interface

15.1 SPI Protocol

The principle of the SPI communication is shown in [Figure 67](#). The message from the micro controller must be sent LSB first. The data from the *SDO* pin is sent LSB first. The TLE8888-1QK samples data from the *SIP* pin on the falling edge of *FCLP* and shifts data out of the *SDO* pin on the rising edge of *FCLP*. Each access must be terminated by a rising edge of *CSN*.

All SPI messages must be exactly 16-bits long, otherwise the SPI message is discarded and the bit **COMFE** in diagnosis register **ComDiag** is set to "1".

There is one message delay in the response to each message (i.e. the response for message N will be returned during message N+1).

There are two valid access possible:

- Write access to registers with write permission: the answer is 1 for the $\overline{R/W}$ bit, the address and the content of the register
- Read access to register with read permission: the answer is 0 for the $\overline{R/W}$ bit, the address and the content of the register

Everything else is not executed.

Note: Write access to multiple read commands are also not valid in SPI mode.

Status Flag Indication: after the falling edge of *CSN* and before the first rising edge of *FCLP* the level of the *SDO* indicates an OR combination of the status of the central failure bit **CF** and the central overtemperature bit **COT** of the diagnosis register **Diag0**.

With this feature during every SPI communication a check of the diagnosis status can be done without additional read access of the diagnosis register.

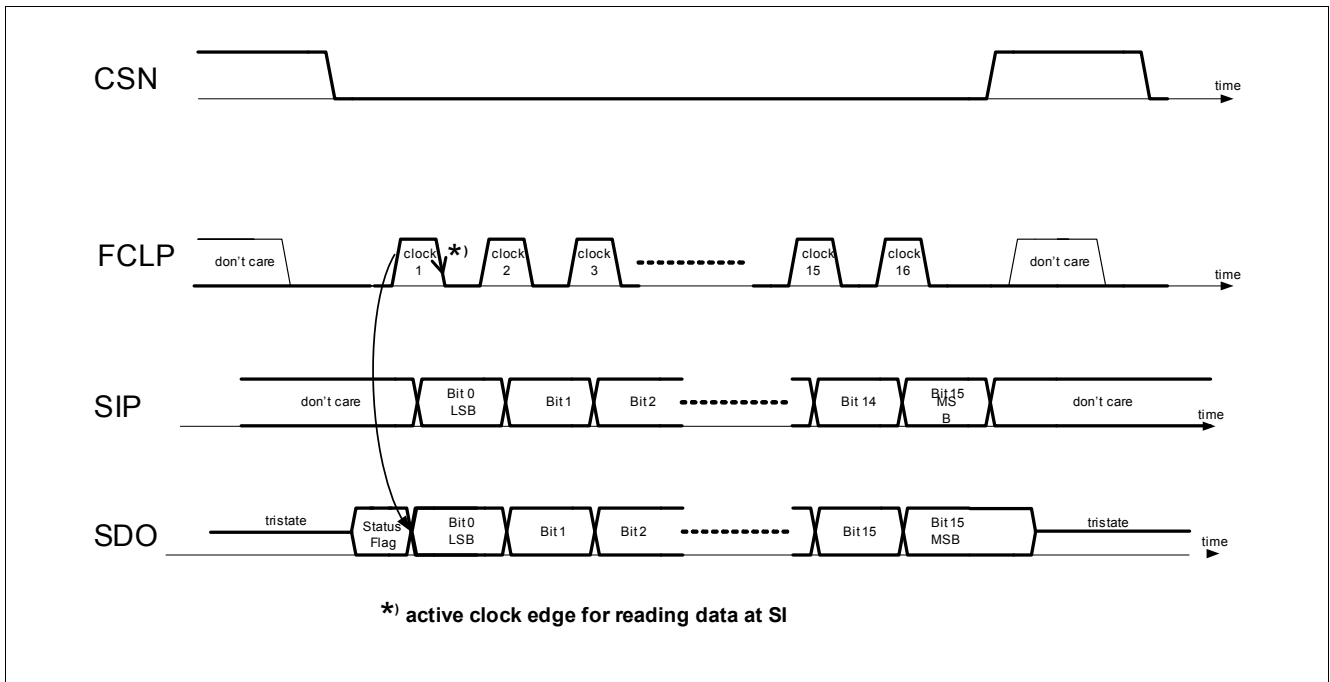


Figure 67 SPI Protocol

SPI Answers:

- during power on reset: SPI commands are ignored, *SDO* is always tristate
- after power on reset: the address and the content of the status register **OpStat0** is transmitted with the next SPI transmission
- during watchdog reset: SPI commands are ignored, *SDO* has the value of the status flag
- after watchdog reset: the address and the content of the diagnosis register **FWDStat1** is transmitted with the first SPI transmission after the low to high transition of *RST*
- after a read or write command: the address and content of the selected register is transmitted with the next SPI transmission (for not existing addresses or wrong access mode the data is always “0”)
- after an invalid communication frame: the address and the content of the diagnosis register **Diag0** is transmitted with the next SPI transmission and the bit **COMFE** in diagnosis register **ComDiag** is set to “1”

15.2 SPI Frame Definition

Overview SPI Frame

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	C7	C6	C5	C4	C3	C2	C1	C0

Field	Bits	Type	Description
C0	0		$\overline{\text{R/W}}$ Bit: defines the access to the register
C[7:1]	[7:1]		Address Bits, definition see Chapter 14
CD[7:0]	[15:8]		Data Bits, definition see Chapter 14

15.3 Electrical Characteristics SPI

Table 51 Electrical Characteristics Communication

$V_S=13.5V$, $V_{V5V}=5V$, $T_j=-40$ to $150^\circ C$, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SPI detection threshold for <i>SIN</i>	V_{FCLN_SPI}	0.3	–	0.7	V		P_15.1
Single ended mode detection threshold for <i>FCLN</i>	V_{FCLN_single}	2	–	3	V		P_15.2
<i>SDO</i>						see Chapter 13.4	P_15.3
Input low level (<i>SIP</i> , <i>FCLP</i> , <i>CSN</i>)	V_{INn_L}	-0.3	–	0.8	V		P_15.4
Input high level (<i>SIP</i> , <i>FCLP</i> , <i>CSN</i>)	V_{INn_H}	1.6	–	5.5	V		P_15.5
Input hysteresis (<i>SIP</i> , <i>FCLP</i> , <i>CSN</i>)	V_{INn_Hys}	0.1	–	0.5	V		P_15.6
Clock frequency	f_{SPI}	–	–	5	MHz		P_15.7

16 EMC Requirements

16.1 ISO Pulse Tests

Definitions for all ISO pulse test on application including the TLE8888-1QK are regarding standard ISO 7637-2:2011. Following amplitude definition for the tests are required:

- Pulse 3a: VS= -140V, all outputs available on ECU connector
- Pulse 3b: VS= 140V, all outputs available on ECU connector
- Pulse 5: VS= +38.5V (clamped), td=400ms (ECU reset is permitted under this test, outputs will be switched off)

The tests are performed only on application level.

17 Application Information

Note: The information in this chapter is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Note: These are very simplified examples of application circuits. The functions must be verified in the real application.

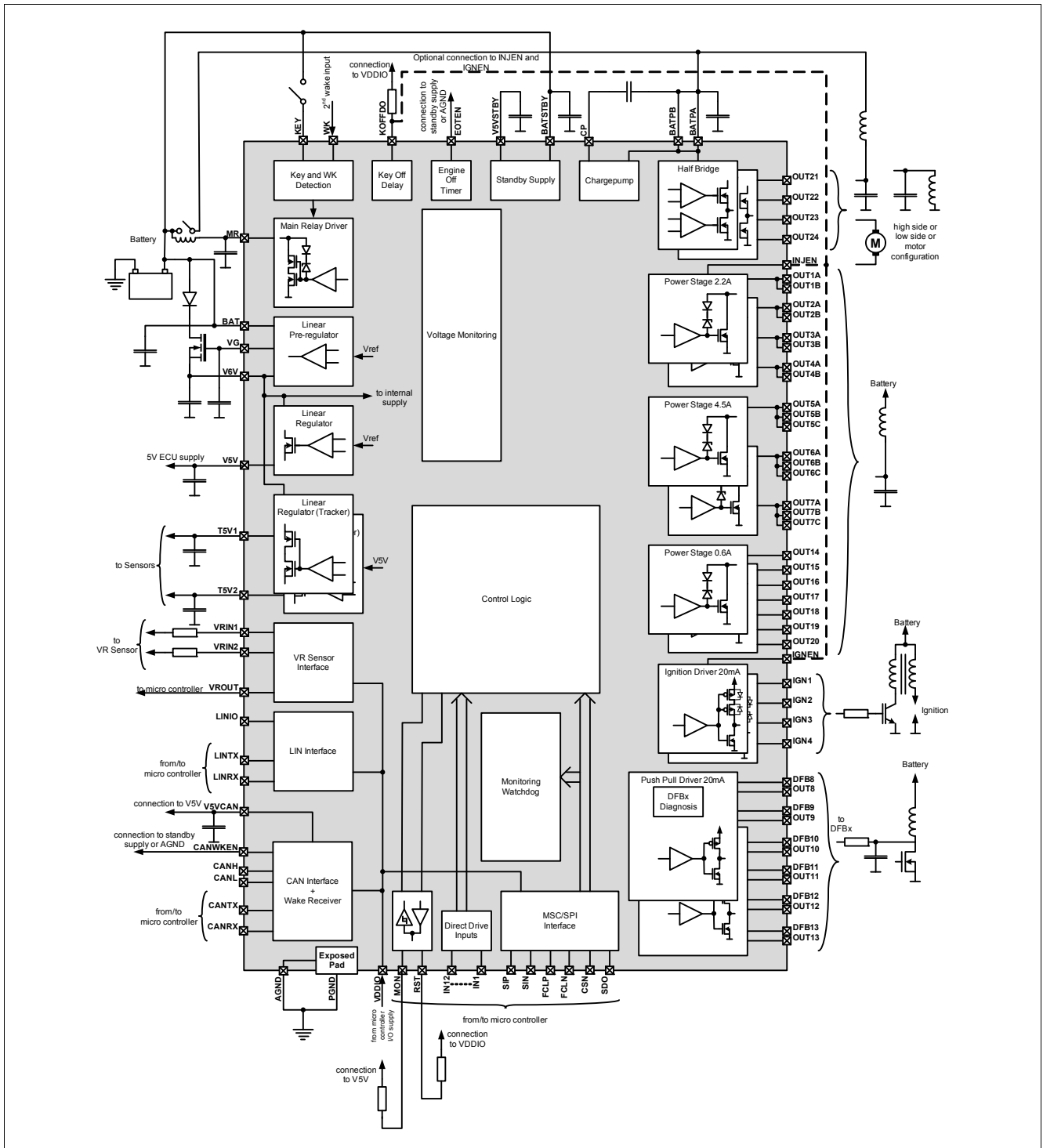


Figure 68 Application Diagram

17.1 Supply Systems

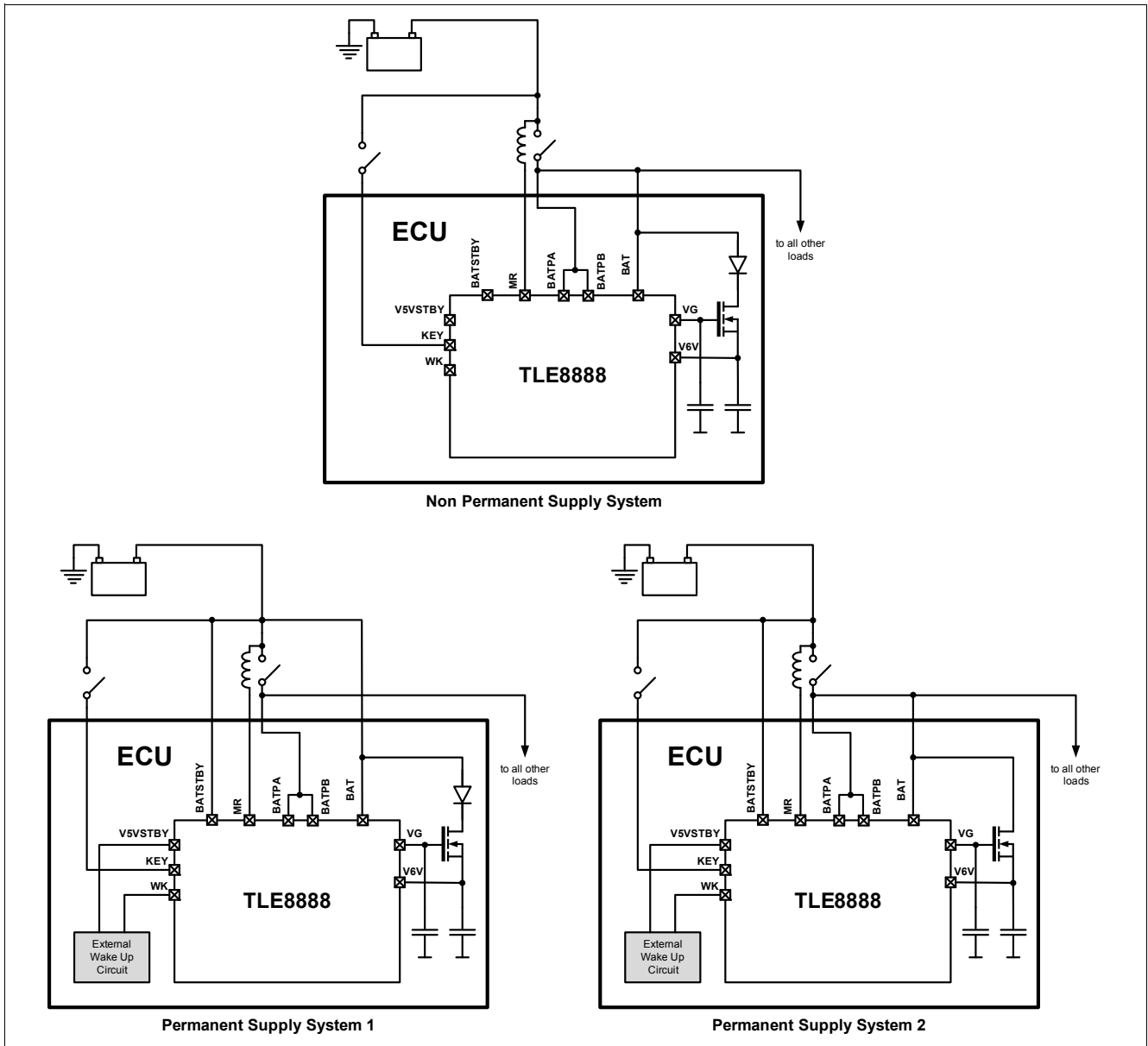


Figure 69 Application Diagram Supply Systems

In **Figure 69** three setups for connecting the battery supply to the TLE8888-1QK are shown. With non permanent battery supply there is no standby supply available and all functions related to this supply (e.g. engine off timer) are not active. Wake up could be done by a signal at the pins *KEY* and *WK*.

In a permanent supply system the standby supply is permanently connected to the battery and all functions related to this supply can be enabled (e.g. CAN remote wake up). The pins *BATPA* and *BATPB* must be connected to the switched battery supply because there is no special mode to reduce the current consumption in standby mode. The pin *BAT* and the external MOSFET of the pre regulator are allowed to be connected permanently to the battery.

17.2 VR Sensor Interface

For Hall sensor signal detection in [Figure 70](#) and [Figure 71](#) different proposals for the external devices are shown. For the description of the set ups see [Chapter 10](#)

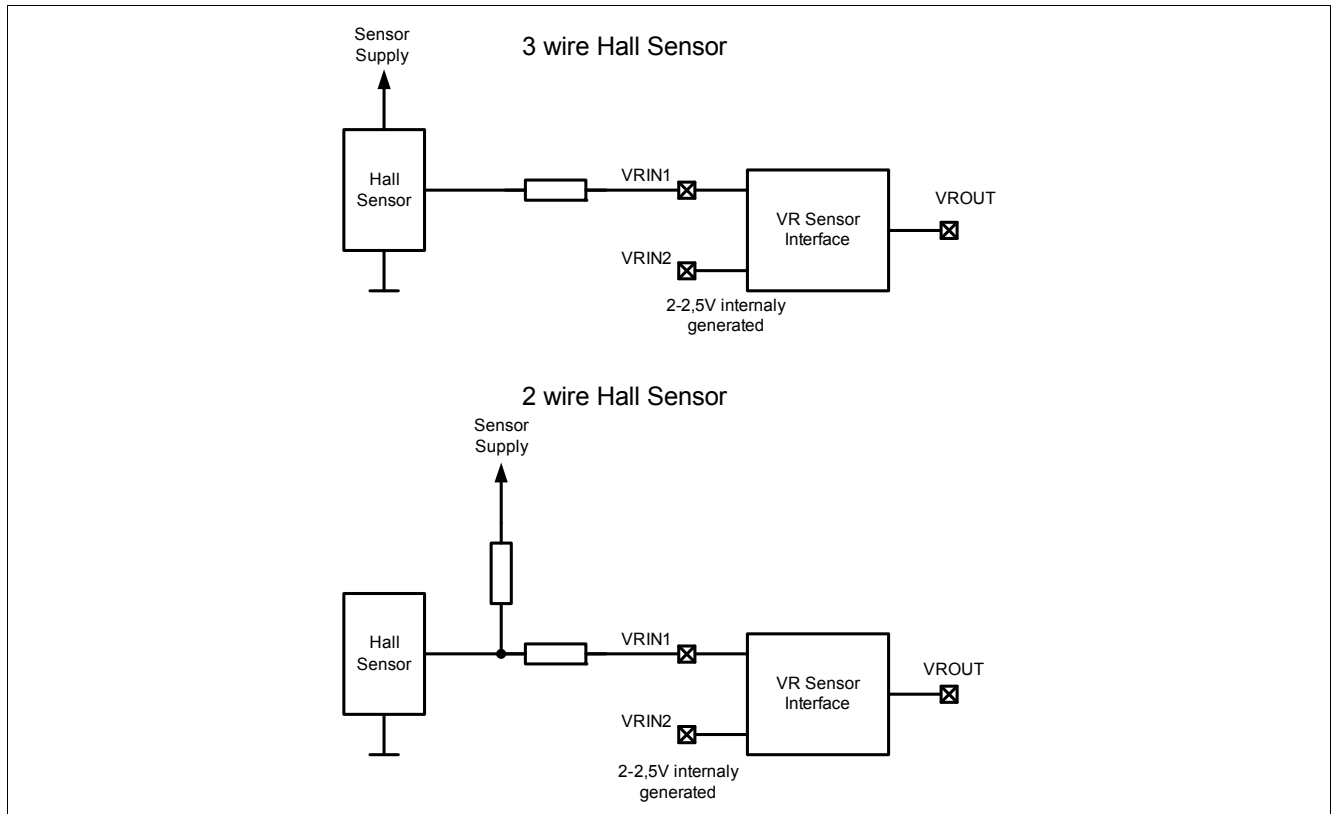


Figure 70 Application Circuit for VR Sensor Interface used for Hall Sensor in Hall Mode Set Up

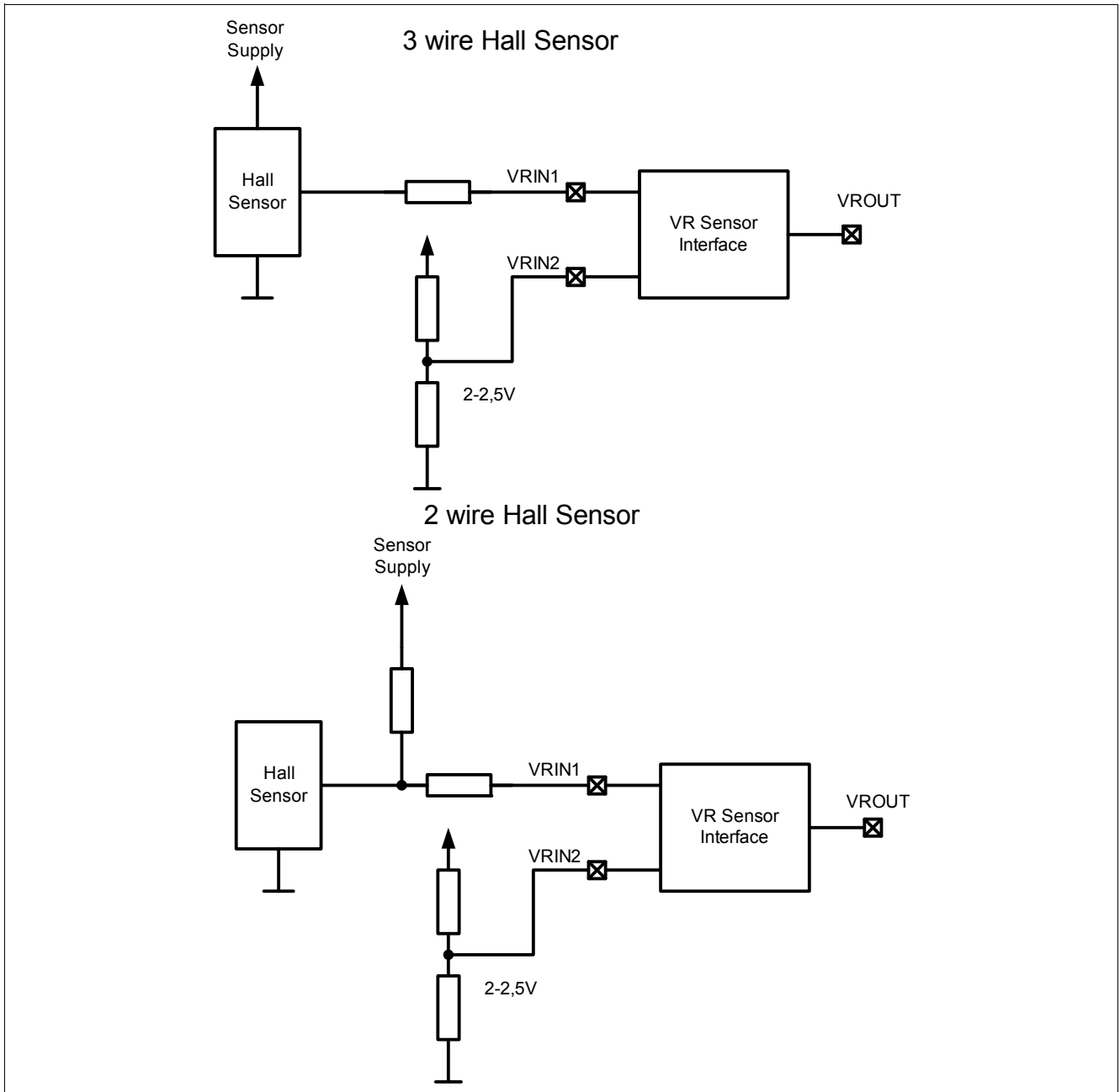


Figure 71 Application Circuit for VR Sensor Interface used for Hall Sensor in Auto, Semi Auto and Manual Detection Mode Set Up

18 Package Outlines

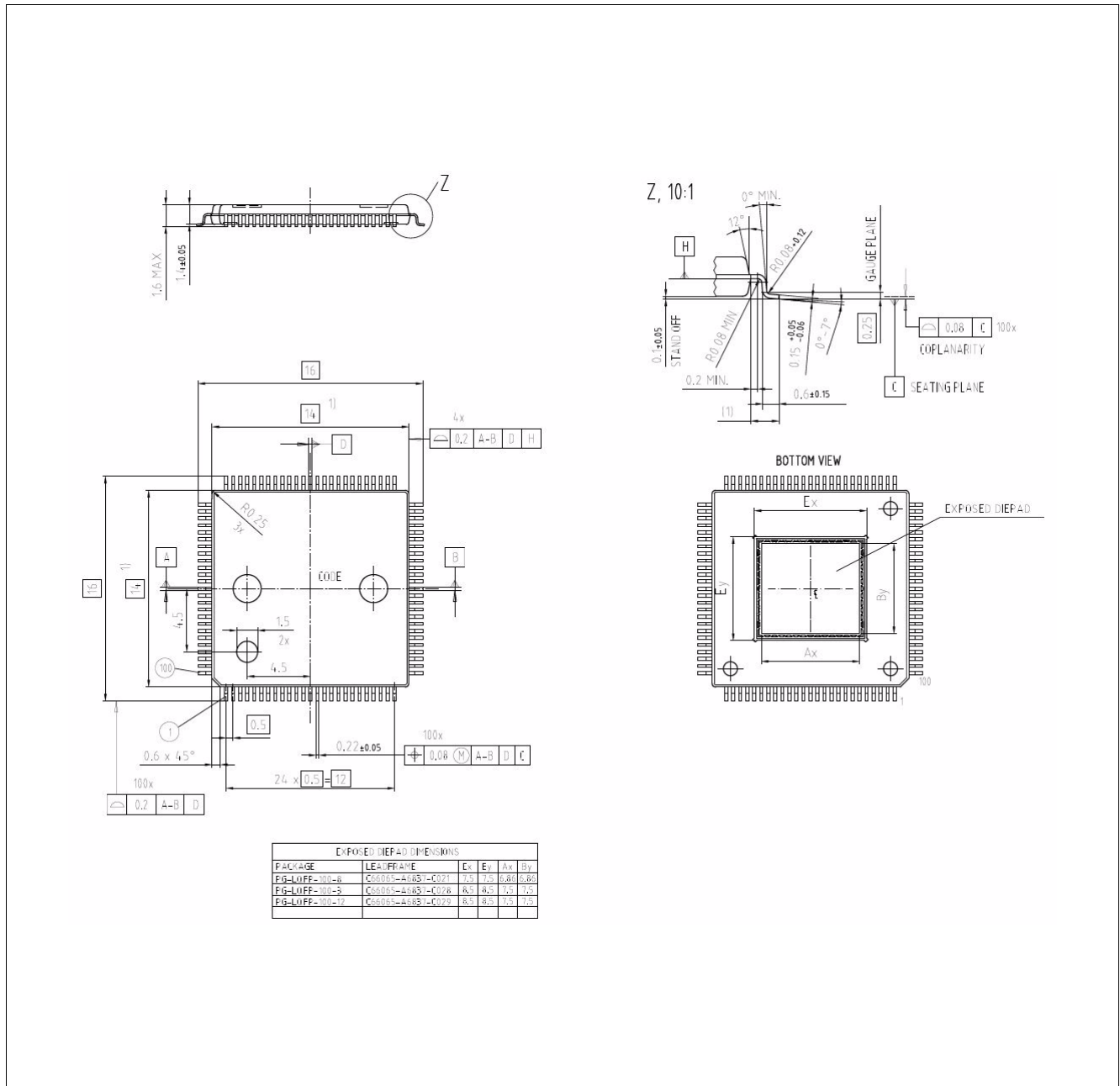


Figure 72 LQFP-100

For the LQFP-100 package the lead frame version C66065-A6837-C029 with an exposed pad size of 8.5mm*8.5mm is used.

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

19 Revision History

Revision	Date	Changes
V1.1	2014-08-20	on all pages: general name changed to "TLE8888-1QK" and date and revision
V1.1	2014-08-20	page 5 and 6: 2 device types added
V1.1	2014-08-20	page 29: parameter P_5.3.24 min/max changed
V1.1	2014-08-20	page 52: parameter P_7.5.2 and P_7.5.11 max defined
V1.1	2014-08-20	page 57: parameter P_8.8.38, P_8.8.39, P_8.8.40, P_8.8.42, P_8.8.43 and P_8.8.44 definiton improved
V1.1	2014-08-20	page 58: parameter P_8.8.45 definiton improved
V1.1	2014-08-20	page 62: table 25 corrected
V1.1	2014-08-20	page 100: PGND reference pin changed
V1.1	2014-08-20	page 2, 9, 10, 11, 17, 18, 20, 21, 22, 26, 38, 39, 43, 44, 45, 48, 49, 52, 56, 58, 196: missing variable names added
V1.0	2014-03-13	Data Sheet

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