MC3232A

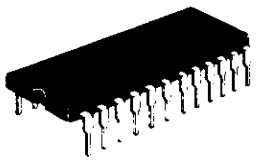
MEMORY ADDRESS MULTIPLEXER

The Motorola MC3232A is an address multiplexer and refresh counter for 16-pin 4K dynamic RAMs that require a 64-cycle refresh. It multiplexes twelve system address bits to the six input address pins of the memory device. The MC3232A also contains a 6-bit refresh counter that is clocked externally to generate the 64 sequential addresses required for refresh. The high performance of the MC3232A will enhance the high speed of the fast N-channel RAMs such as the MCM4027.

- Simplifies 16-Pin 4K Dynamic Memory Design
- Reduces Package Count
- 6-Bit Binary Counter for 64 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  I_F = 0.25 mA Max
- Schottky TTL for High Performance Address Input to Output Delay
  t_{AO} = 25 ns @ C_L = 250 pF, 9.0 ns Max @ C_L = 15 pF
- Second Source to Intel 3232
  (Detect Zero Function Not Included and Additional Power Fail Feature Added at Pin 13)

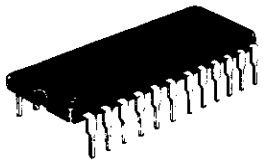
MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUITS

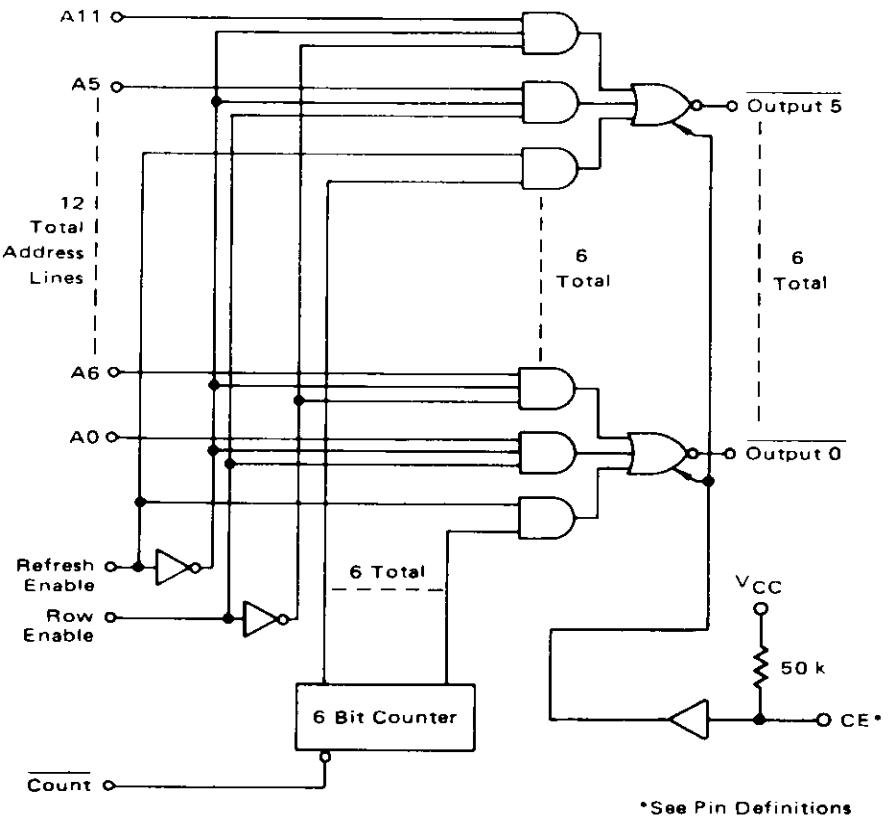


L SUFFIX
CERAMIC PACKAGE
CASE 623

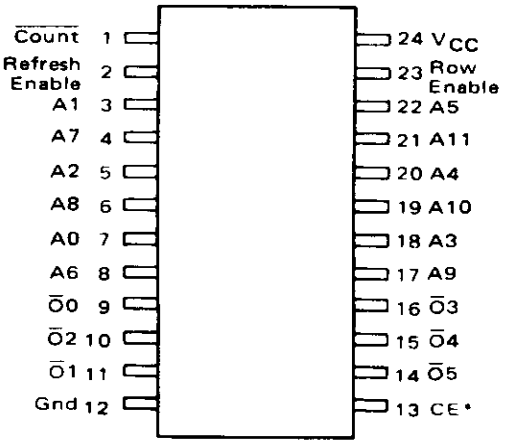
P SUFFIX
PLASTIC PACKAGE
CASE 649



LOGIC DIAGRAM



*See Pin Definitions



Note: A0 Through A5 Are Row Addresses
A6 Through A11 Are Column Addresses
*See Pin Definitions

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A5)
L	L	Column Address (A6 through A11)

Count — Advances Internal Refresh Counter

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C, typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State (V_{IL} = 0.45 V)	I_{IL}	–	-0.04	-0.25	mA
Input Current, High Logic State (V_{IH} = 5.5 V)	I_{IH}	–	–	10	μA
Input Voltage, Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	–	–	V
Output Voltage, Low Logic State (I_{OL} = 5.0 mA)	V_{OL}	–	0.25	0.4	V
Output Voltage, High Logic State (I_{OH} = -1.0 mA)	V_{OH}	2.8	4.0	–	V
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	-0.8	-1.5	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	75	125	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C, typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					
Address Input to Output	t_{AO}				ns
(Load = 1 TTL, C_L = 250 pF)		–	12	25	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		–	6.0	9.0	
Row Enable to Output	t_{OO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	27	41	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	12	27	
Refresh Enable to Output	t_{EO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	30	45	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	14	27	
$\overline{\text{Count}}$ Pulse Width	$t_{W\overline{C}}$	30	–	–	ns
Counting Frequency	$f_{\overline{C}}$	5.0	10	–	MHz

FIGURE 1 – AC WAVEFORMS with MCM6604 NORMAL CYCLE

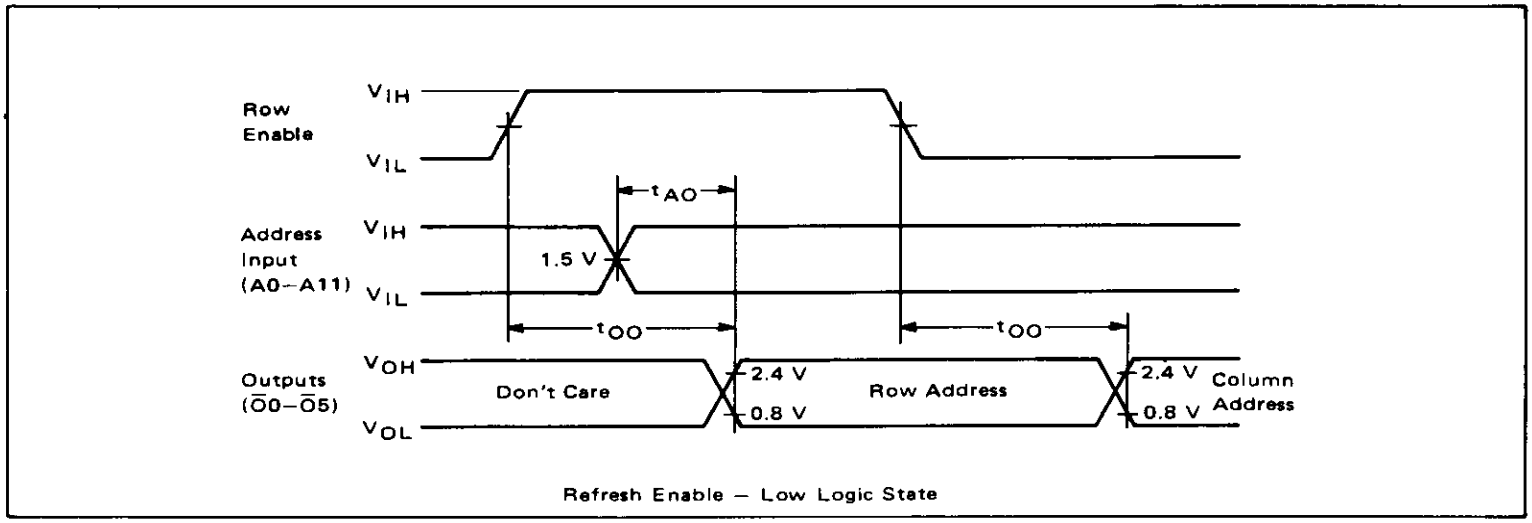
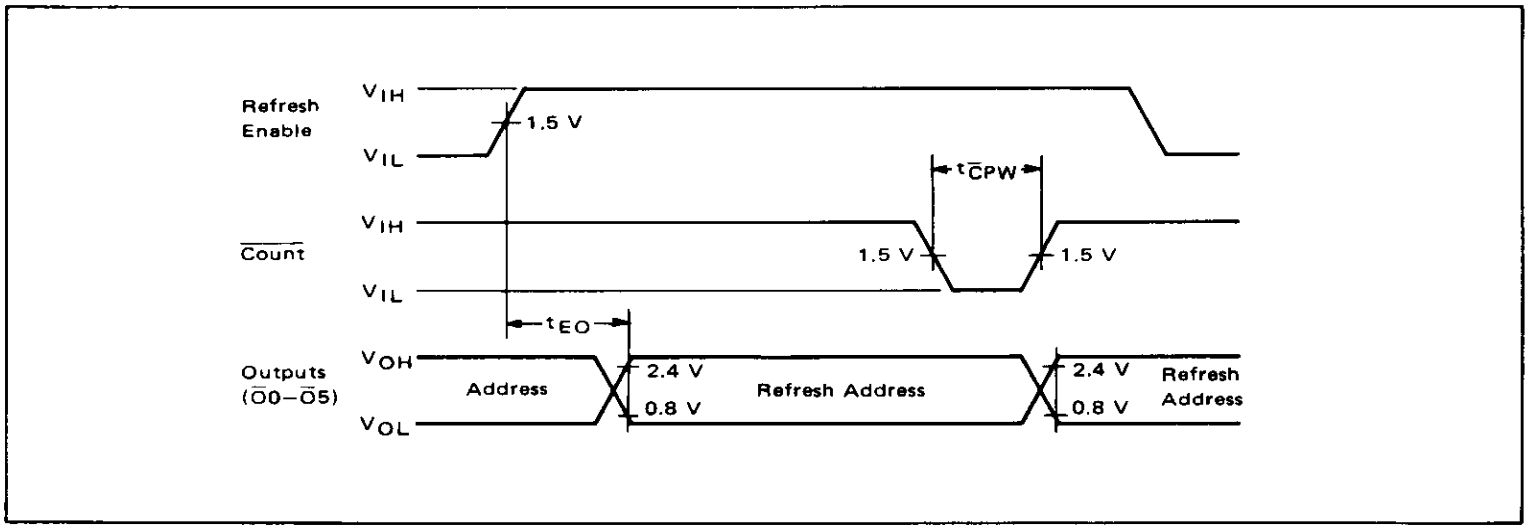


FIGURE 2 – REFRESH CYCLE



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

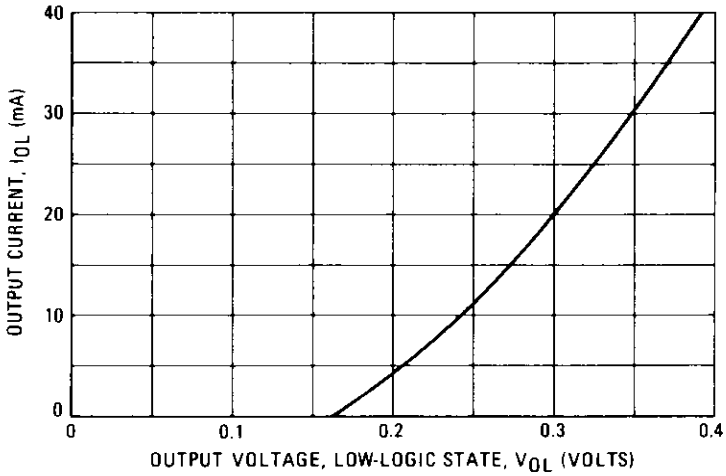
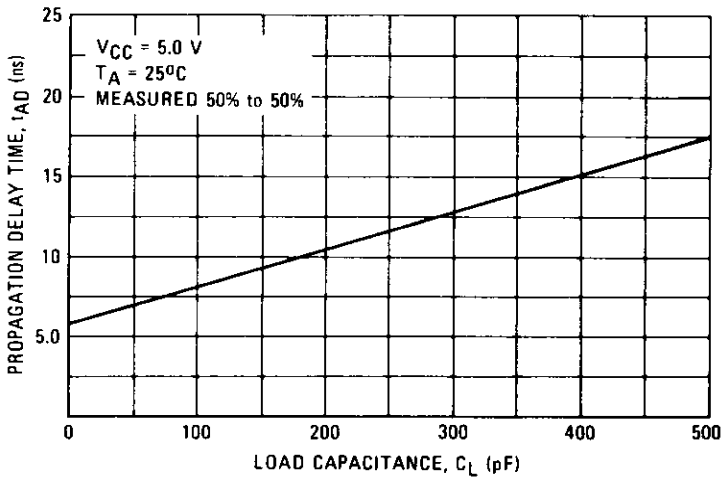


FIGURE 4 – PROPAGATION DELAY versus LOAD CAPACITANCE
Row or Column Address to Output



PIN DEFINITIONS

$\overline{\text{Count}}$ Input – Pin 1

Active low input increments internal 6-bit counter by one for each count pulse in.

Refresh Enable Input – Pin 2

Active high input which determines whether the MC3232A is in refresh mode (H) or address enable (L).

A0–A5 Inputs – Pins 7, 3, 5, 18, 20, 22

Row address inputs.

A6–A11 Inputs – Pins 8, 4, 6, 17, 19, 21

Column address inputs.

$\overline{O}$0–$\overline{O}$5 Outputs – Pins 9, 11, 10, 16, 15, 14

Address outputs to memories. Inverted with respect to address inputs.

Gnd – Pin 12

Power supply ground.

CE Input – Pin 13

Optional use, chip enable control pin. Left open, an internal 50 kΩ pullup resistor keeps this pin high and the MC3232A is a functional replacement for the Intel 3232 (without detect zero function). As an active input, when pulled low, all 3232A outputs go three-state. Regardless of Pin 13 (CE) condition, when power (V_{CC}) is removed, all 3232A outputs go three-state. In addition, the refresh address counter is reset to all 1s so that upon return of supply power, control of refresh addressing can be returned to the MC3232A (by pulling Pin 13 high) at a known address (i.e., all 1s). This option is available tested by consulting factory.

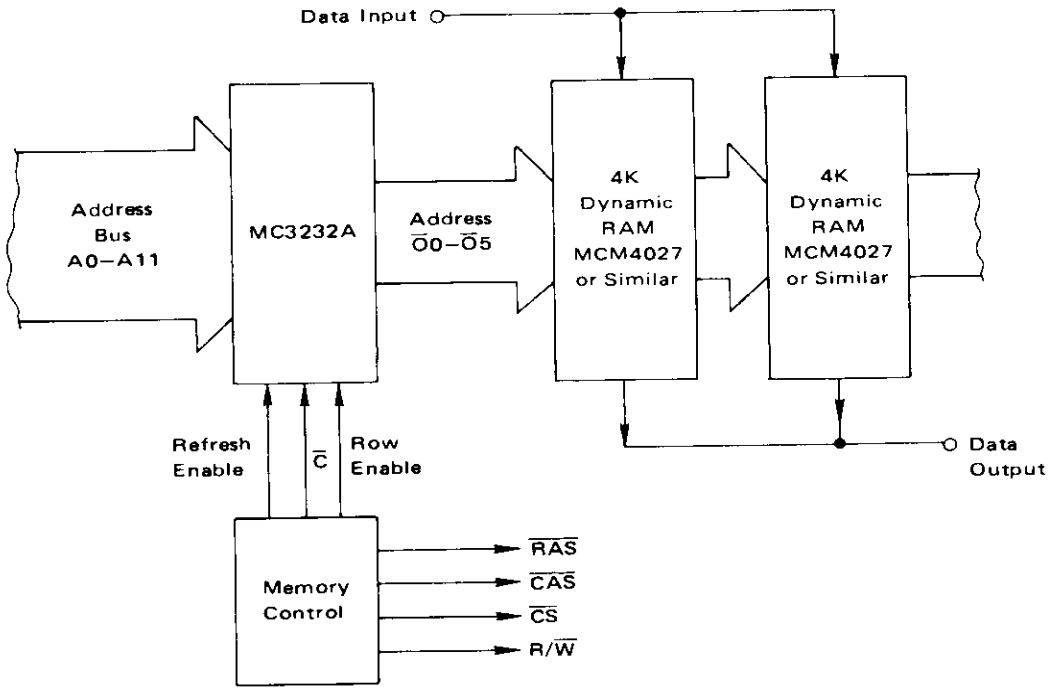
Row Enable Input – Pin 23

High input selects row, low input selects column addresses of the driven memories.

V_{CC} – Pin 24

+5 V power supply input. Due to high capacitance drive capability, a 0.1 μF capacitor should be used to ground along with careful V_{CC} and Gnd Bus layout.

GENERAL 4K DYNAMIC RAM
SIMPLIFIED BLOCK DIAGRAM



TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs