NWP2081T

Half-bridge driver IC

Rev. 1 — 3 September 2013 Product data sheet

1. General description

The NWP2081T is a high-voltage monolithic integrated circuit made using the latch-up free Silicon-On-Insulator (SOI) process. The circuit is designed for driving MOSFETs in a half-bridge configuration.

2. Features and benefits

- Latch-up free and robust half-bridge driver
- Output driver capability: $I_{O(sink)}$ = 400 mA and $I_{O(source)}$ = 200 mA
- Maximum frequency 800 kHz
- Outputs in phase with CLK input
- Adjustable dead-time
- Low active shutdown input

3. Applications

- Driver (via external MOSFETs) for any kind of load in a half-bridge configuration

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NWP2081T	SO8	plastic small outline package; 8 leads	SOT96-1

5. Block diagram

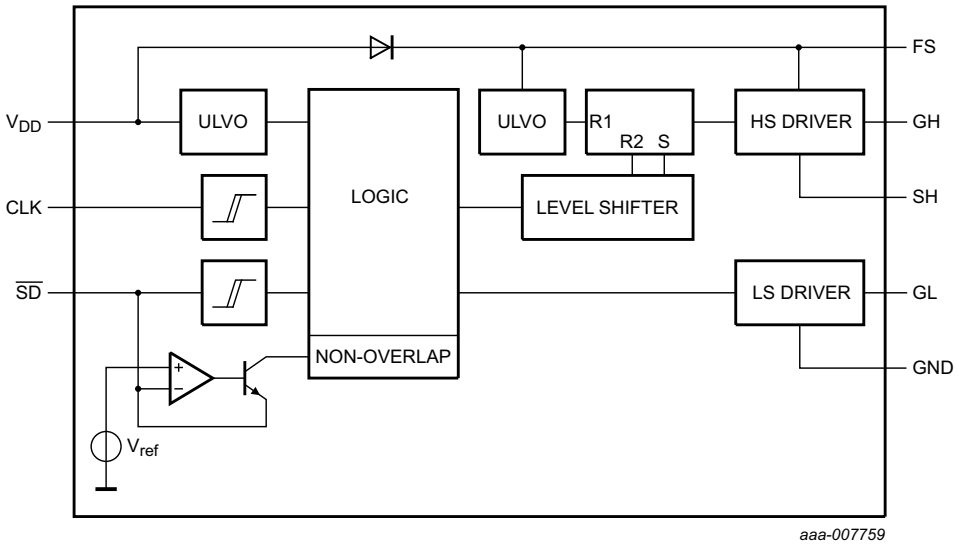

Fig 1. NWP2081T block diagram

Refer to Figure 4 for detailed information on the required application components.

6. Pinning information

6.1 Pinning

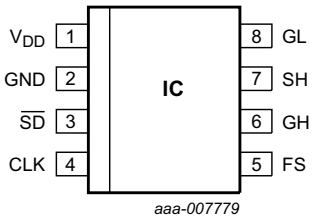

Fig 2. NWP2081T pinning diagram

6.2 Pin description

Table 2. Pin description NWP2081T

Symbol	NWP2081T (SO8)	Description
V_{DD}	1	IC supply
GND	2	IC ground and low-side driver return
$\overline{SD}$	3	low active analog shutdown input and non-overlap time setting
CLK	4	clock logic input
FS	5	floating supply voltage

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Table 2. Pin description NWP2081T *...continued*

Symbol	NWP2081T (SO8)	Description
GH	6	high-side MOSFET gate
SH	7	high-side MOSFET source
GL	8	low-side MOSFET gate

7. Functional description

7.1 Start-up state

The IC enters the start-up state when the supply voltage on pin V_{DD} increases. In the start-up state, the high-side power transistor is non-conducting and the low-side power transistor is switched on. The internal circuit is reset and the capacitor on the bootstrap pin FS is charged. The start-up state is defined until the value of V_{DD} = the $V_{DD(start)}$ value. After which the IC switches to the oscillation state.

The circuit enters the start-up state again when the voltage on pin $V_{DD} < V_{DD(stop)}$.

7.2 NWP2081T oscillation state

In the oscillation state, the output voltage of the GL and GH drivers depend on the logical signals CLK and $\overline{SD}$ (see Table 3).

Table 3. NWP2081T logic table

State	CLK	$\overline{SD}$	GH	GL
start-up	-	-	LOW	HIGH
oscillation	0	1	LOW	HIGH
oscillation	1	1	HIGH	LOW
oscillation	0	0	LOW	LOW
oscillation	1	0	LOW	LOW

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7.3 NWP2081T non-overlap time

The external resistor (R_{SD}) on pin $\overline{SD}$ sets the non-overlap time of the NWP2081T. The relationship between this resistor value and actual dead-time is listed in Figure 3.

It is essential to add a 10 nF to 100 nF decoupling capacitor across R_{SD} to ensure a noise immune dead-time system.

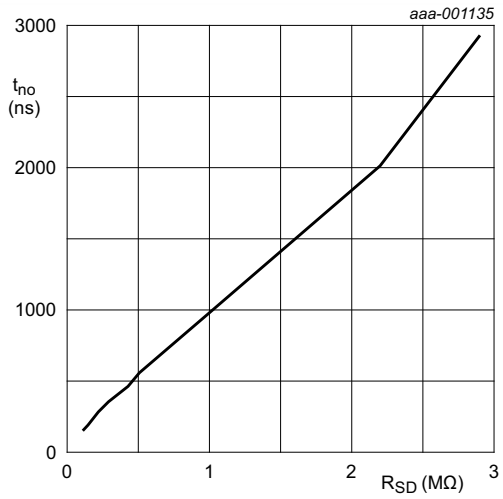

Fig 3. Non-overlap time versus $\overline{SD}$ resistor (R_{SD})

7.4 NWP2081T shutdown protection

When the voltage at pin $\overline{SD}$ is pulled below V_{IH}, the internal sink drivers of the pins GL and GH are immediately enabled to switch off the external power MOSFETs.

The shutdown comparator has a hysteresis of $V_{hys(SD)}$ to avoid multiple switching.

Preferably, pin $\overline{SD}$ is pulled low via a collector of a transistor (see Figure 4) to avoid loading of this pin (Influences the non-overlap time settings) at normal operation.

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	nominal		0	15.5	V
V_{FS}	voltage on pin FS			V_{SH}	V_{SH} + 15.5	V
V_{SH}	voltage on pin SH	source high-side MOSFET		−3	+600	V
		t < 1 μs		−14	+600	V
V_{CLK}	voltage on pin CLK	logic input for output drivers		0	15.5	V
$V_{i(SD)}$	input voltage on pin $\overline{SD}$	logic input for output drivers and analog input for non-overlap setting		0	15.5	V
SR	slew rate	on pin SH; repetitive		−6	+6	V/ns
T_j	junction temperature			−40	+150	°C
T_{amb}	ambient temperature			−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model:	[1]			
		pins FS, GH and SH		-	1	kV
		pins V_{DD}, $\overline{SD}$, CLK, and GL		-	2	kV
		charge device model:	[2]			
		all pins		-	500	V

[1] In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] In accordance with the Charged Device Model (CDM): equivalent to discharging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
SO8					
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	160	K/W

[1] In accordance with IEC 60747-1.

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10. Characteristics

Table 6. Characteristics

T_j = 25 °C; all voltages are measured with respect to SGND; V_{DD} = 12.8 V; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-voltage supply						
I_{leak}	leakage current	FS = GH = SH = 600 V	-	-	10	µA
Start-up state						
I_{VDD}	current on pin V_{DD}		420	520	620	µA
$V_{DD(start)}$	start supply voltage		9	10	11	V
$V_{DD(stop)}$	stop supply voltage		8	8.5	9	V
$V_{DD(hys)}$	hysteresis of supply voltage	start-to-stop	1	1.5	2	V
Pin CLK input						
V_{IH}	HIGH-level input voltage		2.7	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
$I_{I(CLK)}$	input current on pin CLK		-	0	1	µA
Pin $\overline{SD}$ input						
V_{IH}	HIGH-level input voltage	to activate shutdown	1.6	2.2	2.8	V
$V_{hys(SD)}$	hysteresis voltage on pin $\overline{SD}$		-	400	-	mV
t_{no}	non-overlap time	R_{SD} = 100 kΩ; typical minimum	-	140	-	ns
		R_{SD} = 3 MΩ; typical maximum	-	2.4	-	µs
Gate drivers						
$I_{O(source)}$	output source current	$V_{FS} = V_{VDD}$ = 12 V; V_{SH} = 0 V; $V_{GH} = V_{GL}$ = 8 V	-	200	-	mA
$I_{O(sink)}$	output sink current	$V_{FS} = V_{VDD}$ = 12 V; V_{SH} = 0 V; $V_{GH} = V_{GL}$ = 4 V	-	400	-	mA
$V_{d(bs)}$	bootstrap diode voltage	$I_{d(bs)}$ = 20 mA	-	2.3	-	V
V_{UVLO}	undervoltage lockout voltage	reset	3.6	4.2	4.8	V
I_{FS}	current on pin FS	$V_{FS} = V_{VDD}$ = 12 V; V_{SH} = 0 V	27	32	37	µA
f_{max}	maximum frequency		800	-	-	kHz

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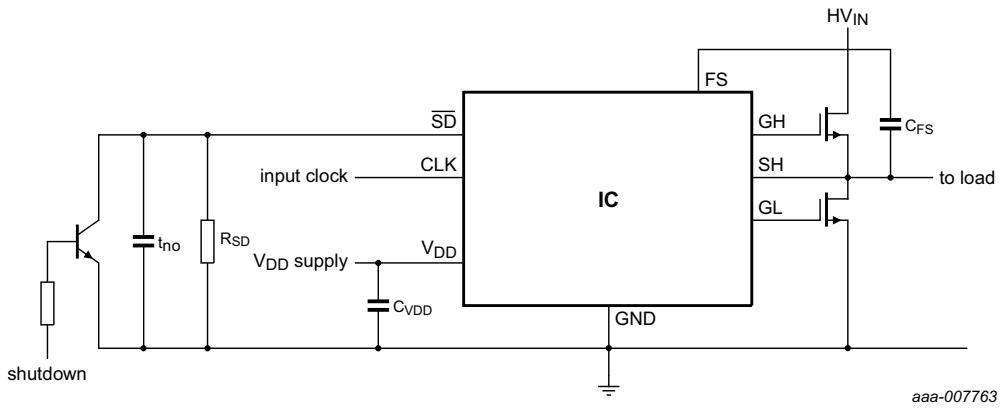
11. Application information



Remark: The capacitor connected to the $\overline{SD}$ pin ensures a noise immune dead-time.

Fig 4. Typical NWP2081T application

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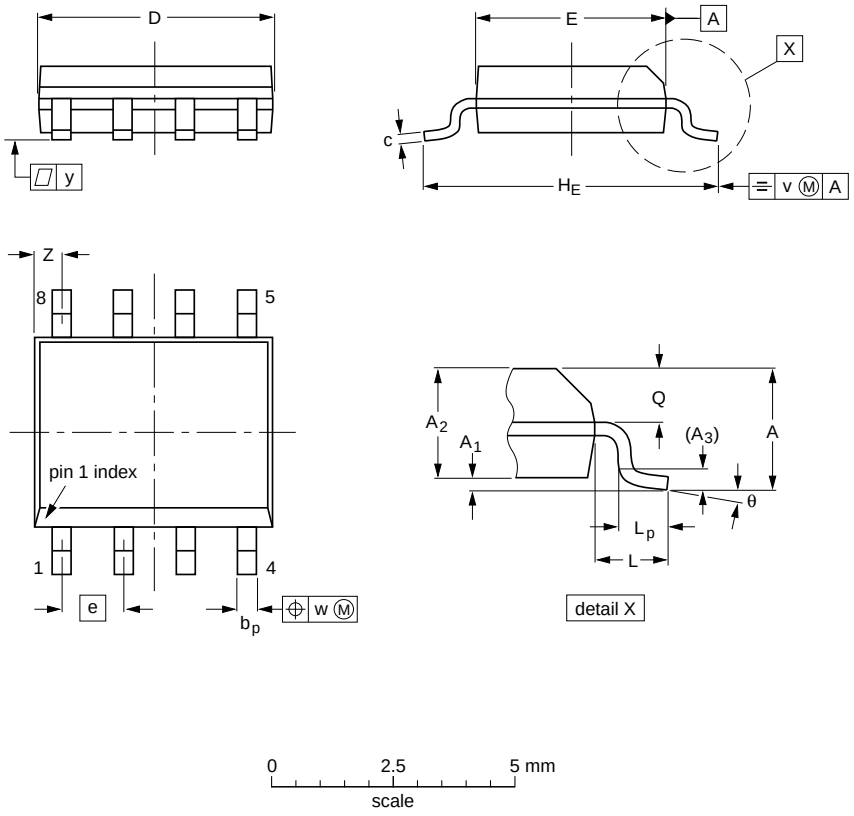
12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 5. Package outline SOT96-1 (SO8)

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13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NWP2081T v.1	20130903	Product data sheet	-	-

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14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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