



SamHop Microelectronics Corp.



STU/D419S

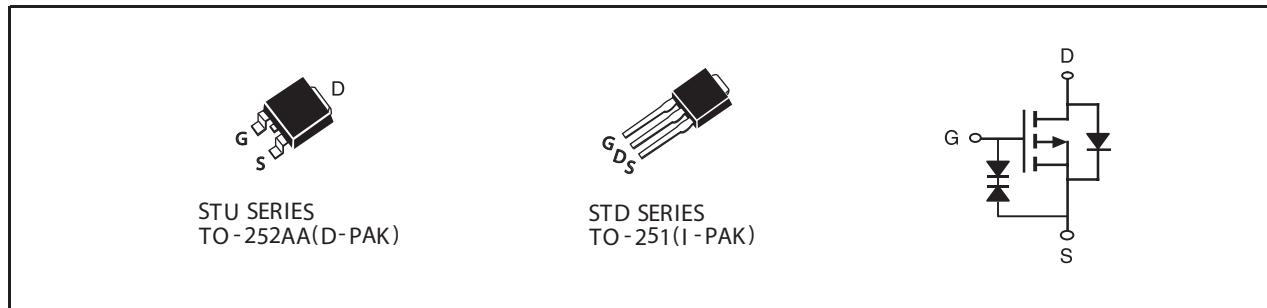
Ver 1.0

P-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
VDSS	ID	RDS(ON) (mΩ) Max
-40V	-58A	11.5 @ VGS=10V
		16 @ VGS=4.5V

FEATURES

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Limit	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous(Package limited)	$T_C=25^\circ\text{C}$	A
	-Continuous(Silicon limited)	$T_C=25^\circ\text{C}$	A
	-Continuous ^a	$T_A=25^\circ\text{C}$	A
I_{DM}	-Pulsed ^b	-175	A
E_{AS}	Single Pulse Avalanche Energy ^d	224	mJ
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	W
	Maximum Power Dissipation ^a	$T_A=25^\circ\text{C}$	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ^a	50	$^\circ\text{C/W}$

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ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-32V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±10	μA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.5	-3	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-20A		9.6	11.5	m ohm
		V _{GS} =-4.5V, I _D =-17A		12.5	16	m ohm
g _{FS}	Forward Transconductance	V _{DS} =-10V, I _D =-20A		9		S
DYNAMIC CHARACTERISTICS ^c						
C _{ISS}	Input Capacitance	V _{DS} =-20V, V _{GS} =0V f=1.0MHz		3550		pF
C _{OSS}	Output Capacitance			710		pF
C _{RSS}	Reverse Transfer Capacitance			420		pF
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =-20V I _D =-1.0A V _{GS} =-10V R _{GEN} =3.3 ohm		40		ns
t _r	Rise Time			70		ns
t _{D(OFF)}	Turn-Off Delay Time			345		ns
t _f	Fall Time			125		ns
Q _g	Total Gate Charge	V _{DS} =-20V, I _D =-20A, V _{GS} =-10V		87		nC
		V _{DS} =-20V, I _D =-20A, V _{GS} =-4.5V		42		nC
Q _{gs}	Gate-Source Charge	V _{DS} =-20V, I _D =-20A, V _{GS} =-10V		9		nC
Q _{gd}	Gate-Drain Charge			20		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Forward Current			-2.0		A
V _{SD}	Diode Forward Voltage ^b	V _{GS} =0V, I _S =-2.0A		-0.77	-1.3	V
Notes						
a. Surface Mounted on FR4 Board, t ≤ 10sec.						
b. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.						
c. Guaranteed by design, not subject to production testing.						
d. Starting T _J =25°C, L=1.25mH, V _{DD} = 30V .(See Figure13)						

Sep,15,2008

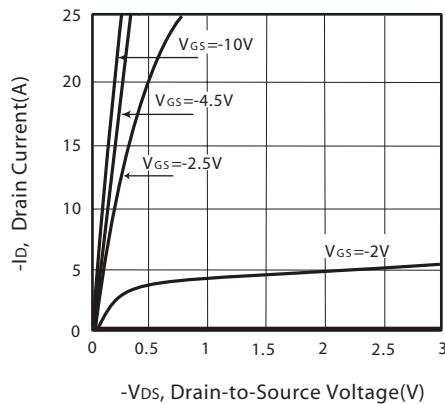


Figure 1. Output Characteristics

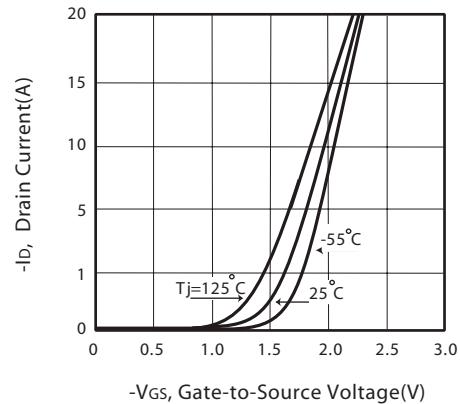


Figure 2. Transfer Characteristics

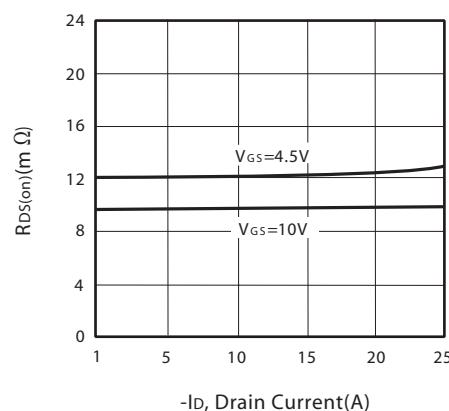


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

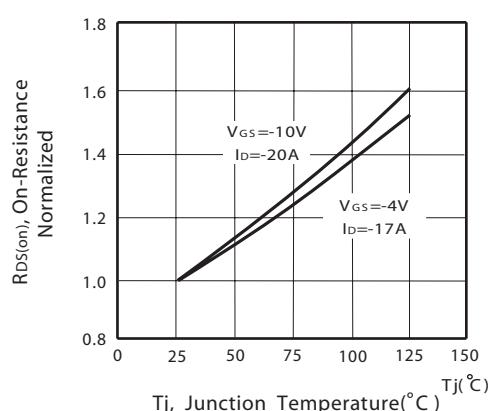


Figure 4. On-Resistance Variation with Drain Current and Temperature

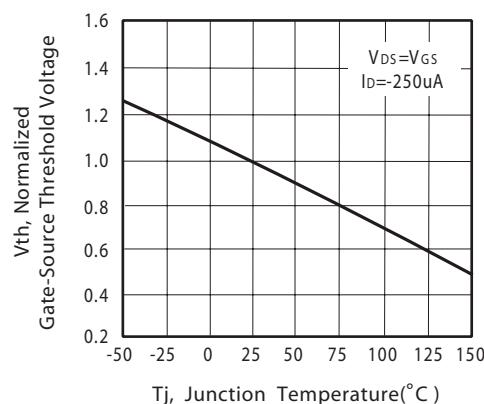


Figure 5. Gate Threshold Variation with Temperature

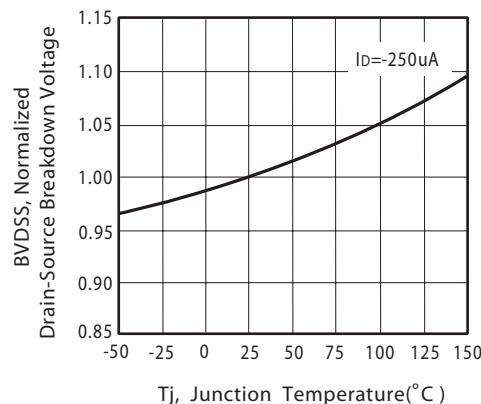
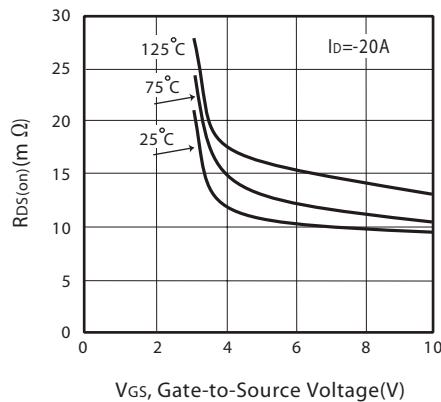
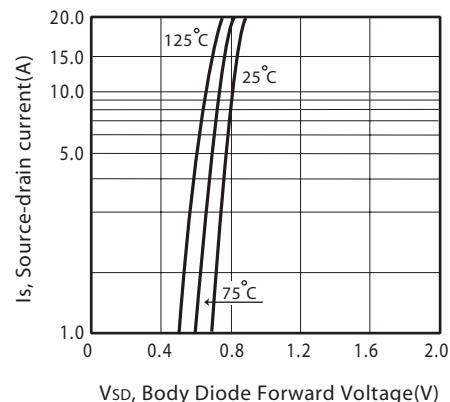


Figure 6. Breakdown Voltage Variation with Temperature



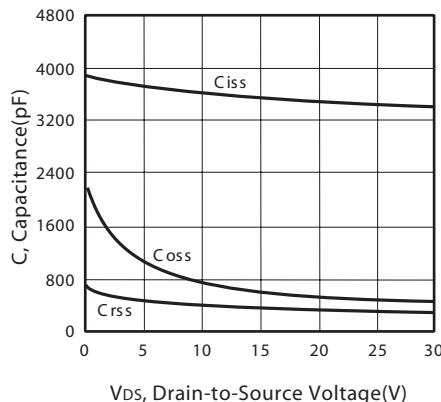
V_{GS}, Gate-to-Source Voltage(V)

Figure 7. On-Resistance vs. Gate-Source Voltage



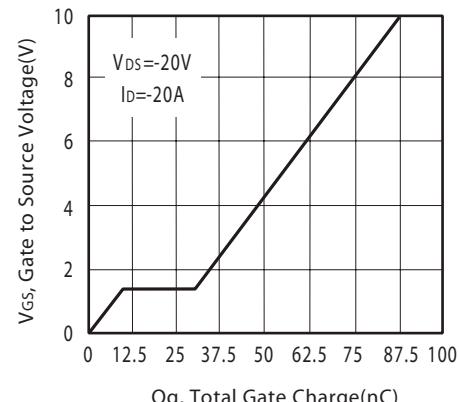
V_{SD}, Body Diode Forward Voltage(V)

Figure 8. Body Diode Forward Voltage Variation with Source Current



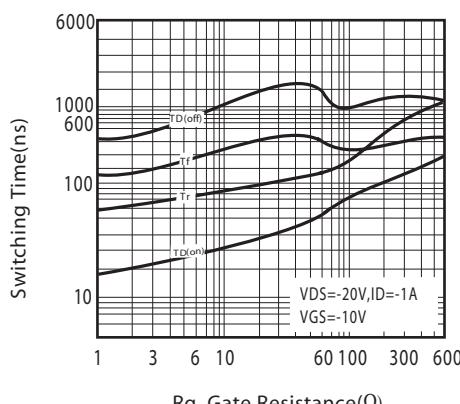
V_{DS}, Drain-to-Source Voltage(V)

Figure 9. Capacitance



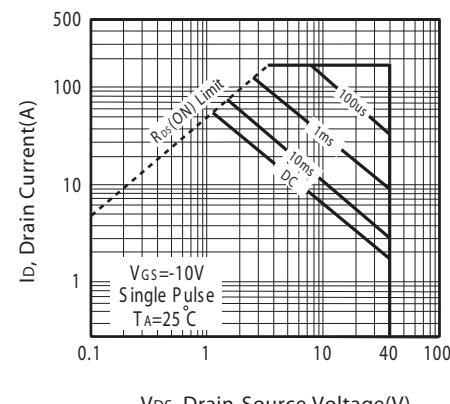
Q_g, Total Gate Charge(nC)

Figure 10. Gate Charge



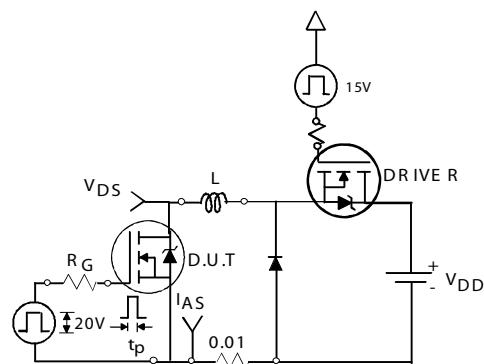
R_g, Gate Resistance(Ω)

Figure 11. switching characteristics



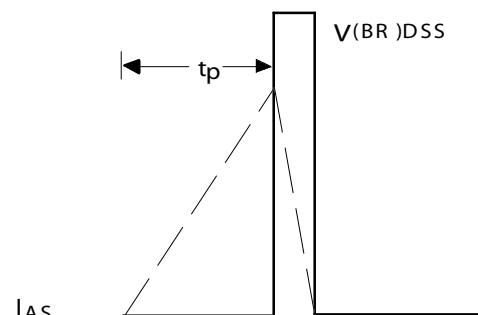
V_{DS}, Drain-Source Voltage(V)

Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

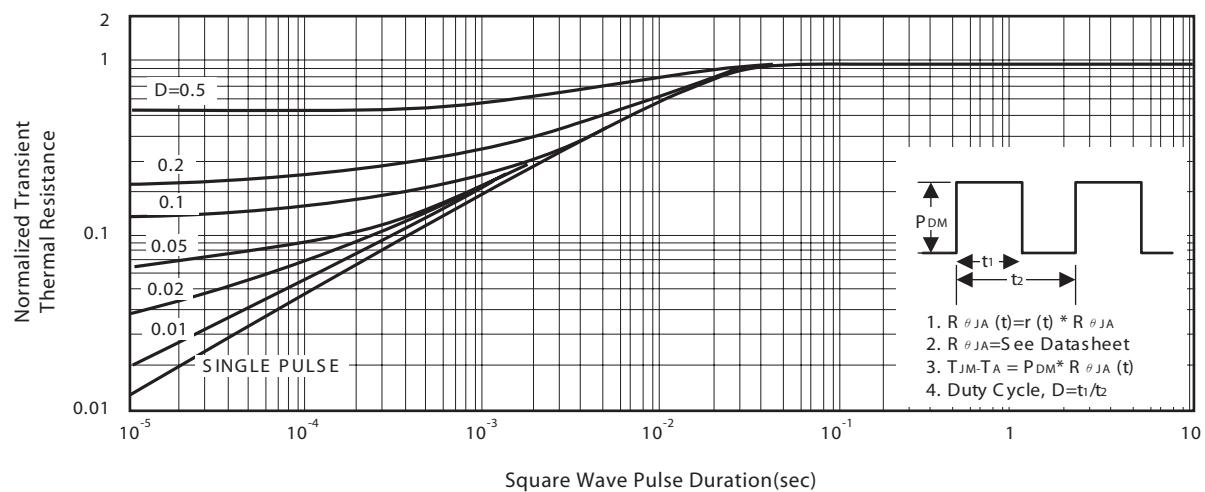
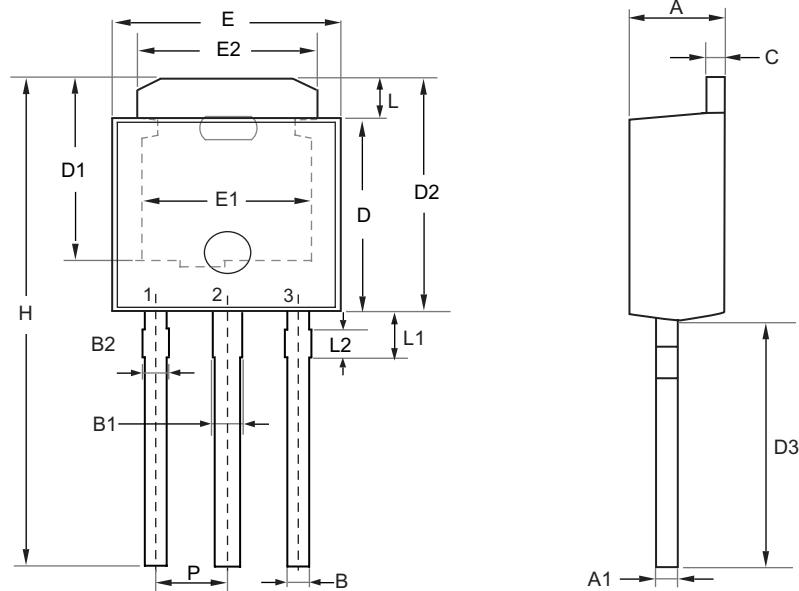


Figure 14. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

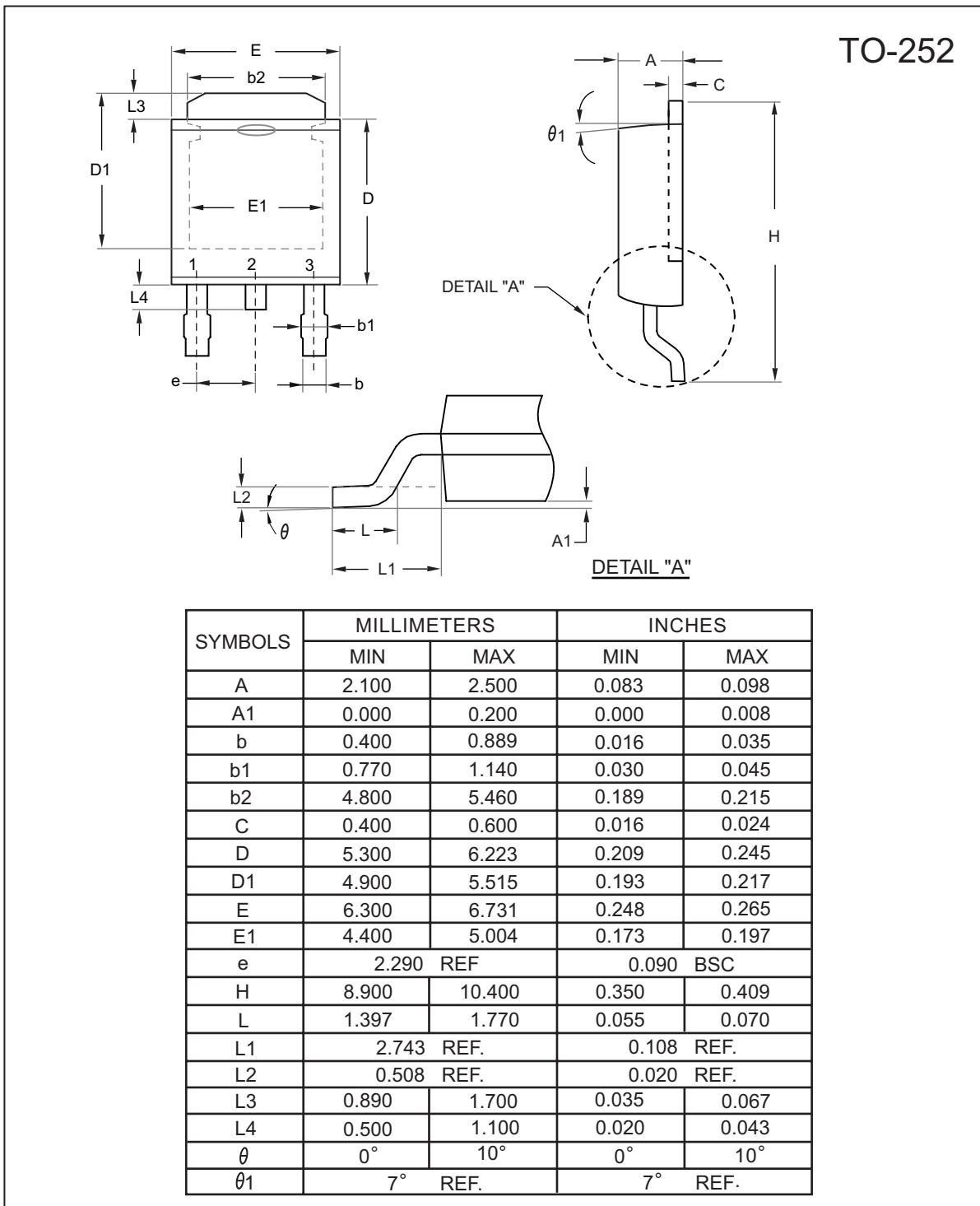
TO-251



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.100	2.500	0.083	0.098
A1	0.350	0.650	0.014	0.026
B	0.400	0.800	0.016	0.031
B1	0.650	1.050	0.026	0.041
B2	0.500	0.900	0.020	0.035
C	0.400	0.600	0.016	0.024
D	5.300	5.700	0.209	0.224
D1	4.900	5.300	0.193	0.209
D2	6.700	7.300	0.264	0.287
D3	7.000	8.000	0.276	0.315
H	13.700	15.300	0.539	0.602
E	6.300	6.700	0.248	0.264
E1	4.600	4.900	0.181	0.193
E2	4.800	5.200	0.189	0.205
L	1.300	1.700	0.051	0.067
L1	1.400	1.800	0.055	0.071
L2	0.500	0.900	0.020	0.035
P	2.300 BSC		0.091 BSC	

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