AN.No.G648D-992E

LIQUID CRYSTAL DISPLAY MODULE

G 6 4 8 D

USER MANUAL

Seiko Instruments Inc.

NOTICE

This manual describes the technical information, the function, and the operation of the G648D Liquid Crystal Display Module of Seiko Instruments Inc. Please read this manual carefully to familiarize yourself with the functions and to make best use of them.
The descriptions here are subject to change without notice.

Revision Record

Edition	Revision	Date
1	Original	November 1988
2		March 1989
3	Optical characteristics, recommended $V_{opr.}$	September 1989

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1. SPECIFICATIONS

1.1 General

The G648D is a thin liquid crystal display (LCD) module that consists of a full dot-matrix LCD panel and CMOS LSIs. The panel features a wide viewing angle and high contrast. The full dot-matrix structure allows both graphics and character display. In addition, the display is clear and stable, with no image warping or position skew, because the display position is specified by the intersection of transparent electrodes in a matrix.

1.2 Features

- Full dot-matrix structure with 640 dots×200 dots
- 1 / 200 duty
- Four-bit parallel data input
- Two power supplies : V_{DD}= 5 V, V_{LC}= -24 V (for driving liquid crystal)
- Weight : 450 g

1.3 Option Specifications

Model	LCD	Dot color*	Background color*	Viewing angle	
G648D00B000	STN type** (yellow green)	Black	Yellow green	6 o'clock	Reflective
G648D00B100				12 o'clock	Reflective
G648D21B000				6 o'clock	Transflective with EL backlighting (white)****
G648D00C000	STN type (blue green)	Black	Green	6 o'clock	Reflective
G648D25B000	STN type (blue)	White	Blue	6 o'clock	Transmissive, with EL backlighting (white)****, negative type***

* The LCD colors are affected by temperature, so the colors at low or high temperature differs slightly from those in the above table.

** STN (Super New TN) LCD
The STN has even better display than the conventional new TN because of its increased twist angles. It has the following features :
① Even clearer display
② Wider visibility and high contrast
③ Easy to see in vertical directions

*** G648D25B000 is a negative type; when the display data is 1, the dots are white. When the display data is 0, the dots are blue. To change to positive display, invert the display data and input it into the module.

**** For the EL backlighting data and specifications, refer to *EL Backlightings for LCD Modules Technical Data*.

1.4 Absolute Maximum Ratings

Vss = 0 V

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply voltage	V_{DD}		− 0.3	6.0	V
	V_{LC}		V_{DD} − 30.0	V_{DD}	V
	V_O	$V_O \geqq V_{LC}$	V_{DD} − 30.0	V_{DD}	V
Input voltage	V_{IN}		− 0.3	V_{DD} + 0.3	V
Operating temperature	T_{opr}		0	+ 50	°C
Storage temperature	T_{stg}		− 20	+ 60	°C

1.5 Electrical Characteristics

Vss = 0 V, Ta = 0°C ~ 50°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	V_{DD} = 5 V ± 5%	− 24.5	− 24.0	− 23.5	V
		V_O	V_{DD} = 5 V ± 5%, $V_O \geqq V_{LC}$	− 23.0	—	—	V
Input voltage	High	V_{IH}	V_{DD} = 5 V ± 5%	0.8 V_{DD}	—	V_{DD}	V
	Low	V_{IL}	V_{DD} = 5 V ± 5%	0	—	0.2 V_{DD}	V
Current consumption*		I_{DD}	V_{DD} = 5.0 V, V_{LC} = − 24.0 V, V_O = − 17.5 V	—	11	25	mA
		I_{LC}		—	9	20	mA
Frame frequency		f_{FRM}	V_{DD} = 5 V ± 5%	65	70	75	Hz

* STN -type (Yellow green , blue)

1.6 Optical Characteristics

1.6.1 STN type (Yellow green, reflective type)

1 / 200 duty, 1 / 15 bias, Vopr = 22.5 V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	C ≧ 2.0, ∅ = 0°	50°	—	—	Notes 1 & 2
		C ≧ 2.0, ∅ = 90°	60°	—	—	
Contrast	C	θ = 5°, ∅ = 0°	3	5	—	Note 3
Response time (rise)	t_{on}	θ = 5°, ∅ = 0°	—	180 ms	—	Note 4
Response time (fall)	t_{off}	θ = 5°, ∅ = 0°	—	350 ms	—	Note 4

1.6.2 STN type (Blue, transmissive type)

1 / 200 duty, 1 / 15 bias, Vopr = 22.5 V, Ta = 25°C

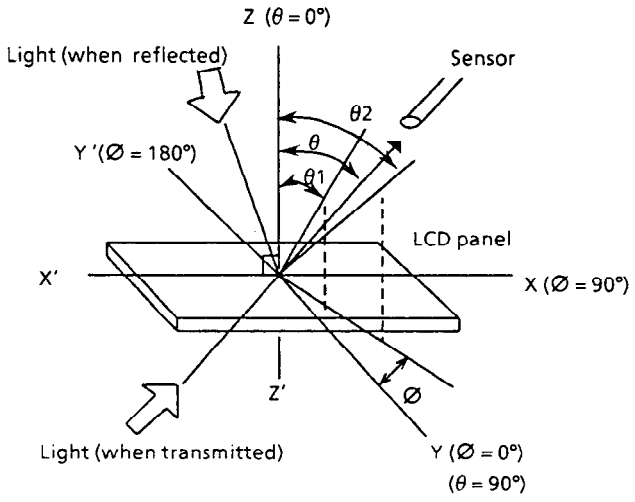
Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	C ≧ 2.0, ∅ = 0°	25°	—	—	Notes 1 & 2
		C ≧ 2.0, ∅ = 90°	40°	—	—	
Contrast	C	θ = 5°, ∅ = 0°	2	3	—	Note 3
Response time (rise)	t_{on}	θ = 5°, ∅ = 0°	—	180 ms	—	Note 4
Response time (fall)	t_{off}	θ = 5°, ∅ = 0°	—	350 ms	—	Note 4

1.6.3 STN type (Blue green, reflective type)

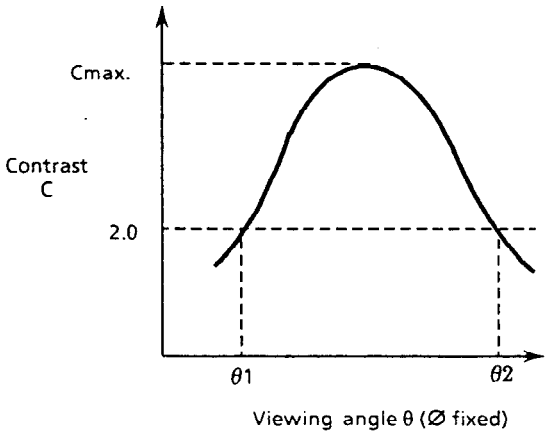
1 / 200 duty, 1 / 15 bias, Vopr = 24.5 V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	C ≧ 2.0, Ø = 0°	50°	–	–	Notes 1 & 2
		C ≧ 2.0, Ø = 90°	60°	–	–	
Contrast	C	θ = 5°, Ø = 0°	3	4	–	Note 3
Response time (rise)	t_{on}	θ = 5°, Ø = 0°	–	220 ms	–	Note 4
Response time (fall)	t_{off}	θ = 5°, Ø = 0°	–	360 ms	–	Note 4

Note 1 : Definition of angles θ and Ø



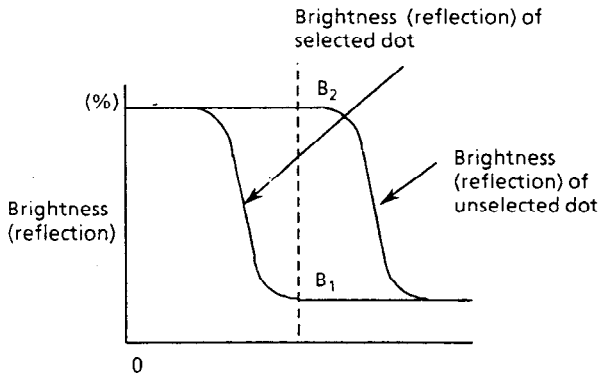
Note 2 : Definition of viewing angles θ1 and θ2



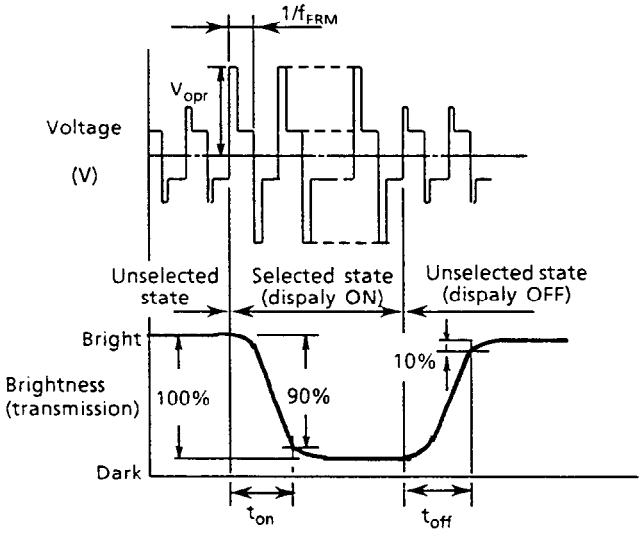
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. above are not always the same.

Note 3 : Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot } (B_2)}{\text{Brightness (reflection) of selected dot } (B_1)}$$



Note 4 : Definition of response time



Note : Measured with a transmissive LCD panel which is displayed 1 cm²

V_{opr} : Operating voltage f_{FRM} : Frame frequency
t_{on} : Response time (rise) t_{off} : Response time (fall)

1.7 Dimensions

Unit : mm/inch
General tolerance : ± 0.5 mm

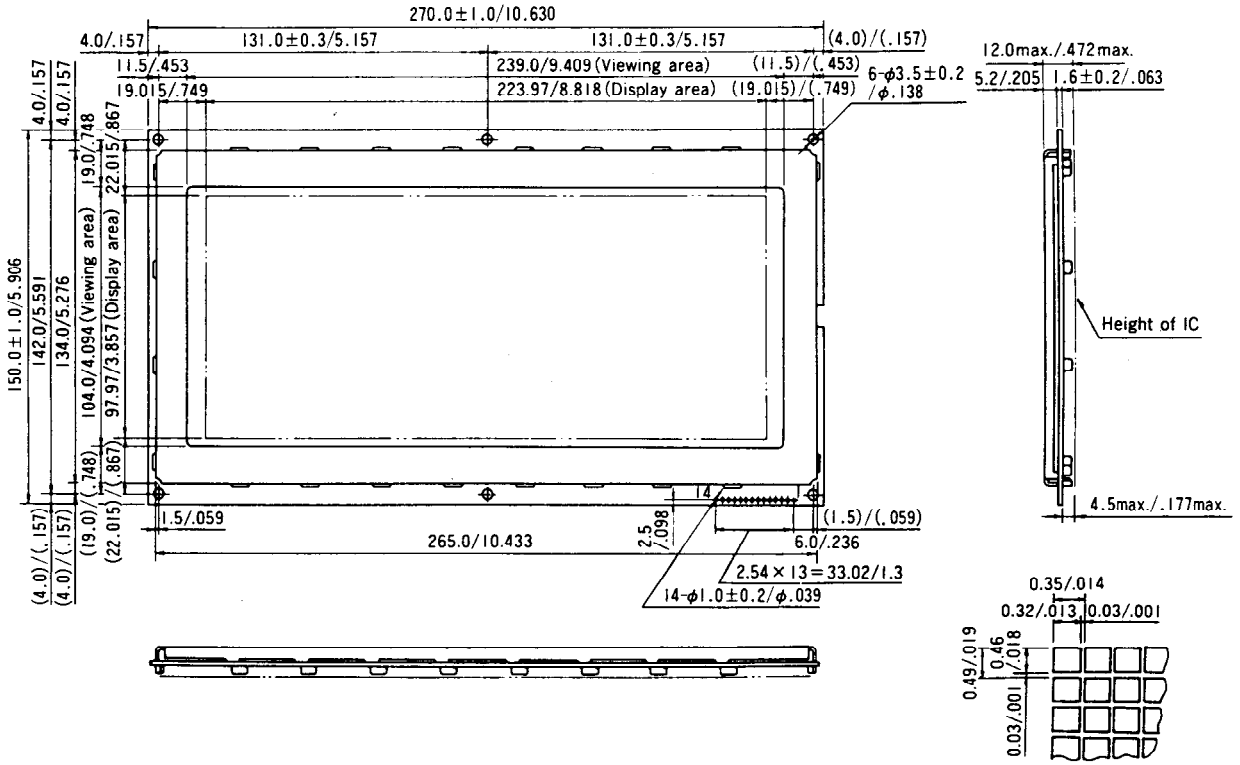


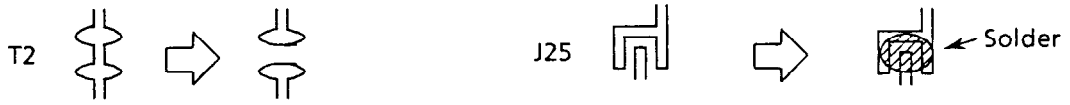
Figure 1 Dimensions

[I/O Terminal Functions]

No.	Symbol	Function
1	D_3	Display data input
2	D_2	Display data input
3	FLM	One-frame timing signal
4	M	Liquid crystal AC drive control signal
5	CL1	One-common-line timing signal
6	CL2	Display data shift clock
7	D_1	Display data input

No.	Symbol	Function
8	D_0	Display data input
9	V_{DD}	Power supply voltage (1) : + 5 V
10	V_{SS}	GND : 0 V
11	V_{LC}	Power supply voltage (2) : − 24 V
12	V_O	Liquid crystal drive voltage adjustment terminal
13	INH	Display ON/OFF control terminal*
14	F_{GND}	Frame ground**

* The INH terminal is normally set to NC. To use this terminal, cut off T2 of module circuit substrate, and unite J25.
The display will then be on when INH is H, and off when INH is L.



** The F_{GND} terminal is connected to the metal frame of the module.
Use this terminal to ground the frame.

2. CIRCUIT STRUCTURE

2.1 Liquid Crystal Driving Circuit

The drive waveform of the LCD panel is shown in Figure 2 on the next page. Since DC voltage will damage the liquid crystal, an AC voltage is applied between the two frames. The signal controlling this is the liquid crystal AC drive control signal (M).

The display quality of some LCD panels may be improved by increasing the frequency of liquid crystal AC drive waveform. For the G648D, in addition to the liquid crystal driving circuit that uses external signals M as AC drive control signals, a liquid crystal driving circuit is provided that includes a circuit that generates AC drive control signals (M') of higher frequency than M so that the best display quality can be obtained. M signals need not be input to the liquid crystal driving circuit that uses M' signals. However, interface circuit that can input M signals should be designed to use both types of liquid crystal driving circuit.

The frame frequency is normally set to about 70 ± 5 Hz to prevent screen flicker.

The G648D has a 1/200 duty cycle, and the common electrodes are selected within a frame by time division from electrode 1 to electrode 200. This is called line sequential scanning. The voltage level of the segment electrodes determines whether the dots at the intersection of the segment electrodes are selected or not, when the common electrode is selected. As shown in Table 1, there are six drive waveform voltage levels, V_a to V_f. The voltage level is determined by the bias value. The voltage between the segment and common electrodes is thus applied to the liquid crystal. The selection waveform for SEG_0-COM_0 and the non-selection waveform for SEG_1-COM_1 are shown in Figure 2. The size of the effective voltage of the waveform determines whether the liquid crystal under the selected dots is in the selection or non-selection state.

Table 1

V_a	Common and segment selection level
V_b	Common non-selection level
V_c	Segment non-selection level
V_d	Segment non-selection level
V_e	Common non-selection level
V_f	Common and segment selection level

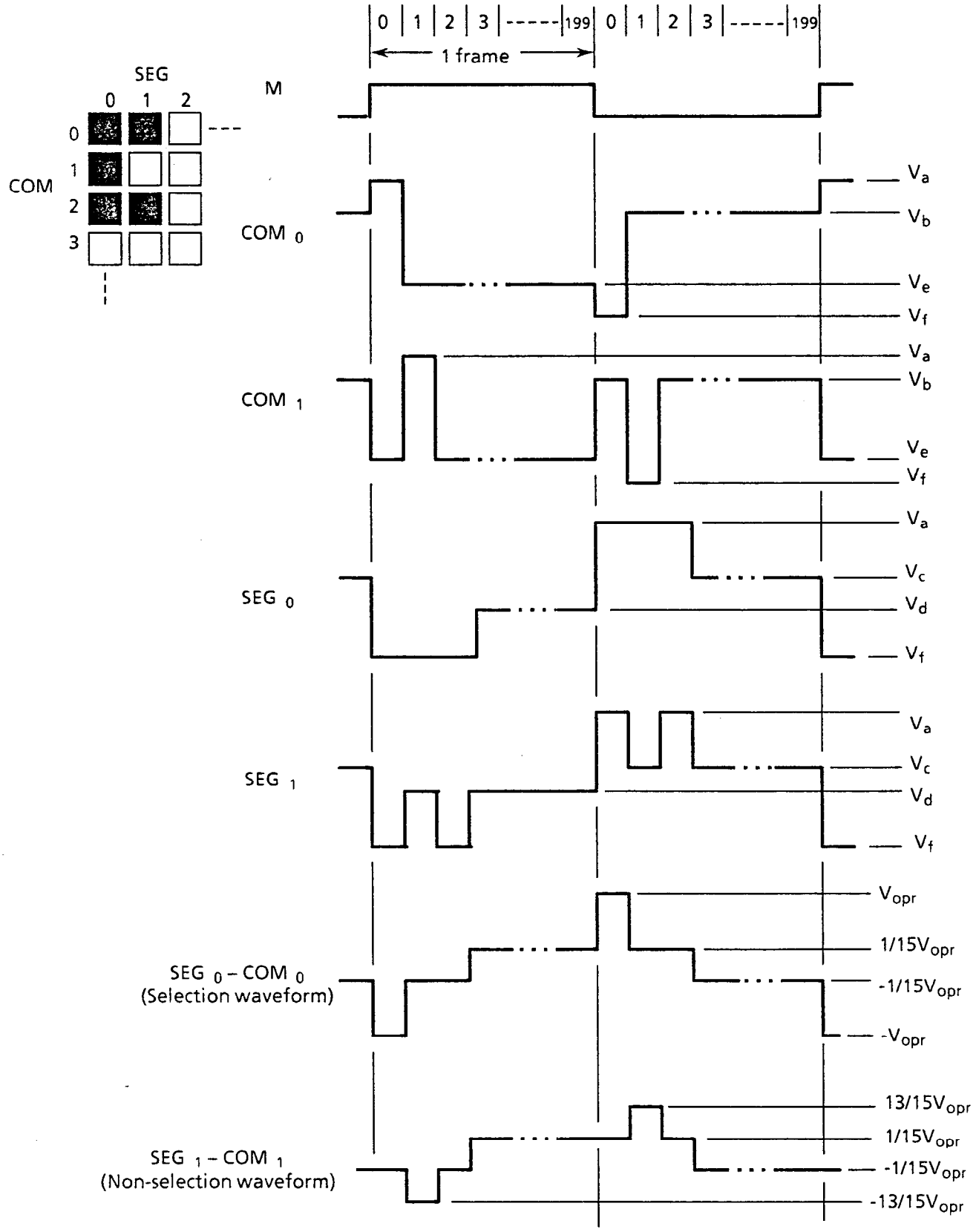


Figure 2 Drive waveform

2.2 Circuit Structure

The G648D consists of common drivers, segment drivers, a bias voltage generation circuit, a M' generation circuit and a V_{opr} control circuit. Figure 3 shows the block diagram.

In the liquid crystal driving circuit where the M' generation circuit is not built in, CL1 and M are directly input to the segment driver and common driver instead of CL' and M'.

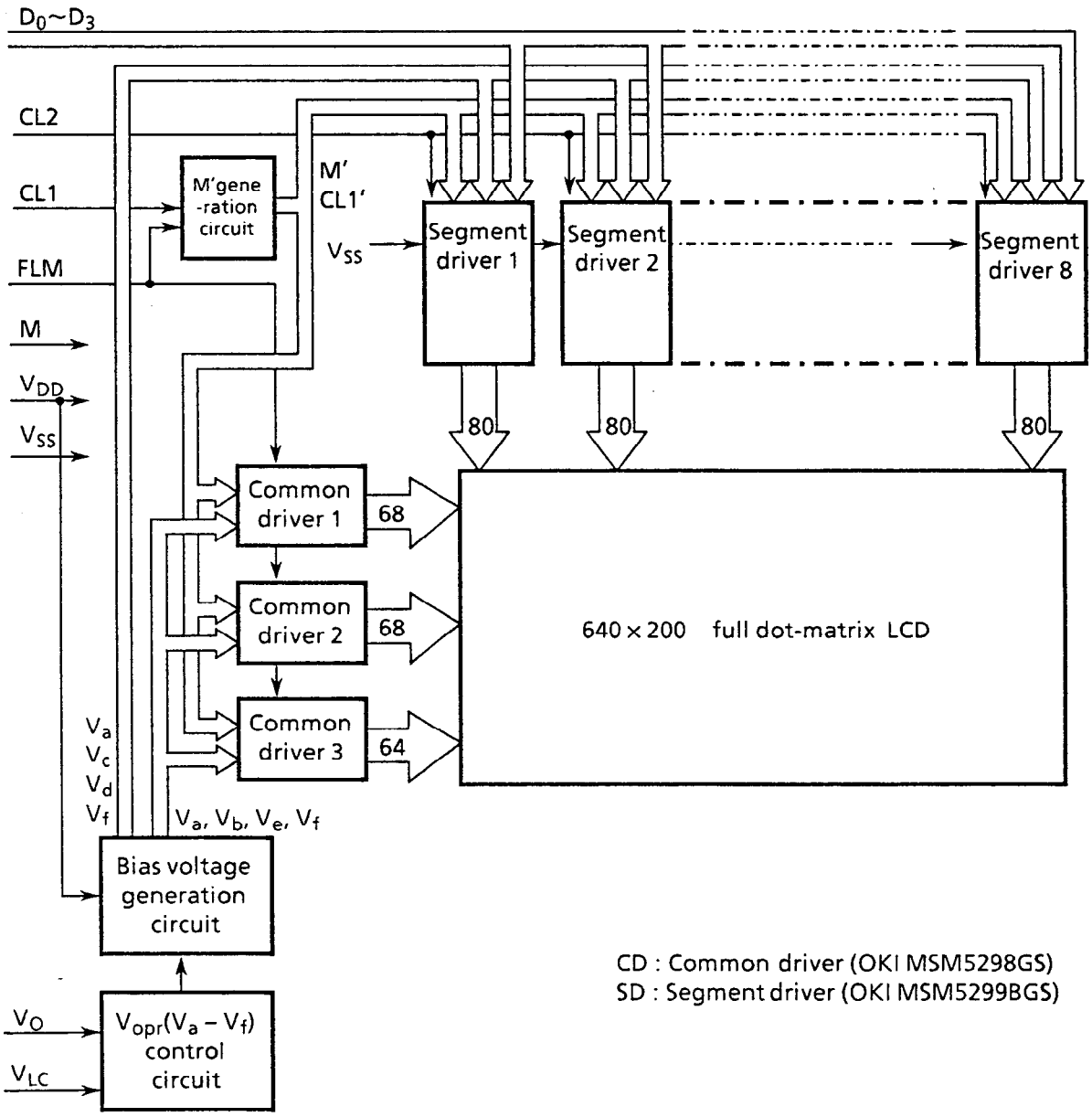


Figure 3 Block diagram

(1) Common driver (OKI MSM5298GS)

A common driver (CD) is a CMOS IC with 68 drive outputs. The G648D has three CDs, whose internal registers are connected each other. They operate as follows. Input one-frame timing signal (FLM) is taken into the internal shift register by the falling edge trigger of the one-common-line timing signal (CL1), and sequentially shifted. After 200-CL1 input, the next FLM is input and the same operation is repeated. As shown in Table 2, the common output is selected according to the shift register contents and the liquid crystal AC drive control signal (M) in the drive circuit, and the common drive waveform is formed.

Table 2

Shift register content	M	COM output
H	H	V_a
	L	V_f
L	H	V_e
	L	V_b

(2) Segment driver (OKI MSM5299BGS)

A segment driver (SD) is a CMOS IC with 80 drive outputs. It operates as follows. Input four-bit data is sequentially taken into the internal register by the falling edge trigger of the display data shift clock (CL2). SD has a chip enable function. After 80 bits of data are taken into SD1, the next data is automatically taken into SD2. G648D has eight SDs and 640 bits of data can be taken. The display data taken into internal register are latched by the falling edge trigger of CL1. As shown in the Table 3, the segment output is selected according to the display data and M in the drive circuit, and the segment drive waveform is formed.

Table 3

Display data	M	SEG output
H	H	V_f
	L	V_a
L	H	V_d
	L	V_c

The relationship between the display data and display screen is shown below..

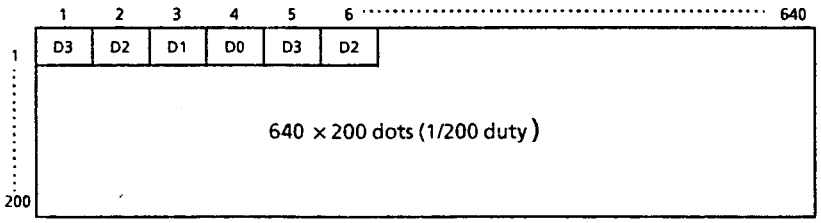


Figure 4

(3) V_{opr} control circuit

Display screen contrast and viewing angle are affected by changes in the liquid crystal operating voltage (V_{opr}). As shown in Figure 5, external V_{LC} is supplied to the operational amplifier and V_{opr} (V_a to V_f) applied to the LCD panel is generated.

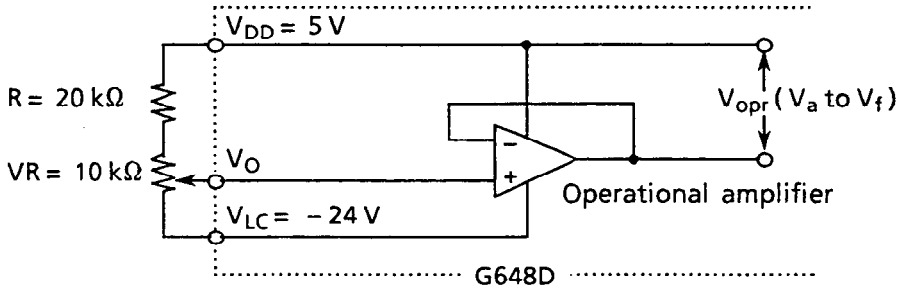


Figure 5

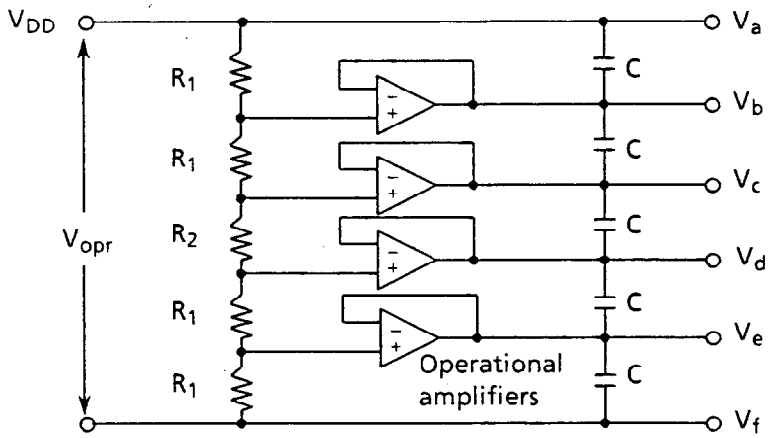
Also, display screen contrast and viewing angle are influenced by the ambient temperature. The recommended V_{opr} level at different temperatures is as follows.

Temperature (°C)		0	25	50
V_{opr} (V)*	STN (Yellow green) STN (Blue)	23.5	22.5	20.5
	STN (Blue green)	25.0	24.5	23.5

* $V_{opr} \approx V_{DD} - V_O$

(4) Bias voltage generation circuit

Six levels of voltage, V_a to V_f, are applied to the common and segment drivers. The voltage is generated through operational amplifier by resistance-division from liquid crystal operating voltage (V_{opr}). Here, an operational amplifier is used as a voltage follower.



1 / 15 bias : $R_2 = (15-4)R_1 = 11\,R_1$

Figure 6 Bias voltage generation circuit

(5) M' generation circuit

As Figure 7 shows, the M' generation circuit takes Ex-OR from a common line timing signal (CL1) on which A time division is performed and a frame timing signal (FLM) on which B time division is performed, and outputs liquid crystal AC drive control signal M'. Values A and B are set according to the LCD panel so that the best display quality can be obtained and the drive voltage can be alternated.

CL1' is the buffer output of CL1.

There are two types of G648D liquid crystal driving circuit: the type that includes the M' generation circuit and the type that does not (it uses external input signals M as liquid crystal AC drive control signals).

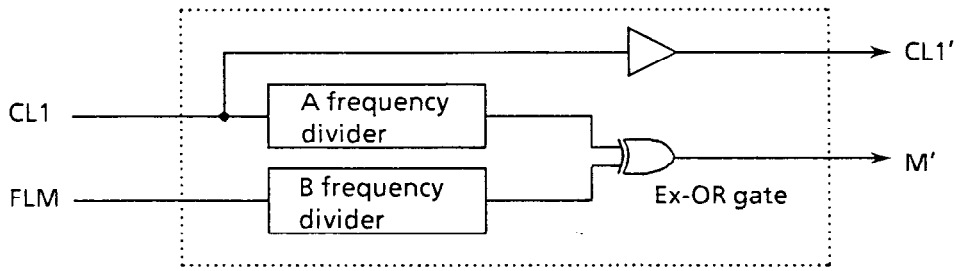


Figure 7 M' generation circuit

2.3 Timing Characteristics

2.3.1 Power ON/OFF and Signal Input Timing

Power ON/OFF and signal input should be performed according to the timing shown in the figure below in order not to damage the LCD driving circuit and the LCD panel.

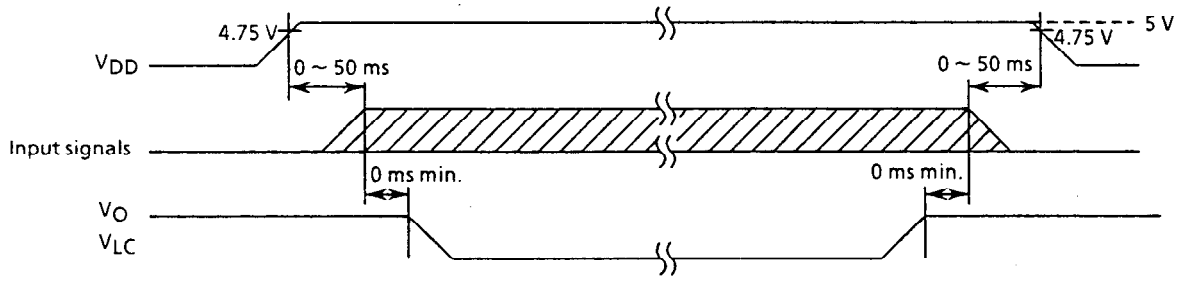


Figure 8 Power ON/OFF and signal input timing

2.3.2 Timing Characteristics

T_a = 0°C to 50°C, V_{DD} = 5.0 V ± 5%

Item	Symbol	Min.	Max.	Unit
CL1 period	tccl1	1000	—	ns
CL1 high pulse width	twcl1h	125	—	ns
CL1 low pulse width	twcl1l	—	—	ns
Data setup time 1	tds1	100	—	ns
Data hold time 1	tdh1	100	—	ns
Allowable M delay time	tdm	—	—	ns
Input signal rise time	t_r	—	50	ns
Input signal fall time	t_f	—	50	ns
CL2 period	tccl2	334	—	ns
CL2 high pulse width	twcl2h	125	—	ns
CL2 low pulse width	twcl2l	125	—	ns
Data setup time 2	tds2	100	—	ns
Data hold time 2	tdh2	100	—	ns
CL2 rise to CL1 rise	tld	63	—	ns
CL2 fall to CL1 fall	tsl	125	—	ns
CL1 rise to CL2 rise	tls	125	—	ns
CL1 fall to CL2 fall	tlh	63	—	ns

Timing chart 1 Timing of signal input into common driver

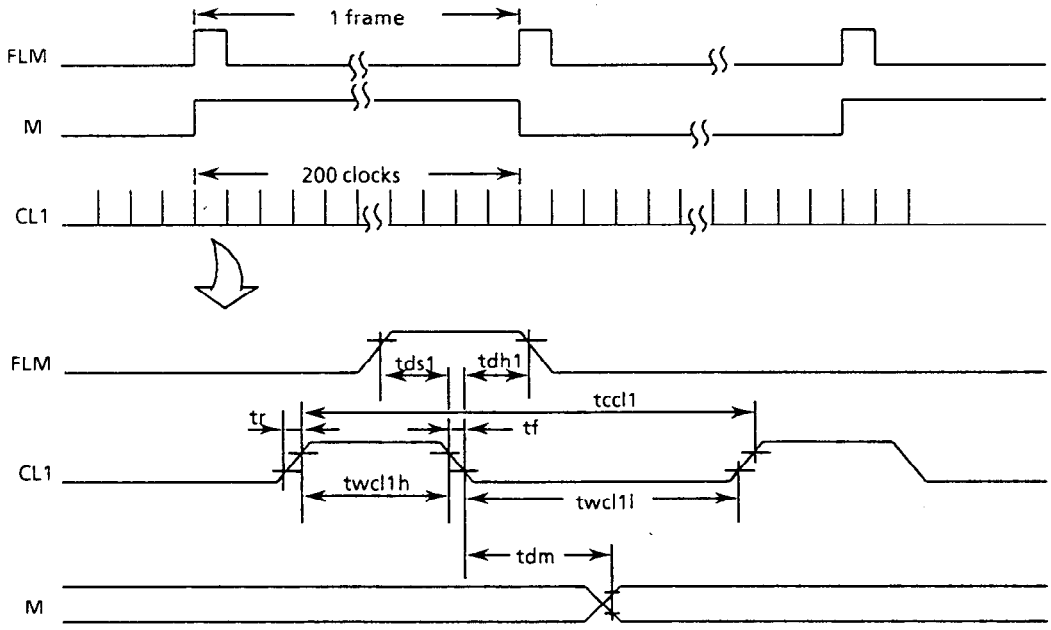


Figure 9

Timing chart 2 Timing of signal input into segment driver

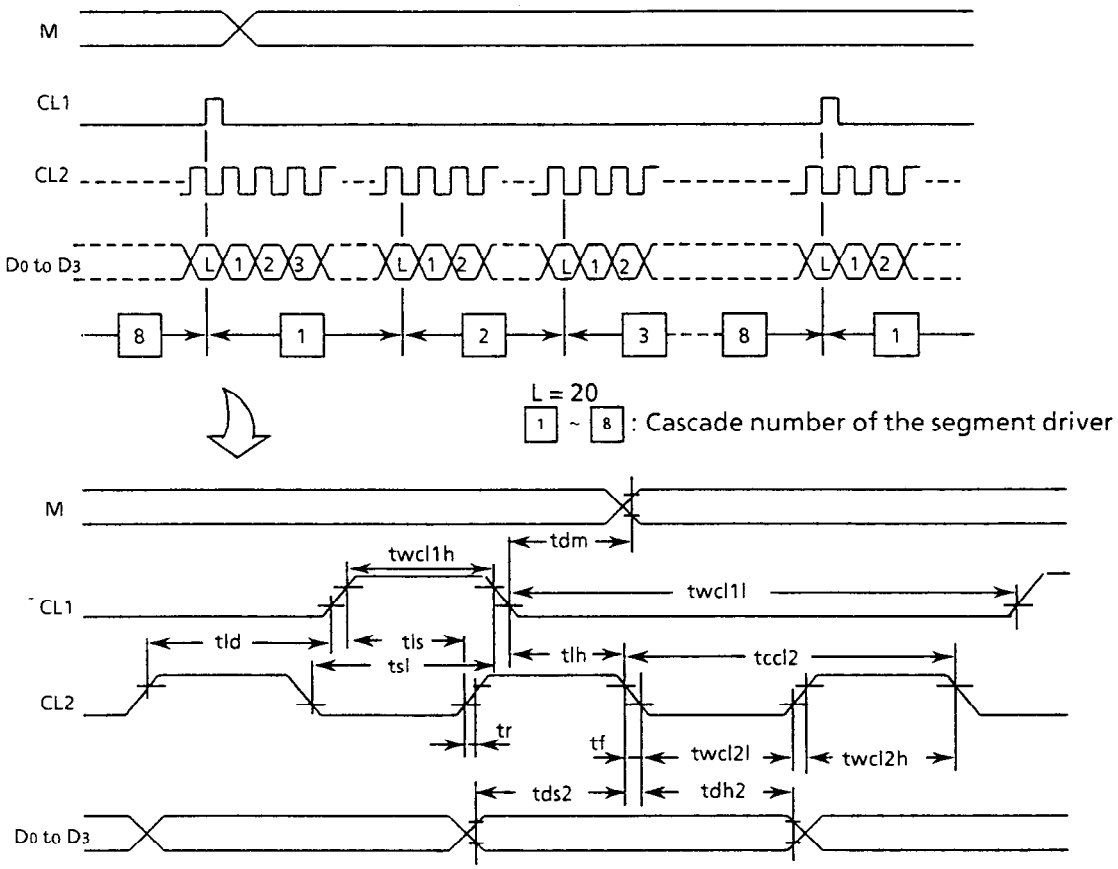


Figure 10

2.4 Interface Circuit

2.4.1 Interface with MPU signal

The G648D is controlled by the MPU circuit, whose interface is easily set up when the LCD controller is used. The LCD controller has basic functions such as receiving information related to the display from the MPU circuit, and sending display timing signals and display data to the LCD module, and other functions such as cursor display.

The G648D must use LCD controllers conforming to the following conditions.

- For a full dot-matrix LCD module
- Where data is transferred to the LCD module in four-bit parallel
- Where G648D display screen has 1/200 duty

The following section gives examples of interfaces using the OKI MSM6255GSK, SEIKO EPSON SED1330FBA, HITACHI HD64646FS and YAMAHA V6366B controllers.

(1) OKI MSM6255GSK

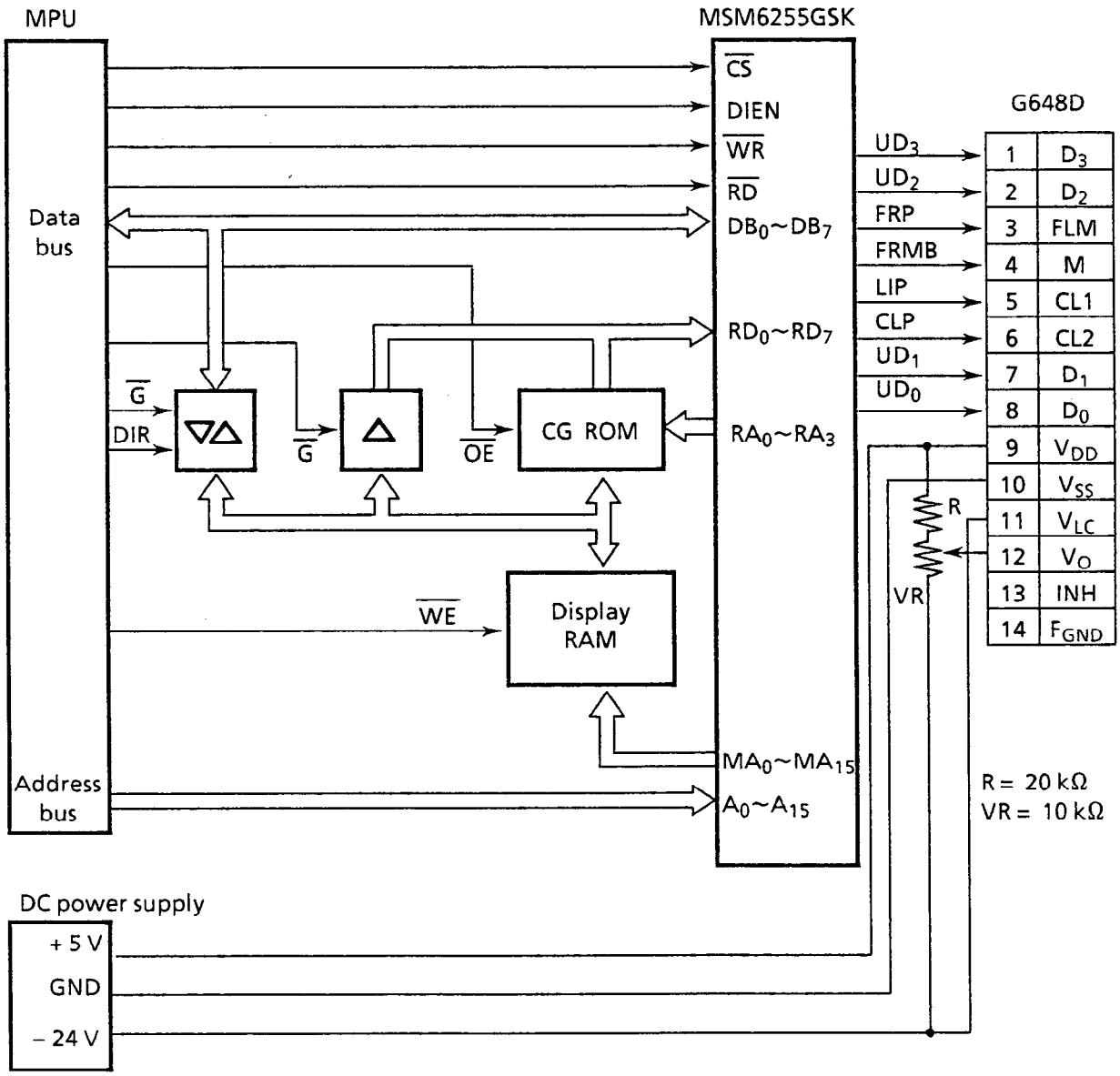


Figure 11 Interface circuit with MSM6255GSK

[Features of the MSM6255GSK]

- Interface with 80-series MPU possible
- Cursor

  ON/OFF; blinking speed, form, and position are programmable
- Scrolling and paging
- CMOS process
- 5-V single power supply

(2) SEIKO EPSON SED1330FBA

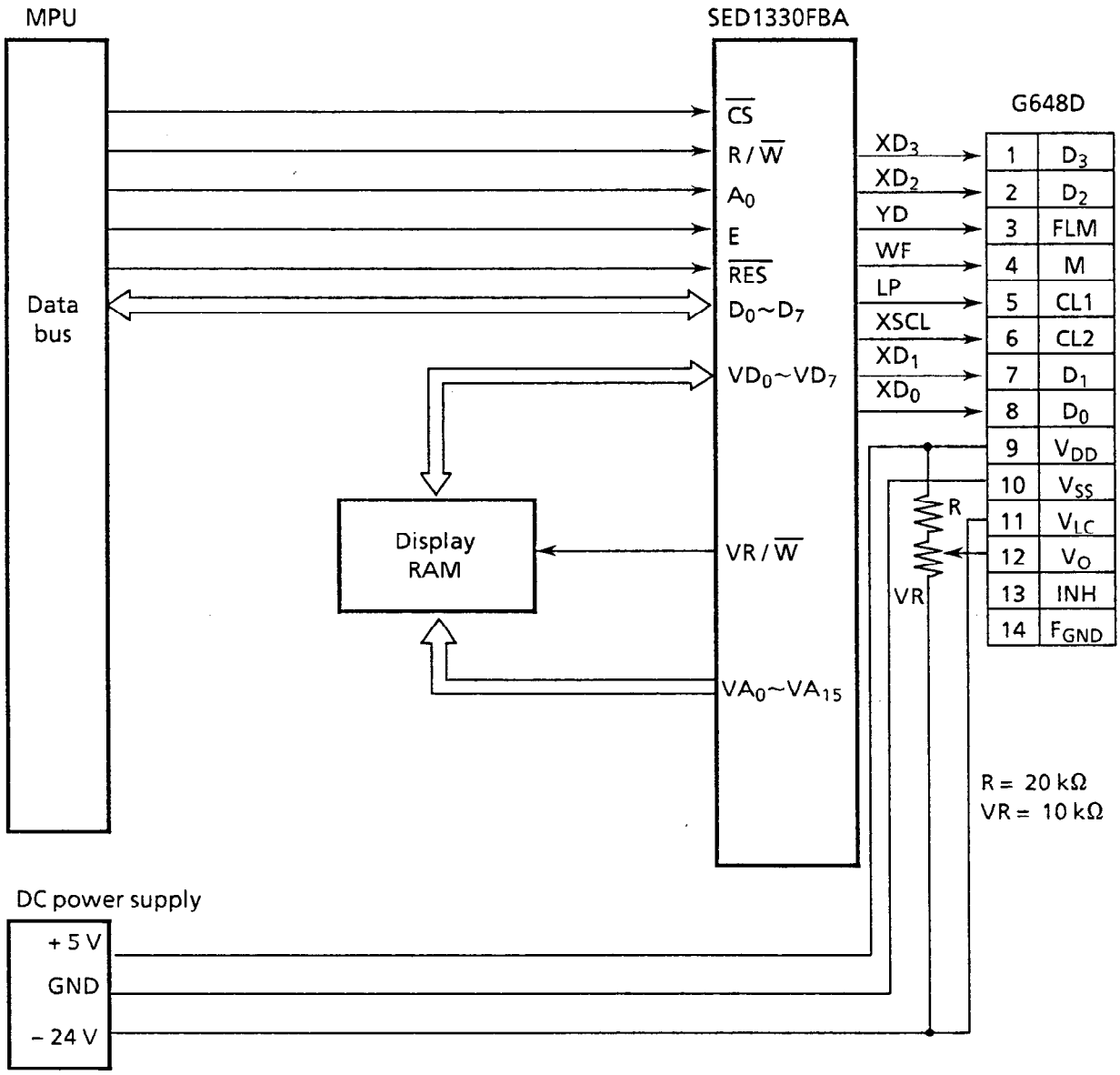


Figure 12 Interface circuit with SED1330FBA

[Features of the SED1330FBA]

- Interface with 80-series or 68-series MPU possible
- Built-in character generator ROM : 160 kinds
- External character generator
  - CG RAM : (8×16 dot-matrix)×64 kinds
  - CG ROM : (8×16 dot-matrix)×256 kinds
- Layered mode : AND, OR, XOR, "preferred" OR
- CMOS process
- Scrolling (vertical and horizontal)
- 5-V single power supply

(3) HITACHI HD64646FS

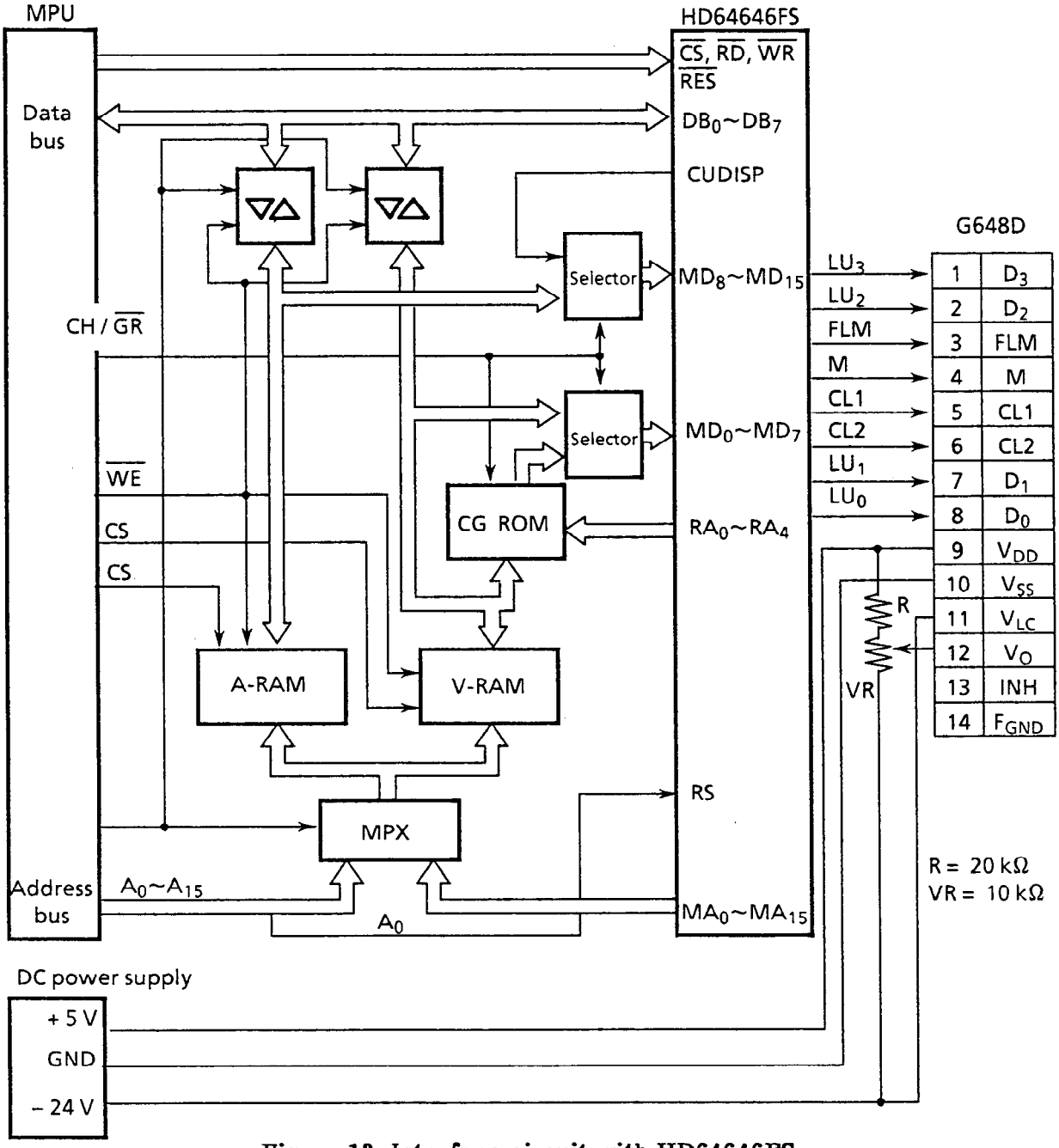


Figure 13 Interface circuit with HD64646FS

[Features of the HD64646FS]

- Interface with 80-series MPU possible
- Layered mode : OR (character and graphics)
- Character reverse, blinking, all black, all white
- Cursor
  - ON/OFF; blinking speed, form and position are programmable
- Character font
  - Vertical : 1 dot to 32 dots
  - Horizontal : 8 dots
- Scrolling
  - Vertical : smooth or character unit
  - Horizontal : character unit
- CMOS process
- 5-V single power supply

(4) YAMAHA V6366B

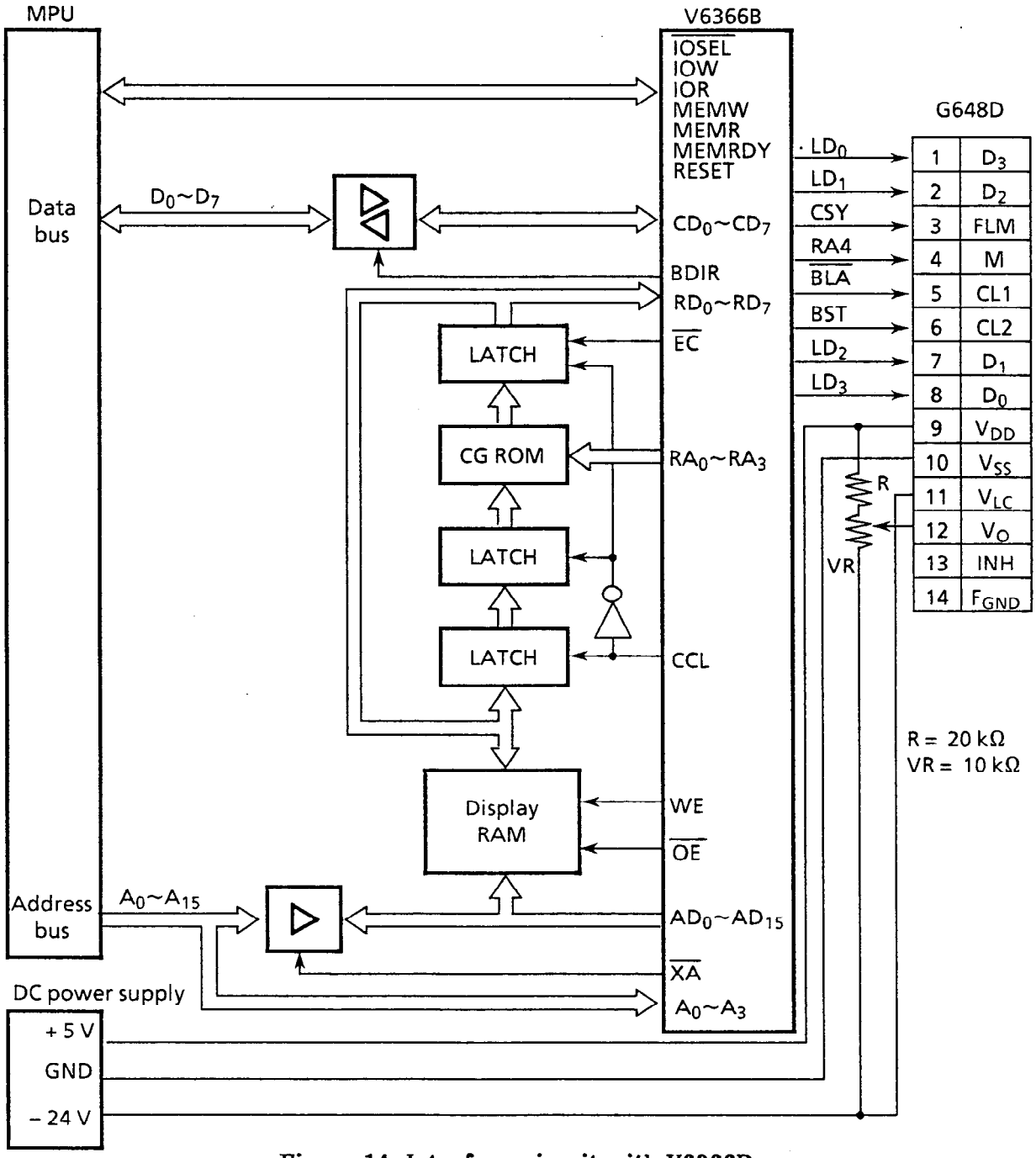


Figure 14 Interface circuit with V6366B

[Features of the V6366B]

- Compatible with CGA, MDA, and HGC for IBM-PC
- Gradation and hatching
- Cursor
  - ON/OFF/Blink; form and position are programmable
- Scrolling smoothly
- Character font
  - Vertical : 1 dot to 32 dots
  - Horizontal : 6, 7, 8, 9, 10, 8×integer dots
- CMOS process
- 5-V single power supply

2.4.2 Interface with video signal

When interfacing with SEIKO EPSON SED1341F controller, the G648D displays using separate video signals, without changing hardware or software. Both SED1341FOB and SED1341FOC can be used for G648D interface.

Figure 15 shows an example of interface circuit using the SED1341F.

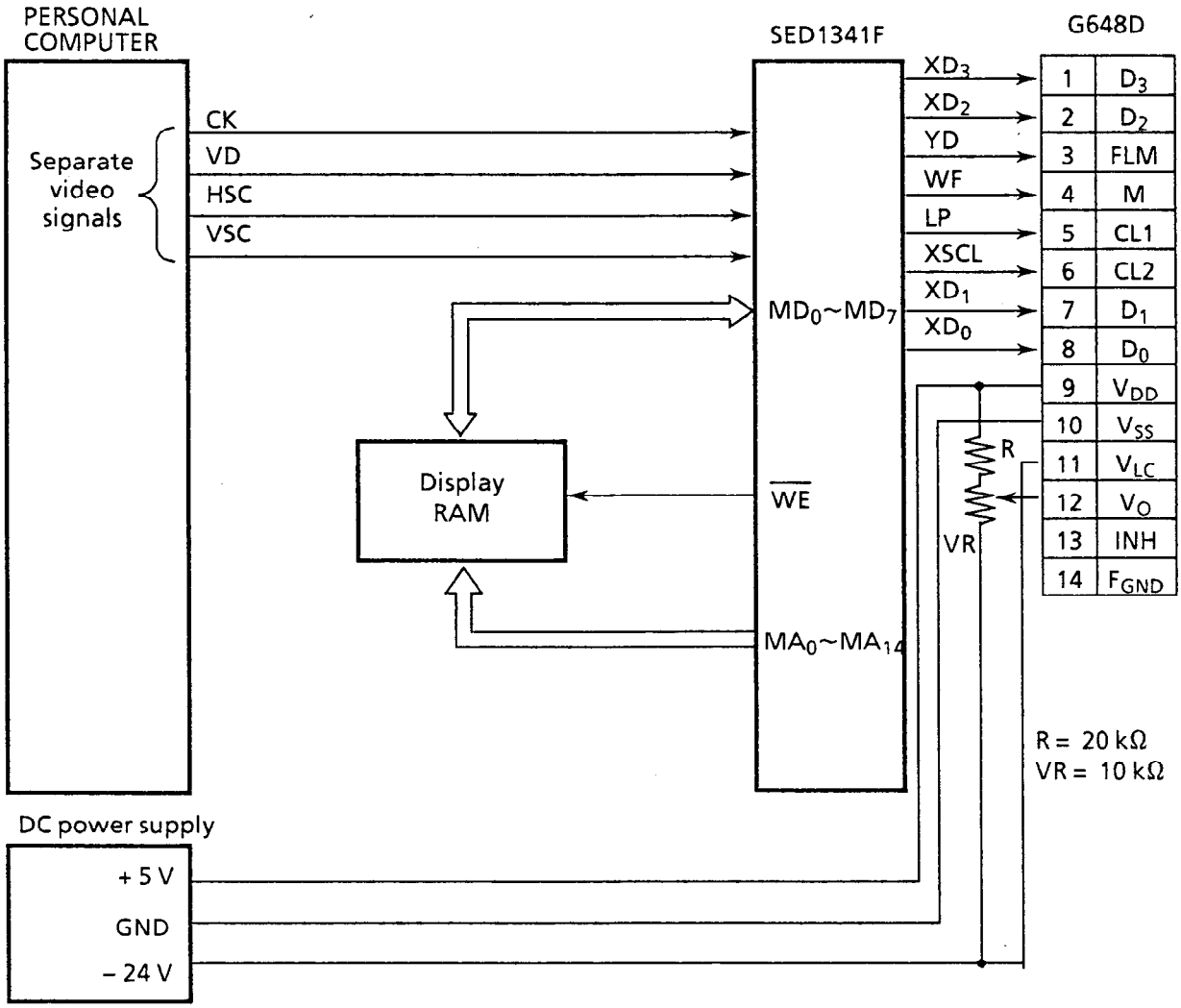


Figure 15 Interface circuit with SED1341F

[Features of the SED1341F]

- Separate signal input compatible with TTL
  - · Video data, Horizontal synchronizing signal, Vertical synchronizing signal, Dot clock
- Dot-clock generation with PLL, which has built-in PLL program counter and phase comparator. Clock frequency is selectable of 14.32 MHz typ. and 21.05 MHz typ.
- Fine adjustment of display position
  - · Register programming method via four-bit bus
- 5-V single power supply

3. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

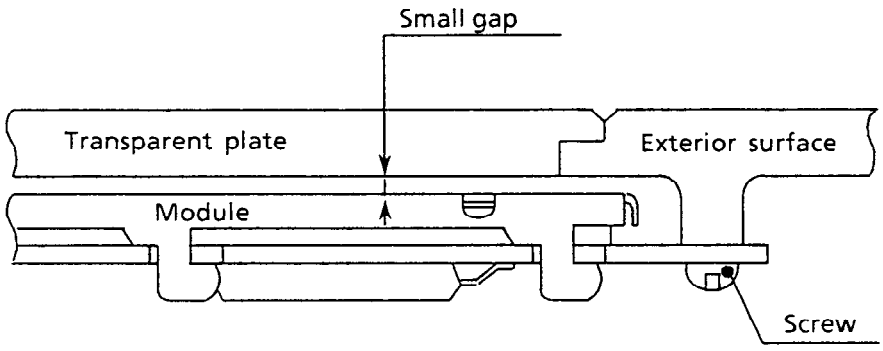
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is made of plate glass; do not hit or press against it.
- Do not remove the panel or frame from the module.
- The polarizer on the display is very fragile; handle it very carefully.

Mounting and Design

- Mount the module in the specified installation sections and holes.
- To protect the module from external pressure, put a plate of transparent material such as acrylic or glass over the display surface, frame, and polarizer. Leave a small gap between the transparent plate and the module.

☆Example



- Keep the module dry. Condensation can damage the transparent electrodes .

Storage

- Store the module in a dark place where the temperature is 25°C ±10°C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module or its components.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizer.

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