SL2ICS2001DW/V1D

I-CODE SLI Label IC bumped wafer specification on UV-tape

Rev. 3.0 — 5 February 2008 Product data sheet addendum
150030 PUBLIC

1. General description

This specification describes the electrical, physical and dimensional properties of Au-bumped sawn wafers on FFC with UV-tape of I-CODE SLI Label ICs on an NXP C075EE process and is the base for delivery of tested I-CODE SLI Label ICs.

2. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Odering code
SL2ICS2001DW/V1D	-	Bumped die on sawn wafer on UV-tape	9352 795 61005

3. Mechanical specification

3.1 Wafer

- Diameter: 8”
- Thickness: 150 μm ± 15 μm

3.2 Wafer backside

- Material: Si
- Treatment: ground and stress release
- Roughness: R_a max. 0.5 μm

  R_t max. 5 μm

3.3 Chip dimensions

- Chip size: 900 x 780 μm^2
- Scribe lines: 80 / 80 μm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride (on top)
- Thickness: 500 nm / 600 nm

3.5 Au bump

- Bump material: > 99.9 % pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
  - within a die: ± 2 μm
  - within a wafer: ± 3 μm
  - wafer to wafer: ± 4 μm
- Bump flatness: ± 1.5 μm
- Bump size:
  - LA, LB: 92 x 92 μm^2
  - VSS[1], TESTIO[1]: 62 x 62 μm^2
- Pad size (unbumped):
  - LA, LB: 78 x 78 μm^2
  - VSS[1], TESTIO[1]: 48 x 48 μm^2
- Bump size variation: ± 5 μm
- Under bump metallization: sputtered TiW

3.6 Fail die identification

Every die is electrically tested according to data sheet. Identification of chips with electrical parameters not conform with the data sheet is done by inking and wafer mapping (all dies at wafer periphery are identified as ‘FAIL’).

The ink information refers to unsawn wafers. At sawn wafers (on FFC) additional ICs are marked as ‘FAIL’ in the wafer map if damaged during the sawing process. These ICs will not be inked.

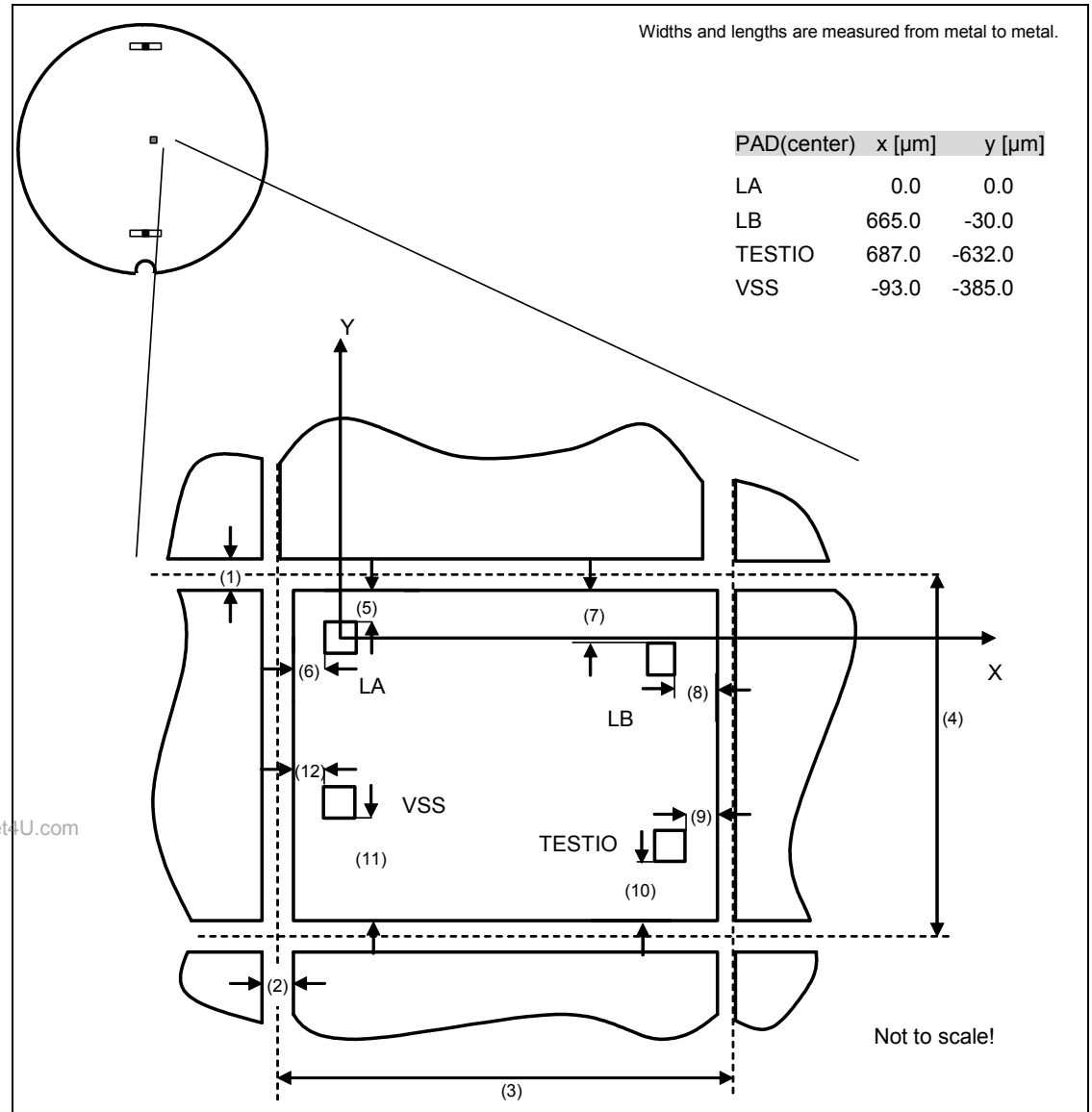
3.6.1 Wafer mapping

Wafer mapping for failed die information is available on floppy-disk.

Format: IBIS format

1. Pad VSS and TESTIO are disconnected when wafer is sawn

4. Chip orientation and bondpad locations



(1) X-Scribeline width: 80 µm
(2) Y-Scribeline width: 80 µm
(3) Chip step, x-length: X-Scribeline + 900 µm
(4) Chip step, y-length: Y-Scribeline + 780 µm
(5) LA bump edge to chip edge, y-length: 39[+7] µm
(6) LA bump edge to chip edge, x-length: 104[+7] µm
(7) LB bump edge to chip edge, y-length: 69[+7] µm
(8) LB bump edge to chip edge, x-length: 39[+7] µm
(9) TESTIO bump edge to chip edge, x-length: 32[+7] µm
(10) TESTIO bump edge to chip edge, y-length: 32[+7] µm
(11) VSS bump edge to chip edge, y-length: 279[+7] µm
(12) VSS bump edge to chip edge, x-length: 26[+7] µm

[+7µm] *…for pad edge to chip edge!*

Fig 1. Chip orientation and bondpad locations

5. Limiting values

Table 2. Limiting values[1][2]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	Storage temperature range		-55	+140	°C
Tj	Junction temperature		-55	+140	°C
V_{ESD}	ESD voltage immunity	[3]	-	±2	kV_{peak}
$I_{max\ LA-LB}$	Maximum input peak current		-	±60	mA_{peak}
T_{jop}	Operating junction temperature		-25	+85	°C
I_{LA-LB}	Input current	[4]	-	30	mA_{rms}

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] MIL-STD-883D, Method 3015.7, Human body model

[4] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_{LA-LB})

6. Characteristics

6.1 Electrical characteristics

Table 3. Characteristics [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{jop} = -25 to 85°C							
V_{LA-LB}	Minimum supply voltage for READ/WRITE/EAS			±2.5	±2.6	±2.9	V_{rms}
f_{op}	Operating frequency		[2]	13.553	13.560	13.567	MHz
C_{res}	Input capacitance between LA – LB	V_{LA-LB} = 2 V_{rms}	[3]	22.3	23.5	24.7	pF
P_{min}	Minimum operating supply power		[4]	-	280	-	µW
m	Modulation of RF voltage for demodulator response	$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$	[5]	-	-	-	%
$t_{P\ sm}$	Modulation pulse length of RF voltage		[5]	-	-	-	µs
t_D	Demodulator response time	m ≥ 10 %, 100 %	[5]	-	-	-	µs
R_{mod}	Load modulation		[5]	-	-	-	Ω
t_{ret}	EEPROM Data retention	T_{amb} ≤ 55 °C		10	-	-	Years
n_{write}	EEPROM Write endurance			100000	-	-	Cycles

[1] Typical ratings are not guaranteed. These values listed are at room temperature.

[2] Bandwidth limitation (±7 kHz) according to ISM band regulations.

[3] Measured with an HP4285A LCR meter at 13.56 MHz.

[4] Including losses in resonant capacitor and rectifier.

[5] Refer to ISO/IEC 15693-2 and 15693-3 including pulse shapes and tolerances; proper coil design assumed.

7. Final wafertest specification

- Mininum yield per wafer: 30 % of 35416 potential good dies.
- Minimum yield per lot: 30 %

8. Hints for label IC encapsulation

8.1 Protection against visible light

As a result of the ultra low power design of the I-CODE SLI Label IC some analogue circuits on the chip are light sensitive. This means that common sun light can impact the operation of the label if the chip is not protected against visible light radiation.

Measurements have shown that a radiation of E_{max} = 60 W/m^2 (spectrum: 400 to 1000 nm) causes a reduced operating range of the plain chip.

Measurements of direct sunlight in summer deliver values up to 260 W/m^2.

To ensure proper operation an expected minimum radiation reduction factor of approx. 9 (2 x 260/60 = 8.7) must be provided by the encapsulation. That means special care has to be taken to ensure a sufficient light protection of the I-CODE SLI Label IC (e.g. non translucent encapsulation or underfiller, …) according to application requirements.

8.2 Protection against UV light

An EEPROM memory, as it is also used in the I-CODE SLI Label IC, has some principle sensitivity to UV light (applies to EEPROM-technology in general).

Thus strong UV exposure in the production of inlets/labels has to be avoided. UV protection has to be ensured using appropriate assembly methods.

8.3 Resistance to x-rays

X-ray exposure on comparable NXP ICs (with even smaller feature size) caused neither a long term influence on the behaviour of the ICs nor on the data retention of the EEPROMs.

9. References

- Data sheet “I-CODE SLI Label IC, functional specification”
- Data sheet “General specification for 8” wafer”
- Data sheet “General quality specification”
- Application note “I-CODE coil design guide”
- Application note “Specification of the IBIS wafermap”
- Application note “Handling and processing of sawn wafers on UV dicing tape”

10. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
150030	5 February 2008	Product data sheet	-	-
	• Initial version			

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Tables

14. Figures

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Date of release: 5 February 2008
Document identifier: 150030