



STB80NF55-06T

N-channel 55 V, 5 m Ω , 80 A STripFET™ II Power MOSFET
in a D²PAK package

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D
STB80NF55-06T	55 V	< 6.5 m Ω	80A

- Exceptional dv/dt capability

Applications

- Switching application
- Automotive

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

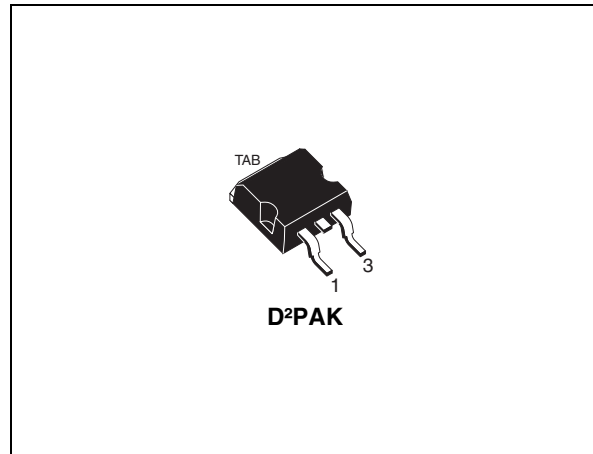


Figure 1. Internal schematic diagram

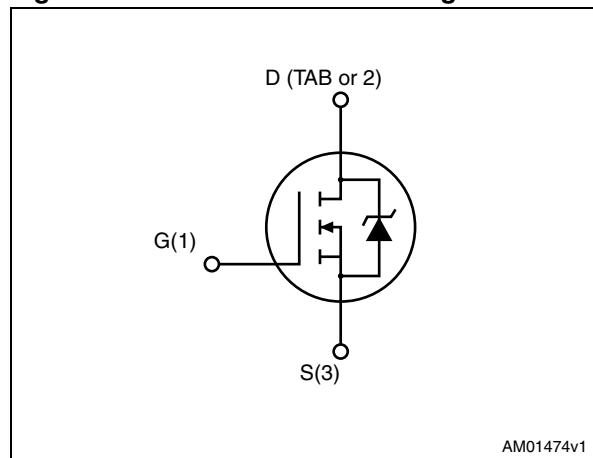


Table 1. Device summary

Order code	Marking	Package	Packaging
STB80NF55-06T	B80NF55-06T	D ² PAK	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuit	8
4	Package mechanical data	9
5	Packing mechanical data	12
6	Revision history	14

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	55	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{tot}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
P_1	Long term load test ($I_D = 100\text{ A}$, $V_{SD} = 15\text{ V}$, $T_{pulse} = 10\text{ msec}$) ΔV_{SD} (tested)	150	W
$P_2^{(3)}$	Short term load test ($I_D = 75\text{ A}$, $V_{SD} = 15\text{ V}$, $T_{pulse} = 700\text{ msec}$) ΔV_{SD} (not tested)	1125	W
	Derating Factor	2	W/ $^\circ\text{C}$
$dv/dt^{(4)}$	Peak diode recovery avalanche energy	7	V/ns
$E_{AS}^{(5)}$	Single pulse avalanche energy	1.3	J
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Guaranteed by process.
4. $I_{SD} \leq 80\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
5. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 30\text{ A}$, $V_{DD} = 30\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max.	0.5	$^\circ\text{C}/\text{W}$
Rthj-pcb ⁽¹⁾	Thermal resistance junction-to pcb max.	35	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR4 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	55			V
V_{BR0}		$V_{GS} = 1.5\ \text{V}$, $I_D = 250\ \mu\text{A}$	40			V
V_{BR1}		$V_{GS} = 1.5\ \text{V}$, $I_D = 10\ \text{mA}$	40			V
V_{BR2}		$V_{GS} = 1.5\ \text{V}$, $I_D = 100\ \text{mA}$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 55\ \text{V}$ $V_{DS} = 55\ \text{V}$, $T_C = 125\ \text{°C}$			10 100	μA μA
$I_{GSS}^{(1)}$	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$V_{GS(th)}^{(2)}$		$T_J = 175\ \text{°C}$, $V_{DS} = V_{GS}$ $I_D = 1\ \text{mA}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 40\ \text{A}$		5.0	6.5	m Ω

1. Tested @ $V_{GS} = \pm 22\ \text{V}$ at wafer level.

2. Guaranteed by process.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$	-	4400		pF
C_{oss}	Output capacitance			1020		pF
C_{rss}	Reverse transfer capacitance			350		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 27\ \text{V}$, $I_D = 60\ \text{A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 13)	-	27		ns
t_r	Rise time			155		ns
$t_{d(off)}$	Turn-off delay time			125		ns
t_f	Fall time			65		ns
Q_g	Total gate charge	$V_{DD} = 44\ \text{V}$, $I_D = 80\ \text{A}$, $V_{GS} = 4.5\ \text{V}$, $R_G = 10\ \Omega$ (see Figure 14)	-	142	193	nC
Q_{gs}	Gate-source charge			29		nC
Q_{gd}	Gate-drain charge			60.5		nC

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 35\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15)	-	100 0.32 6.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

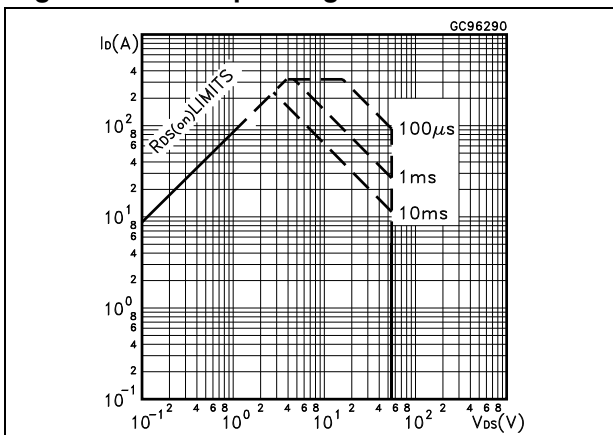


Figure 3. Thermal impedance

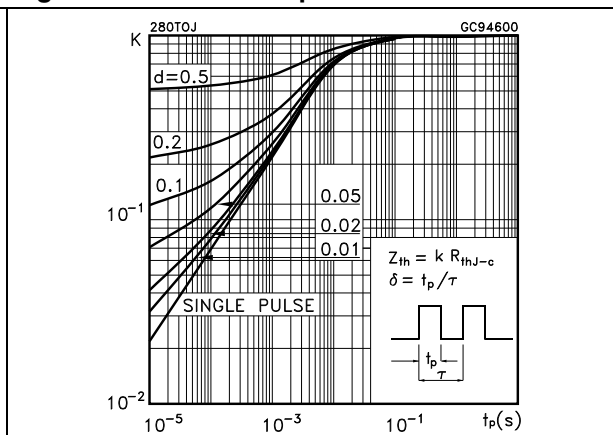


Figure 4. Output characteristics

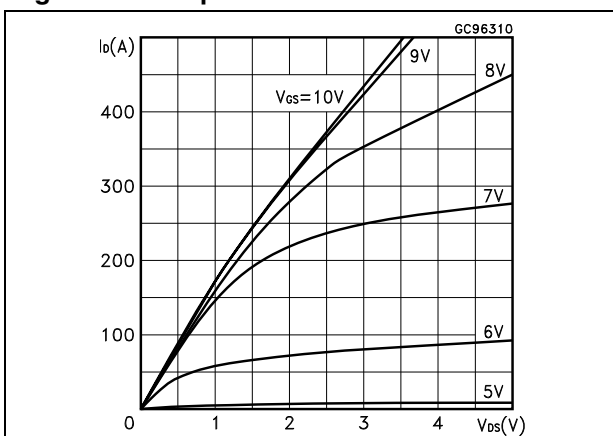


Figure 5. Transfer characteristics

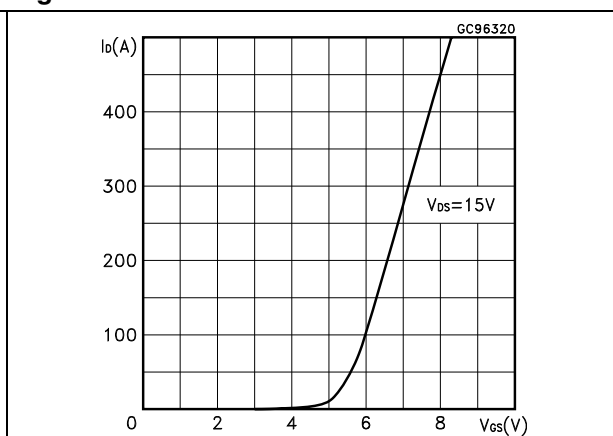


Figure 6. Normalized BV_{DSS} vs. temperature

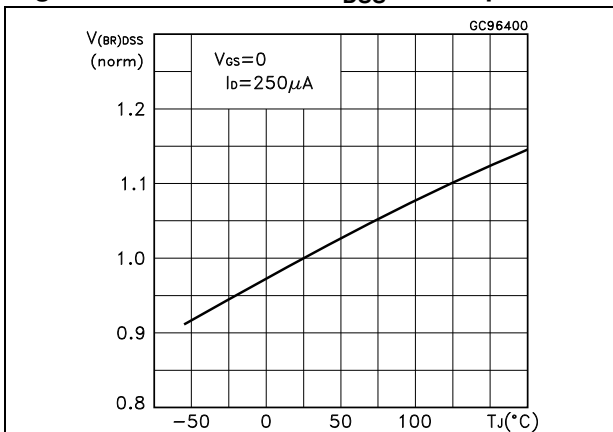


Figure 7. Static drain-source on-resistance

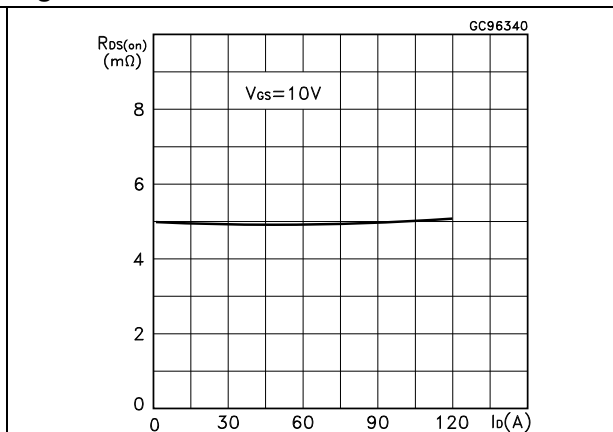


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

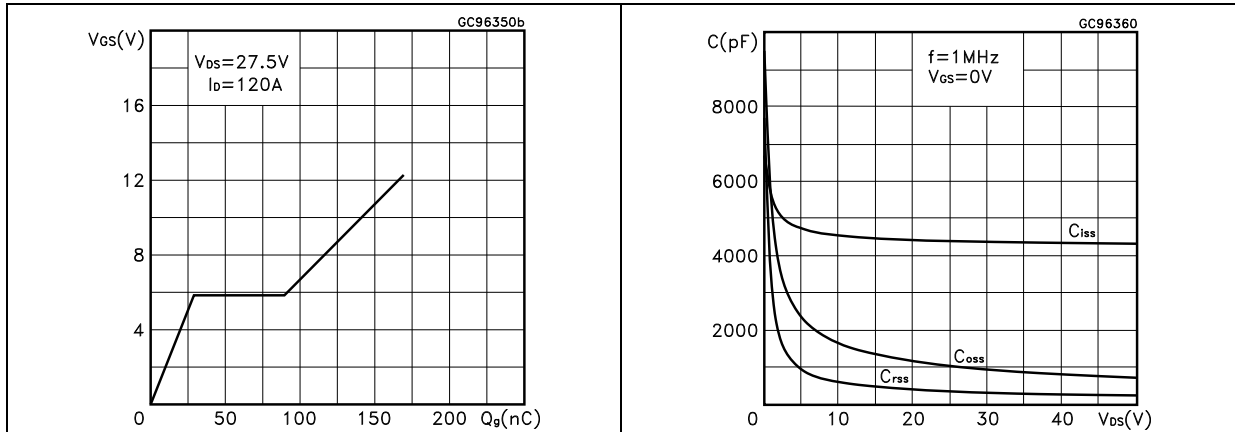


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on-resistance vs. temperature

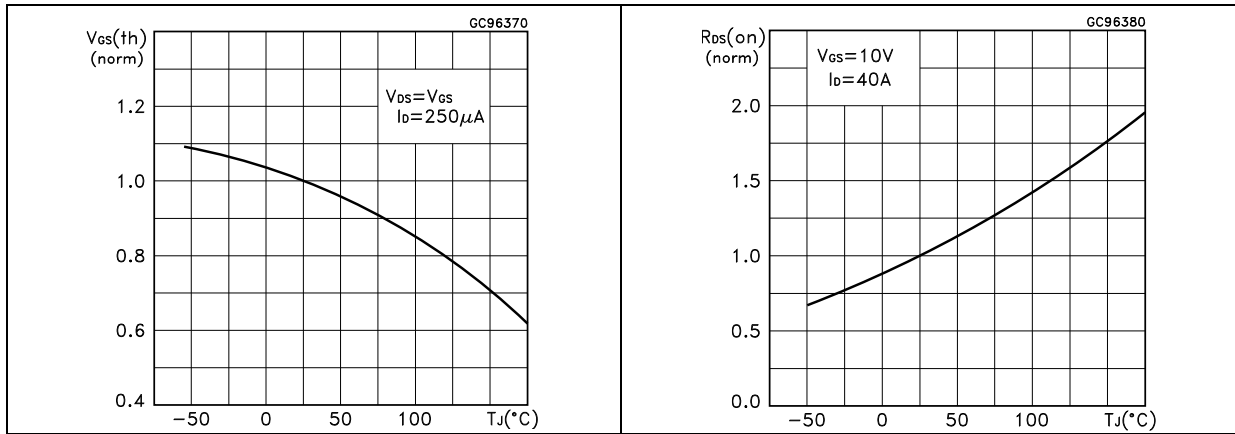
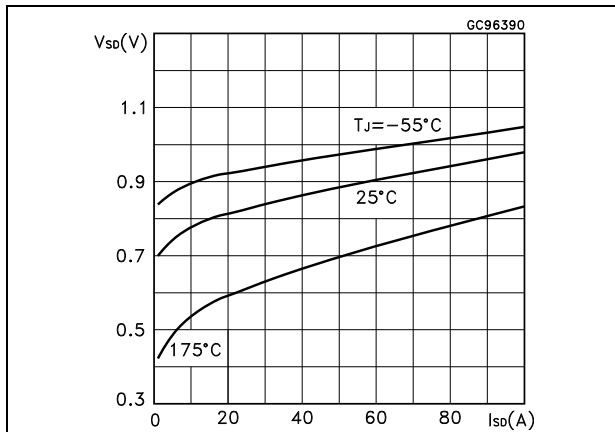


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

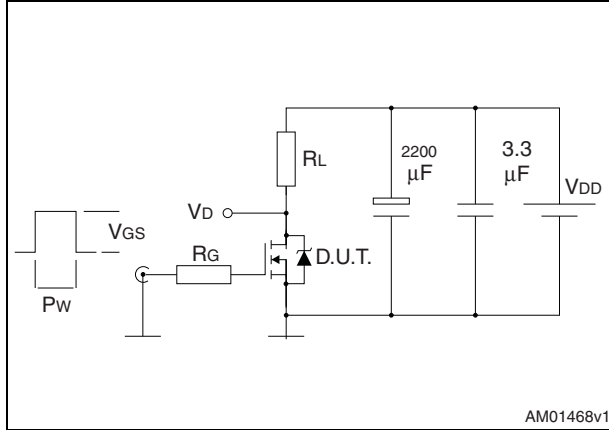


Figure 14. Gate charge test circuit

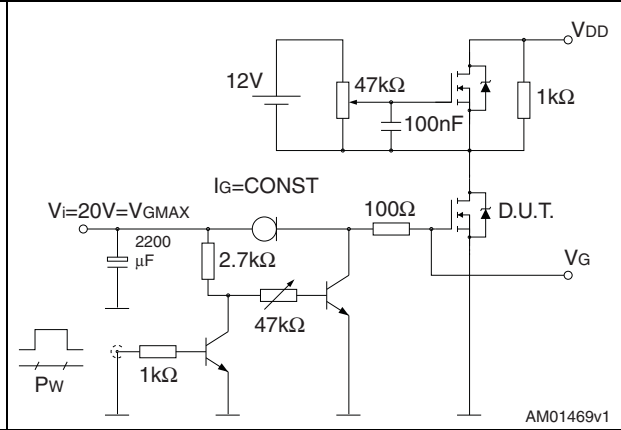


Figure 15. Test circuit for inductive load switching and diode recovery times

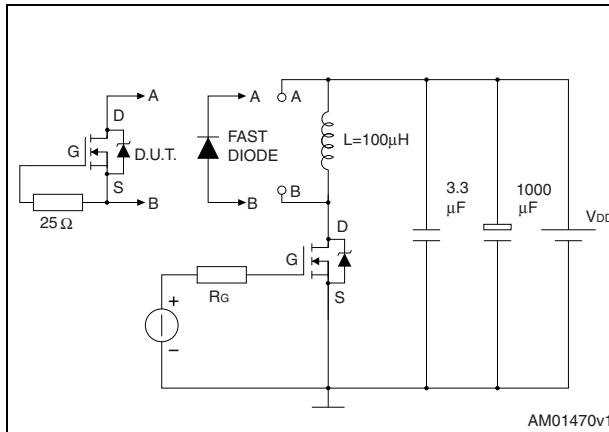


Figure 16. Unclamped Inductive load test circuit

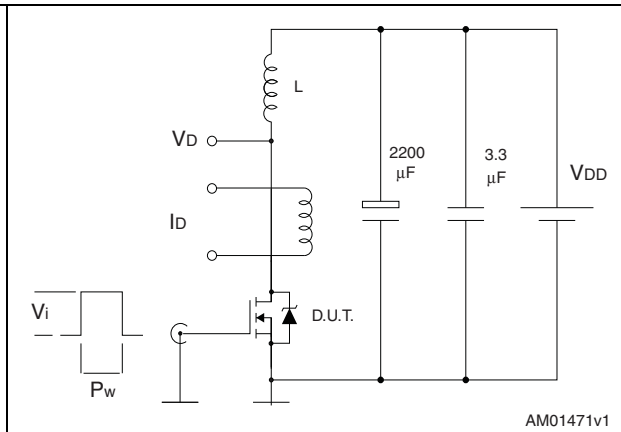


Figure 17. Unclamped inductive waveform

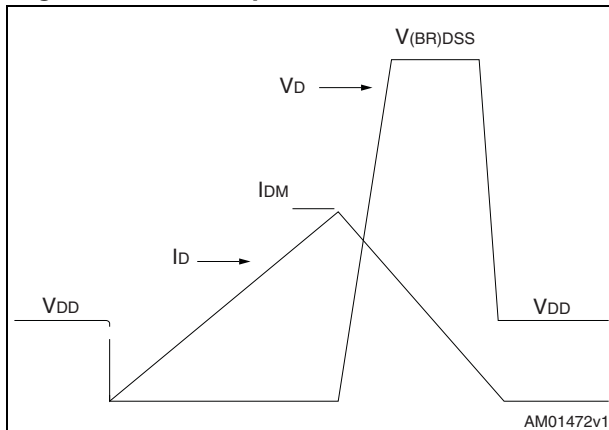
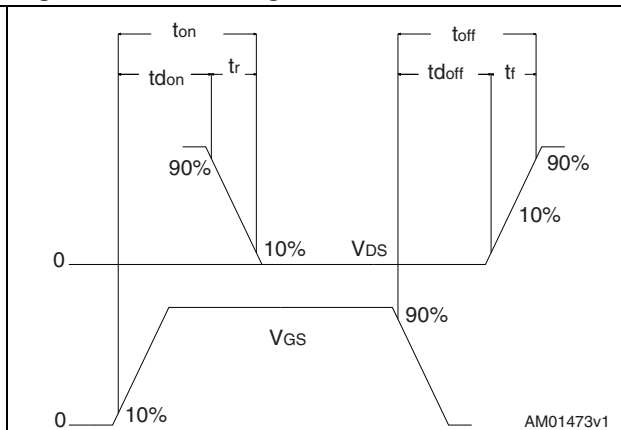


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 7. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 19. D²PAK (TO-263) drawing

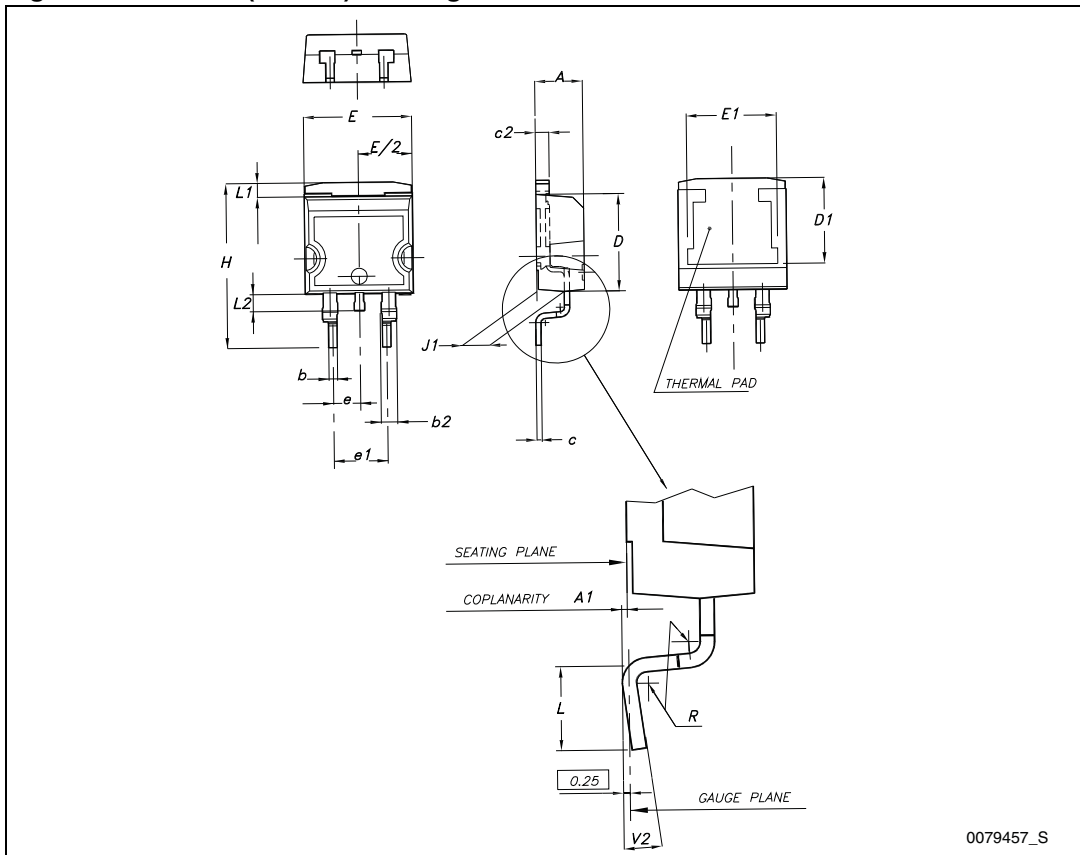


Figure 20. D²PAK footprint^(a)



a. All dimensions are in millimeters

5 Packing mechanical data

Table 8. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 21. Tape for D²PAK (TO-263)

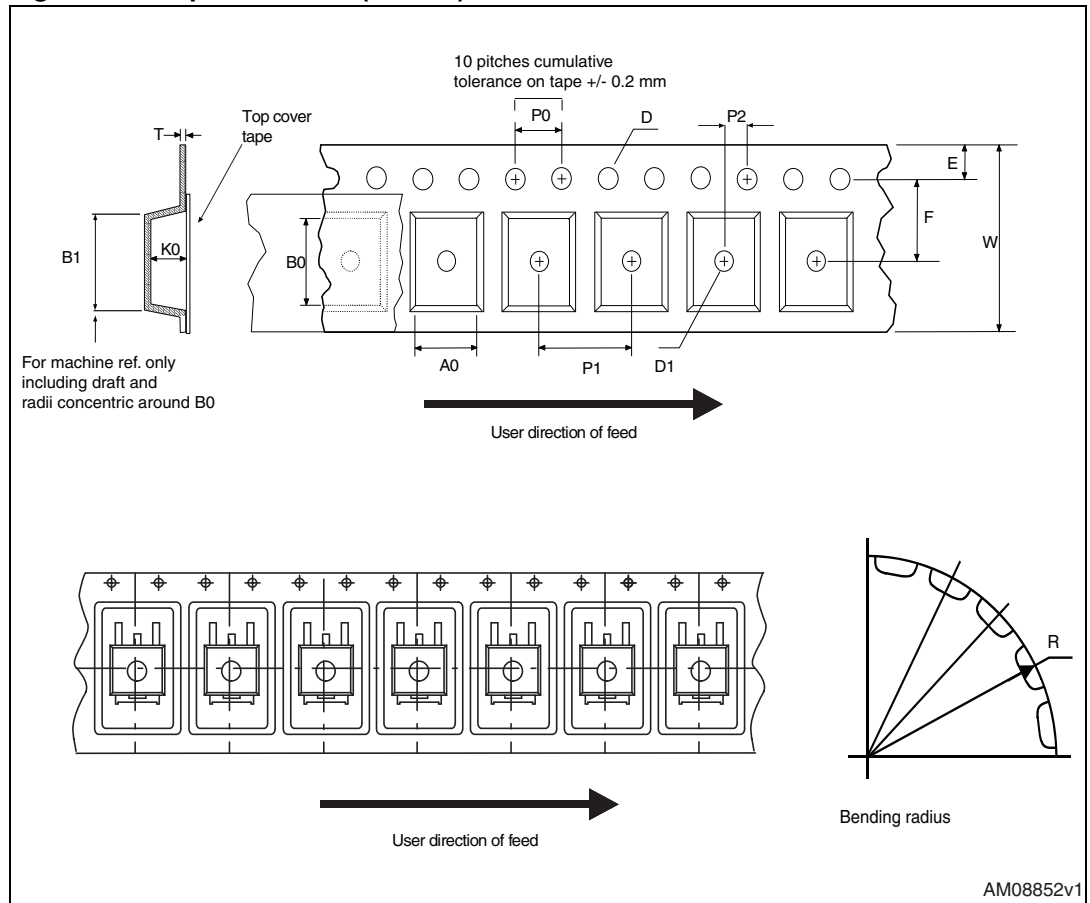
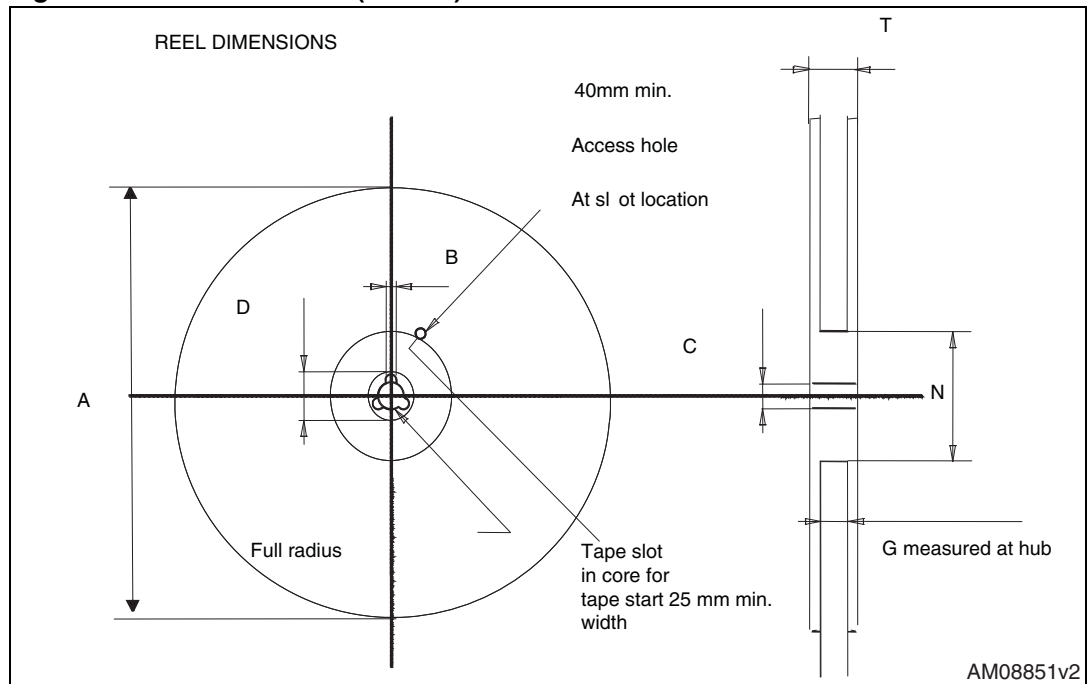


Figure 22. Reel for D²PAK (TO-263)



6 Revision history

Table 9. Revision history

Date	Revision	Changes
19-Jan-2012	1	First issue.

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